# 54LS02, 54S02
## Gates

**Quad Two-Input NOR Gate**
***Product Specification***



### FUNCTION TABLE

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| L | L | H |
| L | H | L |
| H | L | L |
| H | H | L |

H = HIGH voltage level
L = LOW voltage level

### ORDERING INFORMATION

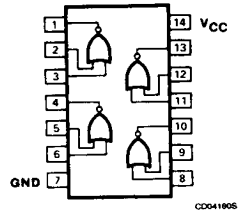
| PACKAGES | ORDER CODE |
|---|---|
| Ceramic DIP | 54LS02/BCA, 54S02/BCA |
| Ceramic Flat Pack | 54LS02/BDA, 54S02/BDA |
| Ceramic LLCC | 54LS02/B2C |

### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 54S | 54LS |
|---|---|---|---|
| A, B | Inputs | 1SUL | 1LSUL |
| Y | Output | 10SUL | 10LSUL |

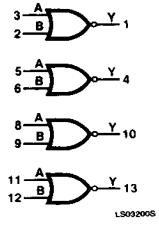
**NOTE:**
Where a 54S Unit Load (SUL) is 50$\mu$A $I_{IH}$ and −2.0mA $I_{IL}$, and 54LS Unit Load (LSUL) is 20$\mu$A $I_{IH}$ and −0.4mA $I_{IL}$.

### PIN CONFIGURATION



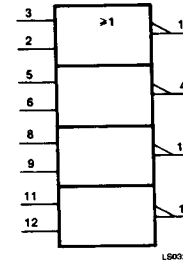

For LLCC pin assignments, see Package Section.

### LOGIC SYMBOL




For LLCC pin assignments, see Package Section.

### LOGIC SYMBOL (IEEE/IEC)




For LLCC pin assignments, see Package Section.

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER | 54LS | 54S | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | 7.0 | 7.0 | V |
| $V_I$ | Input voltage range | −0.5 to +7.0 | −0.5 to +5.5 | V |
| $I_I$ | Input current range | −30 to +1 | −30 to +5 | mA |
| $V_O$ | Voltage applied to output in HIGH output state range | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | V |
| $T_{STG}$ | Storage temperature range | −65 to +150 | | °C |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | | 54LS | | | 54S | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.0 | 5.5 | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | HIGH-level input voltage | | 2.0 | | | 2.0 | | | V |
| $V_{IL}$ | LOW-level input voltage | | | | +0.7 | | | +0.8 | V |
| | | +125°C | | | +0.7 | | | +0.7 | |
| $I_{IK}$ | Input clamp current | | | | −18 | | | −18 | mA |
| $I_{OH}$ | HIGH-level output current | | | | −400 | | | −1000 | μA |
| $I_{OL}$ | LOW-level output current | | | | 8 | | | 20 | mA |
| $T_A$ | Operating free-air temperature range | | −55 | | +125 | −55 | | +125 | °C |

## DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER | TEST CONDITIONS[1] | | 54LS02 | | | 54S02 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[2] | Max | Min | Typ[2] | Max | |
| $V_{OH}$ | HIGH-level output voltage | $V_{CC}$ = MIN, $V_{IL}$ = MAX, $I_{OH}$ = MAX | | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| $V_{OL}$ | LOW-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = MIN, $V_{IL}$ = MAX, $I_{OL}$ = MAX | | | 0.25 | 0.4 | | | 0.5 | V |
| | | | +125°C | | | 0.4 | | | 0.45 | |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = $I_{IK}$ | | | | −1.5 | | | −1.2 | V |
| $I_{IH2}$ | Input current at maximum input voltage | $V_{CC}$ = MAX | $V_I$ = 5.5V | | | | | | 1.0 | mA |
| | | | $V_I$ = 7.0V | | | 0.1 | | | | |
| $I_{IH1}$ | HIGH-level input current | $V_{CC}$ = MAX | $V_I$ = 2.4V | | | | | | | μA |
| | | | $V_I$ = 2.7V | | | 20 | | | 50 | |
| $I_{IL}$ | LOW-level input current | $V_{CC}$ = MAX | $V_I$ = 0.4V | | | −0.4 | | | | mA |
| | | | $V_I$ = 0.5V | | | | | | −2.0 | |
| $I_{OS}$ | Short-circuit output current[3] | $V_{CC}$ = MAX | | −20 | | −100 | −40 | | −100 | mA |
| $I_{CC}$ | Supply current (total) | $V_{CC}$ = MAX | $I_{CCH}$ Outputs HIGH | | 1.6 | 3.2 | | 17 | 29 | mA |
| | | | $I_{CCL}$ Outputs LOW | | 2.8 | 5.4 | | 26 | 45 | |

**NOTES:**

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

## AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

| SYMBOL | PARAMETER | TEST CONDITIONS | 54LS $C_L = 15pF$ | | 54S $C_L = 15pF$ | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay | Waveform 1 | | 15<br>15 | | 5.5<br>5.5 | ns |

## AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$[4]

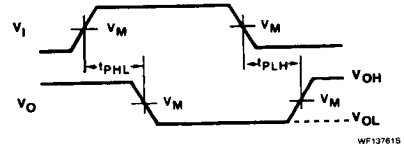
| SYMBOL | PARAMETER | TEST CONDITIONS | 54LS $C_L = 50pF$ | | 54S $C_L = 50pF$ | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay | Waveform 1 | | 20<br>20 | | 7.0<br>7.0 | ns |

**NOTE:**
4. These parameters are guaranteed, but not tested.

## AC ELECTRICAL CHARACTERISTICS $T_A = -55°C$ and $+125°C$, $V_{CC} = 5.0V$[4]

| SYMBOL | PARAMETER | TEST CONDITIONS | 54LS $C_L = 50pF$ | | 54S $C_L = 50pF$ | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay | Waveform 1 | | 26<br>26 | | 9.0<br>9.0 | ns |

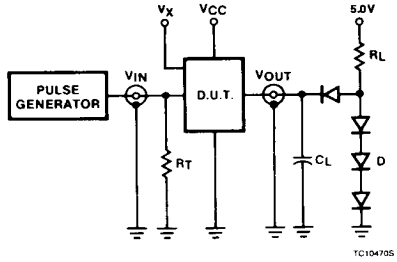
## AC WAVEFORM



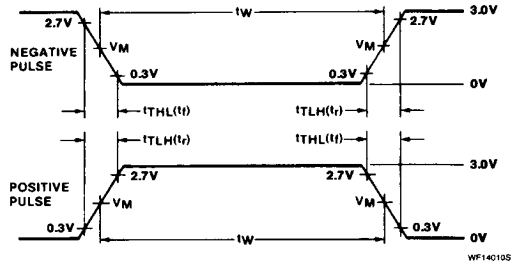

**NOTE:** $V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

**Waveform 1. Waveform for Inverting Outputs**

## TEST CIRCUIT AND WAVEFORM




Test Circuit for 54 Totem-Pole Outputs




Input Pulse Definition

| FAMILY | INPUT PULSE CHARACTERISTICS | | | | | |
|---|---|---|---|---|---|---|
| | $R_L$ | $V_M$ | Rep. Rate | $T_W$ | $T_{TLH}$ | $T_{THL}$ |
| 54LSXXX | 2.0kΩ | 1.3V | 1MHz | 500ns | ⩽15ns | ⩽6ns |
| 54XXX | 400Ω | 1.5V | 1MHz | 500ns | ⩽7ns | ⩽7ns |
| 54SXXX | 280Ω | 1.5V | 1MHz | 500ns | ⩽2.5ns | ⩽2.5ns |

DEFINITIONS
$C_L$ = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
$R_T$ = Termination resistance should be equal to $Z_{OUT}$ of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
$V_X$ = Unclocked pins must be held at: ⩽0.8V, ⩾2.7V or open per function table.