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Kind regards,

Team Nexperia

PSMN8R0-40PS

N-channel 40 V 7.6 mΩ standard level MOSFET

Rev. 02 — 25 June 2009 — Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in TO220 package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive sources

1.3 Applications

- DC-to-DC convertors
- Load switching
- Motor control
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference

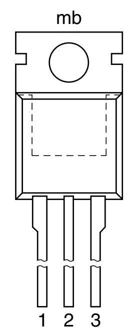
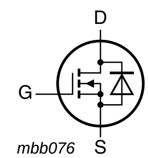
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	-	40	V
I_D	drain current	$T_{mb} = 25$ °C; $V_{GS} = 10$ V; see Figure 1		-	-	77	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2		-	-	86	W
Dynamic characteristics							
Q_{GD}	gate-drain charge	$V_{GS} = 10$ V; $I_D = 25$ A; $V_{DS} = 20$ V; see Figure 14; see Figure 15		-	3.8	-	nC
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 25$ A; $T_j = 25$ °C; see Figure 13	[1]	-	6.2	7.6	mΩ

[1] Measured 3 mm from package.

founded by Philips

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 **SOT78 (TO-220AB)**	
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

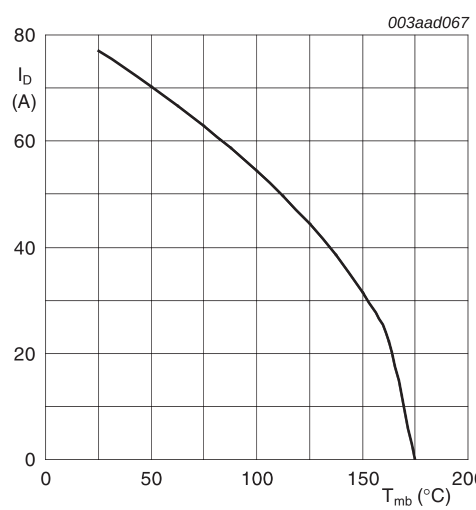
Type number	Package		
	Name	Description	Version
PSMN8R0-40PS	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78

4. Limiting values

Table 4. Limiting values

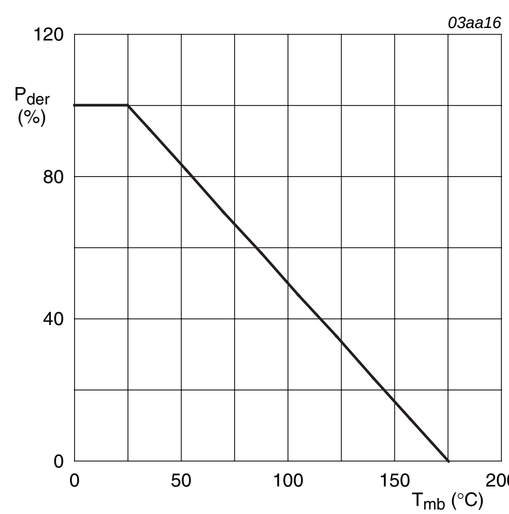
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	-	40	V
V_{DGR}	drain-gate voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C; $R_{GS} = 20$ kΩ	-	40	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10$ V; $T_{mb} = 100$ °C; see Figure 1	-	55	A
		$V_{GS} = 10$ V; $T_{mb} = 25$ °C; see Figure 1	-	77	A
I_{DM}	peak drain current	$t_p \leq 10$ µs; pulsed; $T_{mb} = 25$ °C; see Figure 3	-	309	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2	-	86	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25$ °C	-	77	A
I_{SM}	peak source current	$t_p \leq 10$ µs; pulsed; $T_{mb} = 25$ °C	-	309	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; $I_D = 77$ A; $V_{sup} \leq 40$ V; unclamped; $R_{GS} = 50$ Ω	-	43	mJ



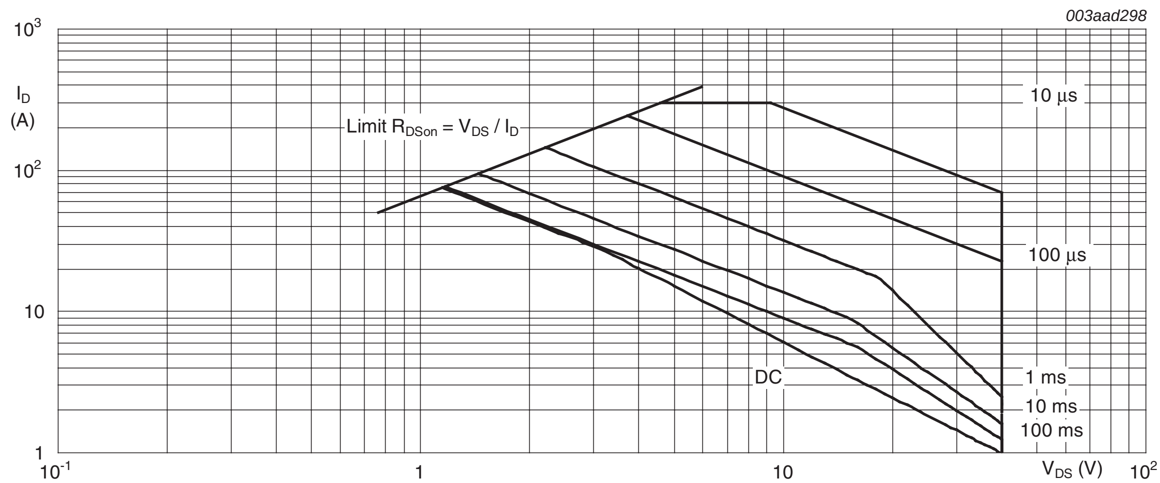
$$V_{GS} \geq 10\,V$$

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$T_{mb} = 25\,°C; I_{DM}$ is single pulse

(1) Capped at 100 A due to package.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	1.2	1.74	K/W

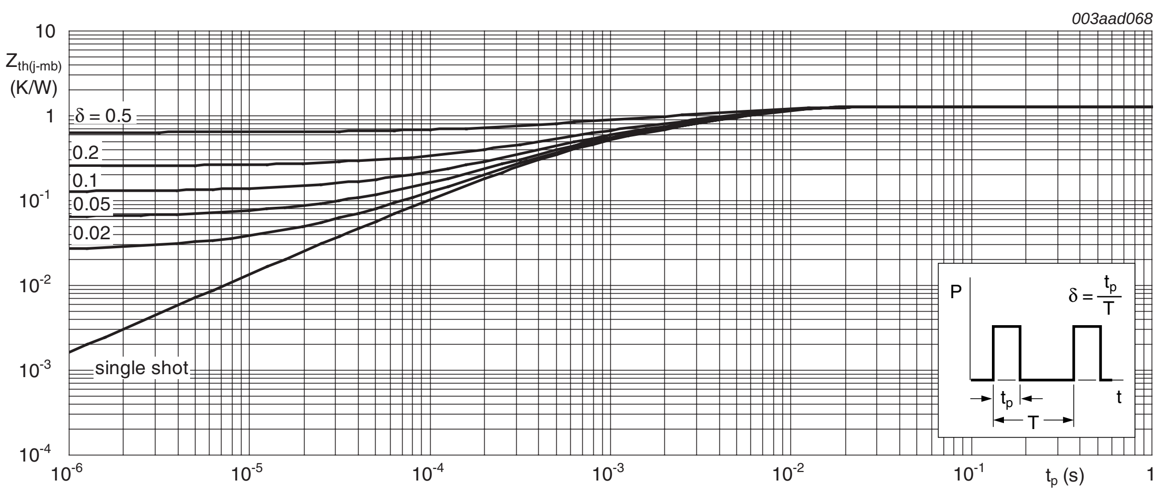


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration; typical values

6. Characteristics

Table 6. Characteristics

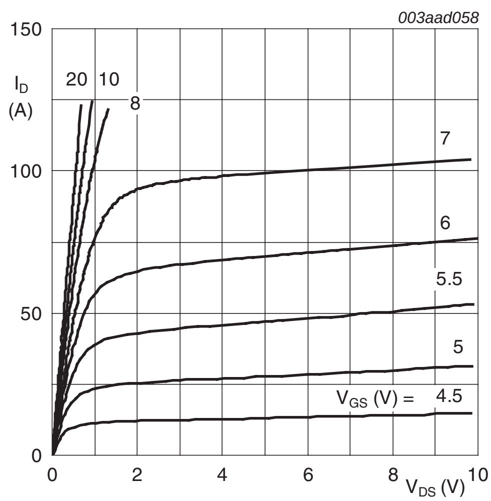
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		36	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		40	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 11; see Figure 12		-	-	4.6	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; see Figure 11; see Figure 12		1	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 11; see Figure 12		2	3	4	V
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 °C		-	-	1.5	µA
		V_{DS} = 40 V; V_{GS} = 0 V; T_j = 125 °C		-	-	30	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 100 °C; see Figure 13		-	-	11	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; see Figure 13	[2]	-	6.2	7.6	mΩ
R_G	internal gate resistance (AC)	f = 1 MHz		-	1.1	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V		-	17	-	nC
		I_D = 25 A; V_{DS} = 20 V; V_{GS} = 10 V; see Figure 14; see Figure 15		-	21	-	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 20 V; V_{GS} = 10 V; see Figure 14; see Figure 15		-	7.2	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge	I_D = 25 A; V_{DS} = 20 V; V_{GS} = 10 V; see Figure 14		-	3.6	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	3.6	-	nC
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 20 V; V_{GS} = 10 V; see Figure 14; see Figure 15		-	3.8	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 25 A; V_{DS} = 20 V; see Figure 14		-	4.8	-	V
C_{iss}	input capacitance	V_{DS} = 12 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; see Figure 16		-	1262	-	pF
C_{oss}	output capacitance			-	327	-	pF
C_{rss}	reverse transfer capacitance			-	160	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 12 V; R_L = 0.5 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 4.7 Ω		-	12	-	ns
t_r	rise time			-	4.7	-	ns
$t_{d(off)}$	turn-off delay time			-	21	-	ns
t_f	fall time			-	4.7	-	ns

Table 6. Characteristics *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 17	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 50 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V	-	30	-	ns
Q_r	recovered charge	I_S = 50 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; T_j = 25 °C	-	18	-	nC

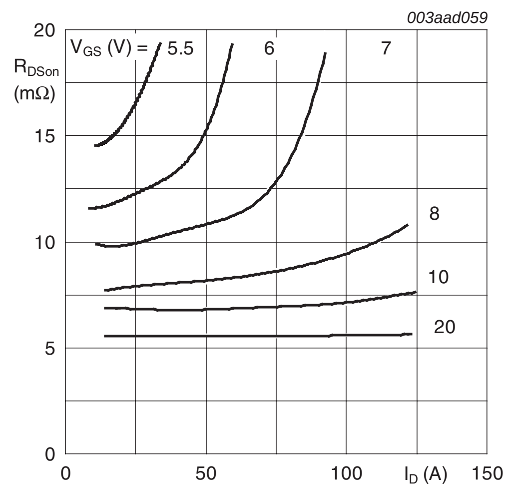
[1] Tested to JEDEC standards where applicable.

[2] Measured 3 mm from package.



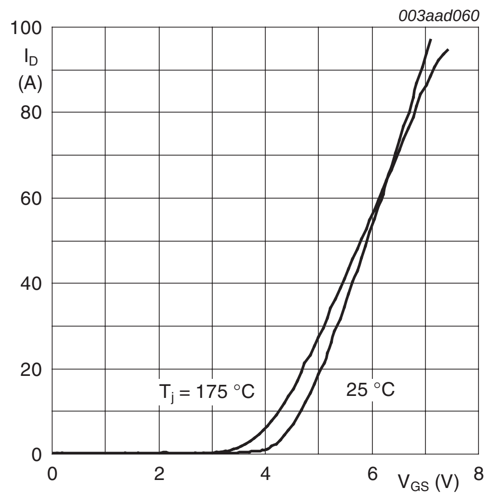
$T_j = 25\,°C; t_p = 300\mu s$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



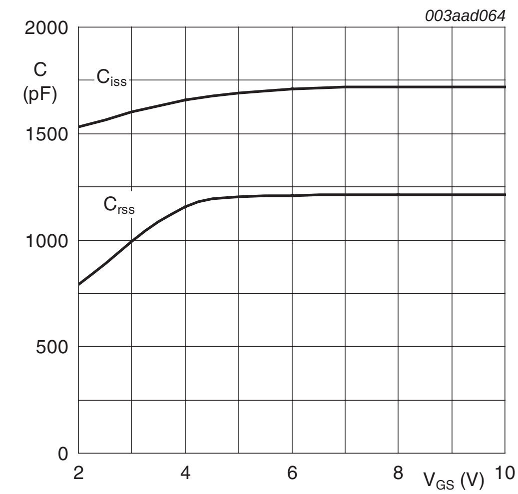
$T_j = 25\,°C; t_p = 300\mu s$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



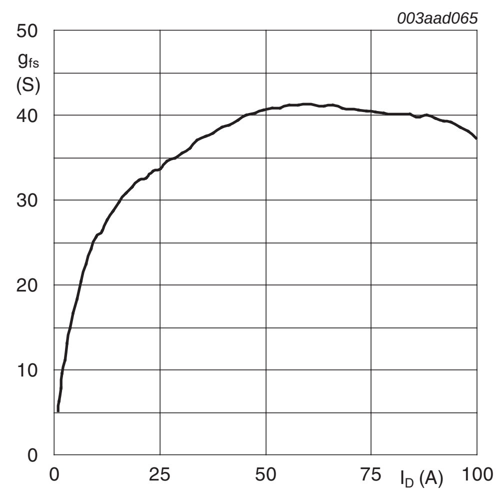
$V_{DS} = 15V$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



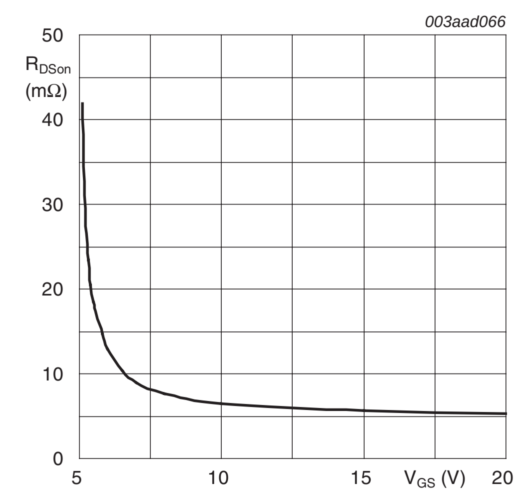
$V_{DS} = 0V; f = 1MHz$

Fig 8. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



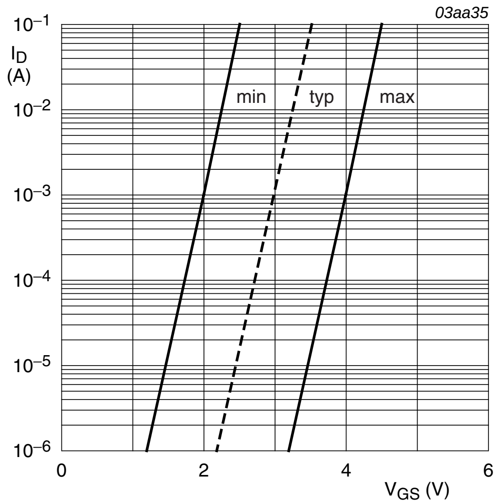
$T_j = 25°C; V_{DS} = 15V$

Fig 9. Forward transconductance as a function of drain current; typical values



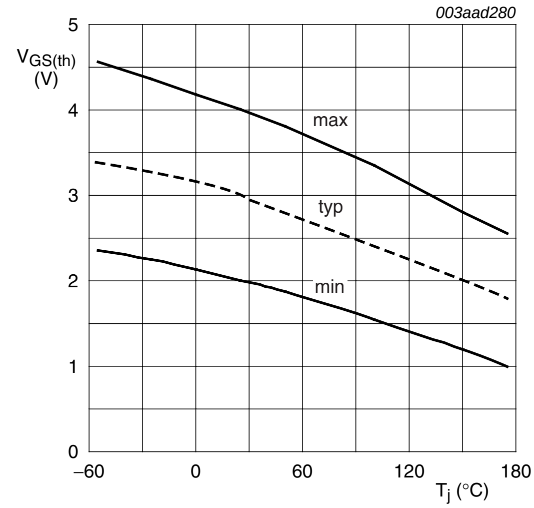
$T_j = 25°C; I_D = 25A$

Fig 10. Drain-source on-state resistance as a function of gate-source voltage; typical values



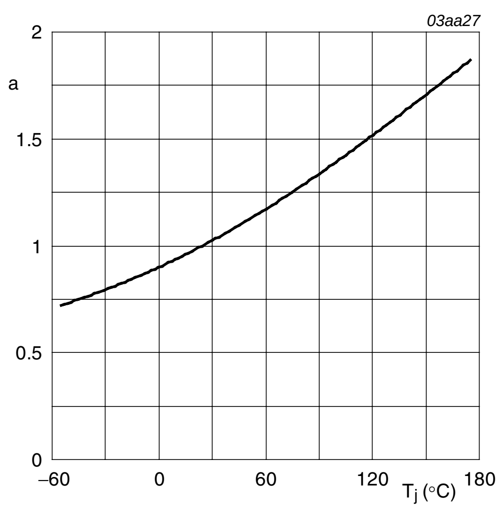
$T_j = 25\,°C; V_{DS} = 5V$

Fig 11. Sub-threshold drain current as a function of gate-source voltage



$I_D = 1mA; V_{DS} = V_{GS}$

Fig 12. Gate-source threshold voltage as a function of junction temperature



$$a = \frac{R_{DSon}}{R_{DSon(25\,°C)}}$$

Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

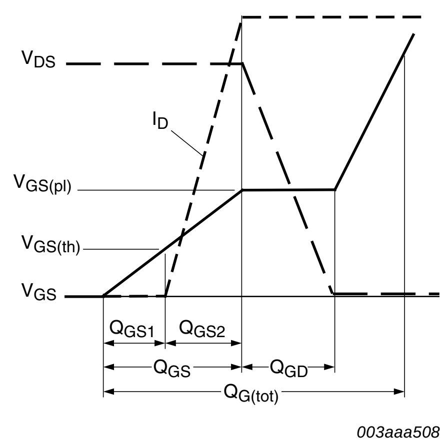
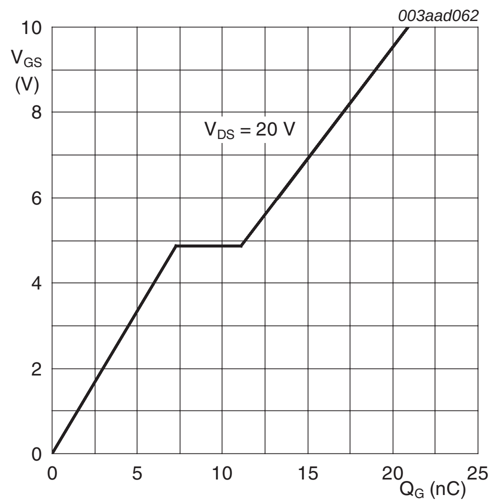
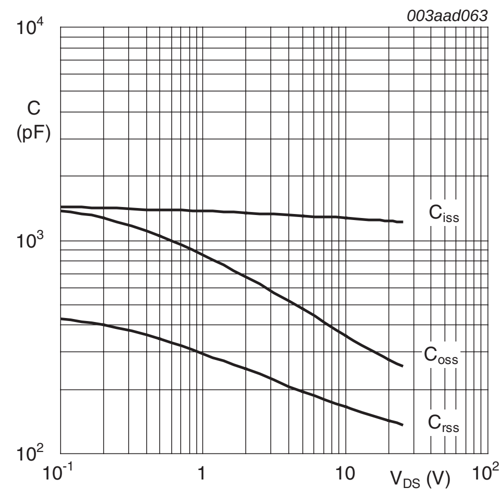


Fig 14. Gate charge waveform definitions



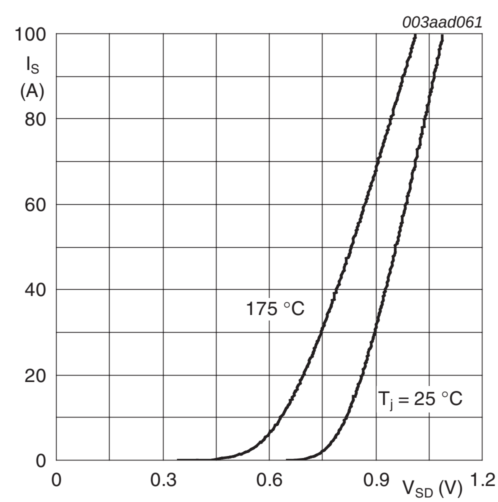
$T_j = 25\,°C; I_D = 25A$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0V; f = 1MHz$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

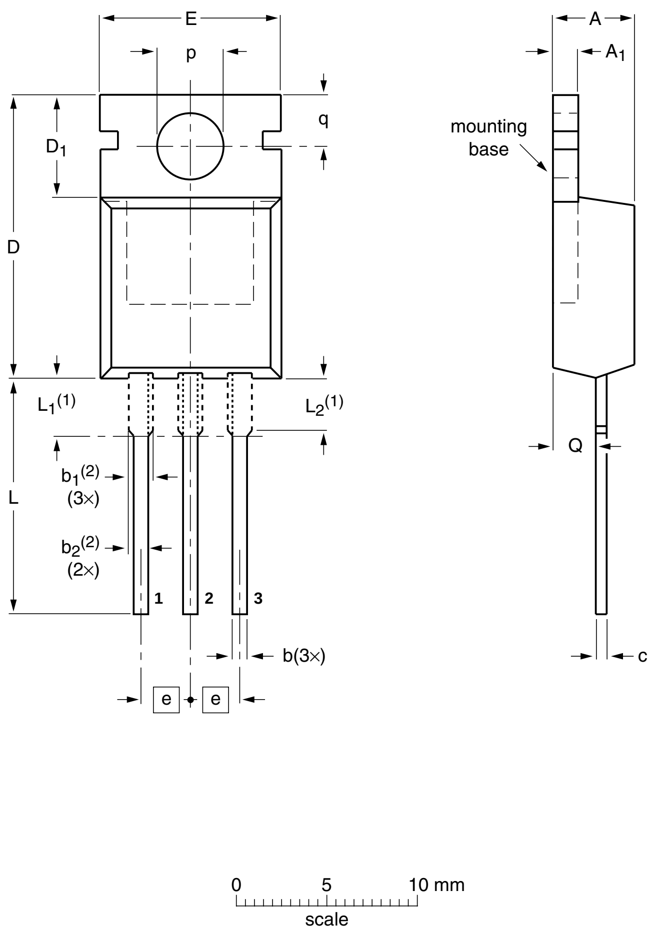


$V_{GS} = 0V$

Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB **SOT78**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	$b_1^{(2)}$	$b_2^{(2)}$	c	D	D_1	E	e	L	$L_1^{(1)}$	$L_2^{(1)}$ max.	p	q	Q
mm	4.7 4.1	1.40 1.25	0.9 0.6	1.6 1.0	1.3 1.0	0.7 0.4	16.0 15.2	6.6 5.9	10.3 9.7	2.54	15.0 12.8	3.30 2.79	3.0	3.8 3.5	3.0 2.7	2.6 2.2

Notes
1. Lead shoulder designs may vary.
2. Dimension includes excess dambar.

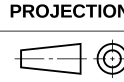
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT78		3-lead TO-220AB	SC-46			~~08-04-23~~ 08-06-13

Fig 18. Package outline SOT78 (TO-220AB)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN8R0-40PS_2	20090625	Product data sheet	-	PSMN8R0-40PS_1
Modifications:	• Status changed from objective to product			
PSMN8R0-40PS_1	20090511	Objective data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status [1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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11. Contents

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