National Semiconductor Corporation

March 1987

IDM29705/29705A 16-Word by 4-Bit Two-Port RAM/Register File

General Description

The IDM29705 and IDM29705A are 16-word by 4-bit RAM/Register File chips housed in a standard 28-pin dual-in-line package. The IDM29705 and the IDM29705A feature TRI-STATE® outputs. These RAMs, which are fabricated using SCL® (Schottky ECL Technology) feature two separate output ports that enable any two 4-bit words to be read from these outputs simultaneously. Each output port contains a four-bit latch. A common Latch Enable (LE) input is used to control all eight latches. The device, which has two Write Enable (WE) inputs, is designed so that either Write Enable (WE_1 or WE_2) and Latch Enable (LE) inputs can be wired together to make the operation of the RAM appear edge-triggered.

The device, which has fully decoded A-address and B-address fields, can address any of the 16 memory words for the A-output port and, simultaneously, select any of the 16 words for presentation at the B-output port. Incoming data is written into the four-bit RAM word selected by the B-address. The D inputs are used to load the new data into the device.

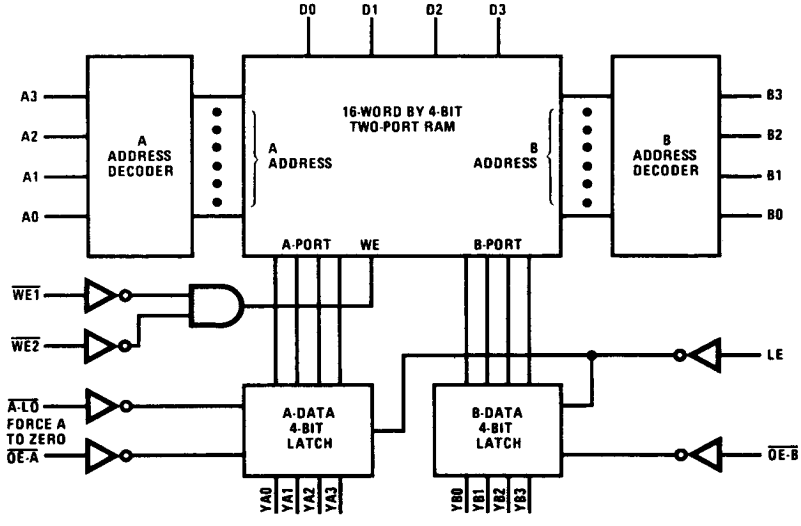
Several of these devices can be cascaded to increase the total number of memory words in the system. When $\overline{OE}$-A is high, the A-output port is in the high-impedance mode. $\overline{OE}$-B, when high, forces the B-output port to the high-impedance state.

The writing of new data into the RAM is controlled by the Write Enable inputs. With both Write Enable inputs low, data is written into the word selected by the B-address field. The memory outputs follow the data inputs during writing if the Latch Enable (LE) is high. With either Write Enable high, no data is written into the RAM.

Features and Benefits

- 16-word by 4-bit, 2-port RAM/Register Files
- Two output ports, each with separate output control
- 4-bit latches on each output port
- Non-inverted data output with respect to data input
- Output enable and write enable inputs provide ease in cascading
- SCL technology (Schottky ECL) provides ECL speeds while keeping low power Schottky input/output voltage and power consumption compatibility
- 100% reliability testing in compliance with MIL-STD-883

IDM29705/29705A Block Diagram



TL/L/9234–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +6.3V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC}max
DC Input Voltage	−0.5V to +5.5V
DC Output Current, into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

Operating Range

P/N	Ambient Temperature	V_{CC}
IDM29705JC	0°C to +70°C	4.75V to 5.25V
IDM29705JM, JM/883	−55°C to +125°C	4.50V to 5.50V
IDM29705AJC, NC	0°C to +70°C	4.75V to 5.25V
IDM29705AJM, JM/883	−55°C to +125°C	4.50V to 5.50V

Standard Screening (conforms to MIL-STD-883 for Class C parts)

Step	MIL-STD-883 Method	Conditions	Level	
			DC, PC	DM, FM
Pre-Seal Visual Inspection	2010	B	100%	100%
Stabilization Bake	1008	C: 24-hour 150°C	100%	100%
Temperature Cycle	1010	C: −65°C to +150°C 10 cycles	100%	100%
Centrifuge	2001	B: 10,000 G	100%	100%
Fine Leak	1014	A: 5×10^{-8} atm-cc/cm^3	100%	100%
Gross Leak	1014	C2: Fluorocarbon	100%	100%
Electrical Test Subgroups 1 and 7 and 9	5004	See below for definitions of subgroups	100%	100%
Insert Additional Screening Here for Class B Parts				
Group A Sample Tests	5005	See below for definitions of subgroups		
Subgroup 1			LTPD = 5	LTPD = 5
Subgroup 2			LTPD = 7	LTPD = 7
Subgroup 3			LTPD = 7	LTPD = 7
Subgroup 7			LTPD = 7	LTPD = 5
Subgroup 8			LTPD = 7	LTPD = 7
Subgroup 9			LTPD = 7	LTPD = 5

Additional Screening for Class B Parts

Step	MIL-STD-883 Method	Conditions	Level
			DMB, FMB
Burn-In	1015	D: 125°C, 160 hours min	100%
Electrical Test	5004		
Subgroup 1			100%
Subgroup 2			100%
Subgroup 3			100%
Subgroup 7			100%
Subgroup 9			100%
Return to Group A Tests in Standard Screening			

Group A Subgroups (as defined in MIL-STD-883, method 5005)

Subgroup	Parameter	Temperature
1	DC	25°C
2	DC	Maximum rated temperature
3	DC	Minimum rated temperature
7	Function	25°C
8	Function	Maximum and minimum rated temperature
9	Switching	25°C
10	Switching	Maximum rated temperature
11	Switching	Minimum rated temperature

2

Electrical Characteristics (over operating temperature range, unless otherwise noted)

Symbol	Parameter	Test Conditions (Note 1)		Min.	Typ (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage (IDM29705 only)	V_{CC} = min, V_{IN} = V_{IH} or V_{IL}	Mil, I_{OH} = −2.0 mA	2.4			Volts
			Com'l, I_{OH} = −4.0 mA				
V_{OL}	Output LOW Voltage	V_{CC} = min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0 mA			0.4	Volts
			I_{OL} = 8.0 mA			0.45	
			I_{OL} = 12 mA			0.5	
			I_{OL} = 16 mA (Note 4)			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = min, I_{IN} = −18 mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = max, V_{IN} = 0.4V	A_i, B_i			−0.25	mA
			Others			−0.36	
I_{IH}	Input HIGH Current	V_{CC} = max, V_{IN} = 2.7V				20	µA
I_I	Input HIGH Current	V_{CC} = max, V_{IN} = 5.5V				0.1	mA
I_{OZ}	Off state (High Impedance) Output Current	V_{CC} = max, V_{IN} = V_{IH} or V_{IL}	V_o = 2.7V			20	µA
			V_o = 0.4V			−20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = max	29705A	−30		−85	mA
			29705	−25		−85	
I_{CC}	Power Supply Current	V_{CC} = max			120	175	mA
		AJC	V_{CC} = 5.25V, T = 70°C			155	mA
		AJM	V_{CC} = 5.5V, T = 125°C			145	mA

Note 1: For conditions shown as Min. or Max., use the appropriate value specified under Electrical Characteristics for the applicable device type.

Note 2: Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.

Note 3: Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Note 4: 29705A commercial temperature range only.

Switching Characteristics (Input Levels = 0V and 3.0V, Transitions measured at 1.5V)

Combinational Delays (In nanoseconds) (C_L = 50 pF)

Parameter	From	To	Conditions	Comm'l Max. (Note 1)		Mil Max. (Note 2)	
				705	705A	705	705A
Access Time	A Address Stable	YA Stable	LE = HIGH	40	30	55	35
	B Address Stable	YB Stable		40	30	55	35
	Both WE LOW	YA = D	LE = HIGH, A = B	45	45	48	45
		YB = D	LE = HIGH	45	45	48	45
Turn-On Time	OE-A or OE-B LOW			25	20	25	25
Turn-Off Time	OE-A or OE-B HIGH	YA or YB Off	C_L = 5 pF (Note 3)	20	20	20	20
Reset Time	A-LO LOW	YA LOW		20	20	30	25
Enable Time	LE HIGH	YA and YB Stable		25	20	25	25
	Data In	YA or YB = D	LE = HIGH, WE both LOW, A = B	45	45	45	45

Switching Characteristics (Continued)

Minimum Setup and Hold Times (in nanoseconds)

Parameter	From	To	Conditions	Comm'l Max. (Note 1)		Mil Max. (Note 2)	
				705	705A	705	705A
Data Setup Time	D Stable	Either WE HIGH		20	15	25	20
Data Hold Time	Either WE HIGH	D Changing		0	0	0	0
Address Setup Time	B Stable	Both WE LOW		3	0	5	3
Address Hold Time	Either WE HIGH	B Changing		0	0	0	0
Latch Close Before Write Begins	LE LOW	WE_1 LOW	WE_2 LOW	0	0	0	0
	LE LOW	WE_2 LOW	WE_1 LOW	0	0	0	0
Address Setup Before Latch Closes	A or B Stable	LE LOW		20	15	40	20
Minimum Pulse Widths (in nanoseconds)							
Write Pulse Width	WE_1	HIGH-LOW-HIGH	WE^2LOW	25	20	25	20
	WE_2	HIGH-LOW-HIGH	WE^1LOW	20	20	20	20
A Latch Reset Pulse	A-LO	HIGH-LOW-HIGH		20	15	20	15
Latch Data Capture	LE	LOW-HIGH-LOW	Address Stable	20	15	20	15

Note 1: T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%.

Note 2: −55°C to +125°C, V_{CC} = 5.0V ± 10%.

Note 3: Measured from 1.5V at the input to 0.5V change in the output level.

Function Tables

Write Control

$\overline{WE}_1$	$\overline{WE}_2$	Function	RAM Outputs at Latch Inputs	
			A-Port	B-Port
L	L	Write D into B	A data (A ≠ B)	D input data
X	H	No write	A data	B data
H	X	No write	A data	B data

YA Read

Inputs			YA Outputs	Function
$\overline{OE}$-A	$\overline{A}$-LO	LE		
H	X	X	Z	High impedance
L	L	X	L	Force YA LOW
L	H	H	A-Port RAM data	Latches transparent
L	H	L	NC	Latches retain data

Function Tables (Continued)

YB Read

Inputs		YB Output	Function
$\overline{OE}$-B	LE		
H	X	Z	High impedance
L	H	B-Port RAM data	Latches transparent
L	L	NC	Latches retain data

H = HIGH Z = High impedance
L = LOW NC = No change
X = Don't care

Pinout Descriptions of the IDM29705/29705A

D_3-D_0: Through these inputs new data can be written in the location specified by the B-address inputs.

A_3-A_0: The 4-bit address presented at the A inputs selects one of the 16 memory words for presentation at the A-data latch outputs.

B_3-B_0: The 4-bit address presented at the B inputs selects one of the 16 memory words for presentation at the B-data latch outputs. This address also selects the location into which data is written.

YA_3-YA_0: The four A-data latch outputs.

YB_3-YB_0: The four B-data latch outputs.

$\overline{WE}_1$, $\overline{WE}_2$: Write enable inputs. When both are low, enables data to be written into the RAM location selected by the B-address field. When either Write Enable input is high, no data can be written into memory.

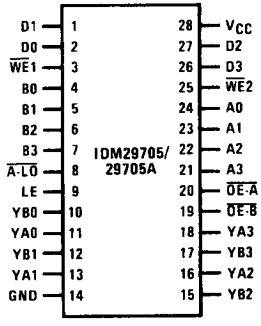
$\overline{OE}$-A: A-port output enable. When low, data in the A-data latch is present at the YA_i outputs. When high, the YA_i outputs are in the high-impedance mode.

$\overline{OE}$-B: B-port output enable. When low, data in the B-data latch is presented at the YB_i outputs. When high, the YB_i outputs are in the high-impedance mode.

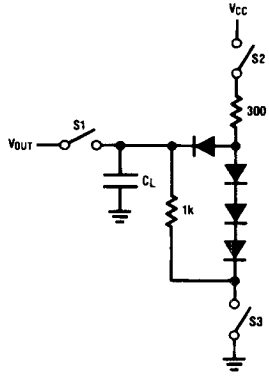
LE: Latch enable. The LE input acts as control for both the RAM-A and RAM-B output ports. When high the latches are transparent and data from the RAM, as selected by the A and B address inputs, is presented at the outputs. When low, the latches retain the last data read from the RAM regardless of the current A and B address inputs.

$\overline{A\text{-}LO}$: Force A to zero. This input operates to force the A-port latch outputs low independent of the LE input or A address inputs. The A-output bus can be forced low using this control input. With $\overline{A\text{-}LO}$ high, the A latches operate in their normal manner. Once forced low, the A latches remain low independent of the $\overline{A\text{-}LO}$ input if the Latch Enable (LE) is low.

IDM29705/29705A Connection Diagram and Test Load



TL/L/9234–2



TL/L/9234–3

Note 1: C_L = 50 pF includes scope probe, wiring and stray capacitances without device in test fixture.

Note 2: S1, S2, S3 are closed during function tests and all AC tests except output enable tests.

Note 3: S1 and S3 are closed while S2 is open for t_{PZH} test. S1 and S2 are closed while S3 is open for t_{PZL} test.

Note 4: C_L = 5 pF for output disable tests.