

16 Megabit (2M x8-Bit) Multi-Purpose Flash

SST39VF016Q



Advance Information

FEATURES:

- **Organized as 2M x8**
- **Single 2.7-3.6V Read and Write Operations**
- **V_{DDQ} Power Supply to Support 5V I/O**
- **Superior Reliability**
 - Endurance: 100,000 Cycles (typical)
 - Greater than 100 years Data Retention
- **Low Power Consumption:**
 - Active Current: 15 mA (typical)
 - Standby Current: 4 μ A (typical)
 - Auto Low Power Mode: 4 μ A (typical)
- **Small Sector-Erase Capability (512 sectors)**
 - Uniform 4 KByte sectors
- **Block-Erase Capability (32 blocks)**
 - Uniform 64 KByte blocks
- **Fast Read Access Time:**
 - 70 and 90 ns
- **Latched Address and Data**
- **Fast Sector-Erase and Byte-Program:**
 - Sector-Erase Time: 18 ms (typical)
 - Block-Erase Time: 18 ms (typical)
 - Chip-Erase Time: 70 ms (typical)
 - Byte-Program Time: 14 μ s (typical)
 - Chip Rewrite Time: 30 seconds (typical)
- **Automatic Write Timing**
 - Internal V_{PP} Generation
- **End of Write Detection**
 - Toggle Bit
 - Data# Polling
- **CMOS I/O Compatibility**
- **JEDEC Standard**
 - Flash EEPROM Pinouts and command sets
- **Packages Available**
 - 40-Pin TSOP (10mm x 20mm)

PRODUCT DESCRIPTION

The SST39VF016Q device is a 2M x8 CMOS Multi-Purpose Flash (MPF) manufactured with SST's proprietary, high performance CMOS SuperFlash technology. The split-gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST39VF016Q writes (Program or Erase) with a 2.7-3.6V power supply. The SST39VF016Q conforms to JEDEC standard pinouts for x8 memories.

Featuring high performance Byte-Program, the SST39VF016Q device provides a typical Byte-Program time of 14 μ sec. The entire memory can typically be erased and programmed byte-by-byte in 30 seconds, when using interface features such as Toggle Bit or Data# Polling to indicate the completion of Program operation. To protect against inadvertent write, the SST39VF016Q has on-chip hardware and Software Data Protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, the SST39VF016Q is offered with a guaranteed endurance of 10,000 cycles. Data retention is rated at greater than 100 years.

The SST39VF016Q device is suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, the SST39VF016Q significantly improves performance and reliability, while lowering power consumption. The SST39VF016Q inherently uses less energy

during Erase and Program than alternative flash technologies. The total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash technologies. The SST39VF016Q also improves flexibility while lowering the cost for program, data, and configuration storage applications.

The SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles.

To meet high density, surface mount requirements, the SST39VF016Q is offered in a 40-pin TSOP package. See Figure 1 for pinout.

Device Operation

Commands are used to initiate the memory operation functions of the device. Commands are written to the device using standard microprocessor write sequences. A command is written by asserting WE# low while keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.



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The SST39VF016Q also has the **Auto Low Power** mode which puts the device in a near standby mode after data has been accessed with a valid Read operation. This reduces the I_{DD} active read current from typically 15 mA to typically 4 μ A. The Auto Low Power mode reduces the typical I_{DD} active read current to the range of 1 mA/MHz of read cycle time. The device exits the Auto Low Power mode with any address transition or control signal transition used to initiate another Read cycle, with no access time penalty.

Read

The Read operation of the SST39VF016Q is controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the Read cycle timing diagram for further details (Figure 2).

Byte-Program Operation

The SST39VF016Q is programmed on a byte-by-byte basis. The Program operation consists of three steps. The first step is the three-byte load sequence for Software Data Protection. The second step is to load byte address and byte data. During the Byte-Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last. The data is latched on the rising edge of either CE# or WE#, whichever occurs first. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or CE#, whichever occurs first. The Program operation, once initiated, will be completed within 20 μ s. See Figures 3 and 4 for WE# and CE# controlled Program operation timing diagrams and Figure 15 for flowcharts. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands issued during the internal Program operation are ignored.

Sector/Block-Erase Operation

The Sector/Block-Erase operation allows the system to erase the device on a sector-by-sector (or block-by-block) basis. The SST39VF016Q offers both small Sector-Erase and large Block-Erase mode. The sector architecture is based on uniform sector size of 4 KByte. The Block-Erase mode is based on uniform block size of 64 KByte. The Sector-Erase operation is initiated by executing a six-byte-command sequence with Sector-Erase command (30H) and sector address (SA) in the last bus cycle. The address lines A12-A20 are used to determine the sector address. The Block-Erase operation is initiated by executing a six-byte-command sequence with Block-Erase command (50H) and block address (BA) in the last bus cycle. The

address lines A16-A20 are used to determine the block address. The sector or block address is latched on the falling edge of the sixth WE# pulse, while the command (30H or 50H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The end of Erase operation can be determined using either Data# Polling or Toggle Bit methods. See Figures 8 and 9 for timing waveforms. Any commands issued during the Sector or Block-Erase operation are ignored.

Chip-Erase Operation

The SST39VF016Q provides a Chip-Erase operation, which allows the user to erase the entire memory array to the "1" state. This is useful when the entire device must be quickly erased.

The Chip-Erase operation is initiated by executing a six byte command sequence with Chip-Erase command (10H) at address 5555H in the last byte sequence. The Erase operation begins with the rising edge of the sixth WE# or CE#, whichever occurs first. During the Erase operation, the only valid read is Toggle Bit or Data# Polling. See Table 4 for the command sequence, Figure 7 for timing diagram, and Figure 18 for the flowchart. Any commands issued during the Chip-Erase operation are ignored.

Write Operation Status Detection

The SST39VF016Q provides two software means to detect the completion of a write (Program or Erase) cycle, in order to optimize the system Write cycle time. The software detection includes two status bits: Data# Polling (DQ7) and Toggle Bit (DQ6). The end of write detection mode is enabled after the rising edge of WE#, which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ7 or DQ6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

Data# Polling (DQ7)

When the SST39VF016Q is in the internal Program operation, any attempt to read DQ7 will produce the complement of the true data. Once the Program operation is completed, DQ7 will produce true data. The device is then ready for the next operation. During internal Erase operation, any attempt to read DQ7 will produce a '0'. Once the internal Erase



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operation is completed, DQ7 will produce a '1'. The Data# Polling is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector, Block or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 5 for Data# Polling timing diagram and Figure 16 for a flowchart.

Toggle Bit (DQ6)

During the internal Program or Erase operation, any consecutive attempts to read DQ6 will produce alternating 1's and 0's, i.e., toggling between 1 and 0. When the internal Program or Erase operation is completed, the DQ6 bit will stop toggling. The device is then ready for the next operation. The Toggle Bit is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector, Block or Chip-Erase, the Toggle Bit is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 6 for Toggle Bit timing diagram and Figure 16 for a flowchart.

Data Protection

The SST39VF016Q provides both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a Write cycle.

V_{DD} Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)

The SST39VF016Q provides the JEDEC approved Software Data Protection scheme for all data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of the three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six-byte sequence. The SST39VF016Q device is shipped with the Software Data Protection permanently enabled. See Table 4 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to read mode within T_{RC}.

Common Flash Memory Interface (CFI)

The SST39VF016Q also contains the CFI information to describe the characteristics of the device. In order to enter the CFI Query mode, the system must write three-byte sequence, same as product ID entry command with 98H

(CFI Query command) to address 5555H in the last byte sequence. Once the device enters the CFI Query mode, the system can read CFI data at the addresses given in tables 5 through 7. The system must write the CFI Exit command to return to Read mode from the CFI Query mode.

Product Identification

The Product Identification mode identifies the device as the SST39VF016Q and manufacturer as SST. This mode may be accessed by hardware or software operations. The hardware operation is typically used by a programmer to identify the correct algorithm for the SST39VF016Q. Users may wish to use the Software Product Identification operation to identify the part (i.e., using the device code) when using multiple manufacturers in the same socket. For details, see Table 3 for hardware operation or Table 4 for software operation, Figure 10 for the Software ID Entry and Read timing diagram and Figure 17 for the ID Entry command sequence flowchart.

Product Identification Mode Exit/CFI Mode Exit

TABLE 1: PRODUCT IDENTIFICATION TABLE

	Address	Data
Manufacturer's Code	0000H	BFH
Device Code	0001H	D9H

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In order to return to the standard Read mode, the Software Product Identification mode must be exited. Exit is accomplished by issuing the Software ID Exit command sequence, which returns the device to the Read operation. This command may also be used to reset the device to the Read mode after any inadvertent transient condition that apparently causes the device to behave abnormally, e.g., not read correctly. Please note that the Software ID Exit/CFI Exit command is ignored during an internal Program or Erase operation. See Table 4 for software command codes, Figure 12 for timing waveform and Figure 17 for a flowchart.

V_{DDQ} - I/O Power Supply

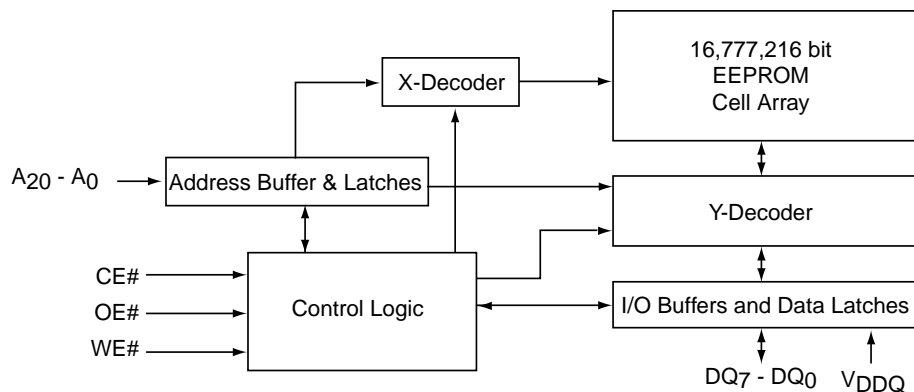
This pin functions as power supply pin for input/output buffers. It should be tied to V_{DD} (2.7 - 3.6V) in a 3.0V-only system. It should be tied to a 5.0V±10% (4.5 - 5.5V) power supply in a mixed voltage system environment where flash memory has to be interfaced with 5V system chips.



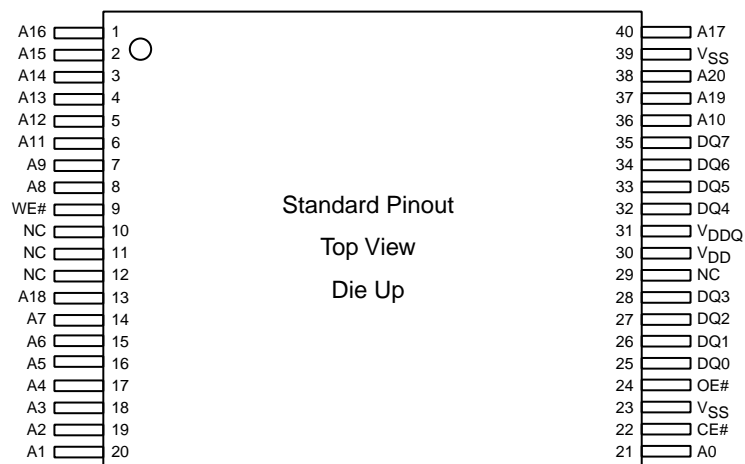
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FUNCTIONAL BLOCK DIAGRAM



333 ILL B1.2



333 ILL F01.1

FIGURE 1: PIN ASSIGNMENTS FOR 40-PIN TSOP PACKAGES



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TABLE 2: PIN DESCRIPTION

Symbol	Pin Name	Functions
A ₂₀ -A ₀	Address Inputs	To provide memory addresses. During Sector-Erase A ₂₀ -A ₁₂ address lines will select the sector. During Block-Erase A ₂₀ -A ₁₆ address lines will select the block.
DQ ₇ -DQ ₀	Data Input/output	To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	To activate the device when CE# is low.
OE#	Output Enable	To gate the data output buffers.
WE#	Write Enable	To control the Write operations.
V _{DD}	Power Supply	To provide 3-volt supply (2.7-3.6V)
V _{DDQ}	I/O Power Supply	Supplies power for input/output buffers. It should be either tied to V _{DD} (2.7 - 3.6V) for 3V I/O or to a 5.0V (4.5 - 5.5V) power supply to support 5V I/O.
V _{SS}	Ground	
NC	No Connection	Unconnected pins.

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TABLE 3: OPERATION MODES SELECTION

Mode	CE#	OE#	WE#	A ₉	DQ	Address
Read	V _{IL}	V _{IL}	V _{IH}	A _{IN}	D _{OUT}	A _{IN}
Program	V _{IL}	V _{IH}	V _{IL}	A _{IN}	D _{IN}	A _{IN}
Erase	V _{IL}	V _{IH}	V _{IL}	X	X	Sector or block address, XXh for Chip-Erase
Standby	V _{IH}	X	X	X	High Z	X
Write Inhibit	X	V _{IL}	X	X	High Z/ D _{OUT}	X
	X	X	V _{IH}	X	High Z/ D _{OUT}	X
Product Identification						
Hardware Mode	V _{IL}	V _{IL}	V _{IH}	V _H	Manufacturer Code (BF) Device Code (D9)	A ₂₀ - A ₁ = V _{IL} , A ₀ = V _{IL} A ₂₀ - A ₁ = V _{IL} , A ₀ = V _{IH} See Table 4
Software Mode	V _{IL}	V _{IL}	V _{IH}	A _{IN}		

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TABLE 4: SOFTWARE COMMAND SEQUENCE

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr ⁽¹⁾	Data	Addr ⁽¹⁾	Data	Addr ⁽¹⁾	Data	Addr ⁽¹⁾	Data	Addr ⁽¹⁾	Data	Addr ⁽¹⁾	Data
Byte-Program	5555H	AAH	2AAAH	55H	5555H	A0H	WA ⁽³⁾	Data				
Sector-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA _x ⁽²⁾	30H
Block-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	BA _x ⁽²⁾	50H
Chip-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry	5555H	AAH	2AAAH	55H	5555H	90H						
CFI Query Entry	5555H	AAH	2AAAH	55H	5555H	98H						
Software ID Exit/ CFI Exit	XXH	F0H										
Software ID Exit/ CFI Exit	5555H	AAH	2AAAH	55H	5555H	F0H						

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- Notes:**
- (1) Address format A₁₄-A₀ (Hex), Addresses A₁₅, A₁₆, A₁₇, A₁₈, A₁₉ and A₂₀ are "Don't Care" for Command sequence.
 - (2) SA_x for Sector-Erase; uses A₂₀-A₁₂ address lines
BA_x, for Block-Erase; uses A₂₀-A₁₆ address lines
 - (3) WA = Program byte address
 - (4) Both Software ID Exit operations are equivalent

Notes for Software ID Entry Command Sequence

1. With A₂₀-A₁=0; SST Manufacturer Code = BFH, is read with A₀ = 0,
SST39VF016Q Device Code = D9H, is read with A₀ = 1.
2. The device does not remain in Software Product ID Mode if powered down.

TABLE 5: CFI QUERY IDENTIFICATION STRING¹

Address	Data	Data
10H 11H 12H	51H 52H 59H	Query Unique ASCII string "QRY"
13H 14H	01H 07H	Primary OEM command set
15H 16H	00H 00H	Address for Primary Extended Table
17H 18H	00H 00H	Alternate OEM command set (00H = none exists)
19H 1AH	00H 00H	Address for Alternate OEM extended Table (00H = none exists)

Note 1: Refer to CFI publication 100 for more details.

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TABLE 6: SYSTEM INTERFACE INFORMATION

Address	Data	Data
1BH	27H	V _{DD} Min. (Program/Erase) DQ7-DQ4: Volts, DQ3-DQ0: 100 millivolts
1CH	36H	V _{DD} Max. (Program/Erase) DQ7-DQ4: Volts, DQ3-DQ0: 100 millivolts
1DH	00H	V _{PP} min. (00H = no V _{PP} pin)
1EH	00H	V _{PP} max. (00H = no V _{PP} pin)
1FH	04H	Typical time out for Byte-Program 2 ^N μs (2 ⁴ = 16 μs)
20H	00H	Typical time out for min. size buffer program 2 ^N μs (00H = not supported)
21H	04H	Typical time out for individual Sector/Block-Erase 2 ^N ms (2 ⁴ = 16 ms)
22H	06H	Typical time out for Chip-Erase 2 ^N ms (2 ⁶ = 64 ms)
23H	01H	Maximum time out for Byte-Program 2 ^N times typical (2 ¹ x 2 ⁴ = 32 μs)
24H	00H	Maximum time out for buffer program 2 ^N times typical
25H	01H	Maximum time out for individual Sector/Block-Erase 2 ^N times typical (2 ¹ x 2 ⁴ = 32 ms)
26H	01H	Maximum time out for Chip-Erase 2 ^N times typical (2 ¹ x 2 ⁶ = 128 ms)

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TABLE 7: DEVICE GEOMETRY INFORMATION

Address	Data	Data
27H	15H	Device size = 2 ^N Byte (15H = 21; 2 ²¹ = 2M Bytes)
28H 29H	00H 00H	Flash Device Interface description; 0000H = x8-only asynchronous interface
2AH 2BH	00H 00H	Maximum number of byte in multi-byte write = 2 ^N (00H = not supported)
2CH	02H	Number of Erase Sector/Block sizes supported by device
2DH 2EH 2FH 30H	FFH 01H 10H 00H	Sector Information (y + 1 = Number of sectors; z x 256B = sector size) y = 511 + 1 = 512 sectors (01FF = 511) z = 16 x 256 Bytes = 4 KBytes/sector (0010H = 16)
31H 32H 33H 34H	1FH 00H 00H 01H	Block Information (y + 1 = Number of blocks; z x 256B = block size) y = 31 + 1 = 32 blocks (001F = 31) z = 256 x 256 Bytes = 64 KBytes/block (0100H = 256)

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Absolute Maximum Stress Ratings (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias -55°C to +125°C
Storage Temperature -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential -0.5V to $V_{DDQ} + 0.5V$
Transient Voltage (<20 ns) on Any Pin to Ground Potential -1.0V to $V_{DDQ} + 1.0V$
Voltage on A₉ Pin to Ground Potential -0.5V to 13.2V
Package Power Dissipation Capability ($T_a = 25^\circ\text{C}$) 1.0W
Surface Mount Lead Soldering Temperature (3 Seconds) 240°C
Output Short Circuit Current⁽¹⁾ 50 mA

Note: ⁽¹⁾ Outputs shorted for no more than one second. No more than one output shorted at a time.

OPERATING RANGE

Range	Ambient Temp	V_{DD}	V_{DDQ}
Commercial	0 °C to +70 °C	2.7 - 3.6V	V_{DD} or 4.5 - 5.5V
Industrial	-40 °C to +85 °C	2.7 - 3.6V	V_{DD} or 4.5 - 5.5V

AC CONDITIONS OF TEST

Input Rise/Fall Time 10 ns
Output Load $C_L = 100 \text{ pF}$
See Figures 13 and 14



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TABLE 8: DC OPERATING CHARACTERISTICS $V_{DD} = 2.7-3.6V$ AND $V_{DDQ} = V_{DD}$ OR $4.5 - 5.5V$

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DD}	Power Supply Current Read Program and Erase		20 25	mA mA	CE#=OE#=V _{IL} , WE#=V _{IH} , all I/Os open, Address input = V _{IL} /V _{IH} , at f=1/T _{RC} Min. CE#=WE#=V _{IL} , OE#=V _{IH} , V _{DD} =V _{DD} Max.
I_{SB}	Standby V _{DD} Current		20	μA	CE#=V _{IHC} , V _{DD} = V _{DD} Max.
I_{ALP}	Auto Low Power Current		20	μA	CE#=V _{ILC} , V _{DD} = V _{DD} Max. All inputs = V _{IHC} or V _{ILC} WE# = V _{IHC}
I_{LI}	Input Leakage Current		1	μA	V _{IN} =GND to V _{DD} , V _{DD} = V _{DD} Max.
I_{LO}	Output Leakage Current		1	μA	V _{OUT} =GND to V _{DD} , V _{DD} = V _{DD} Max.
V _{IL}	Input Low Voltage	2.0 V _{DD} -0.3	0.8	V	V _{DD} = V _{DD} Min.
V _{ILC}	Input Low Voltage (CMOS)		0.3	V	V _{DD} = V _{DD} Max.
V _{IH}	Input High Voltage			V	V _{DD} = V _{DD} Max.
V _{IHC}	Input High Voltage (CMOS)			V	V _{DD} = V _{DD} Max.
V _{OL}	Output Low Voltage		0.4	V	I _{OL} = 100 μA, V _{DD} = V _{DD} Min.
V _{OH}	Output High Voltage	2.4		V	I _{OH} = -100 μA, V _{DD} = V _{DD} Min.
V _H	Supervoltage for A ₉ pin	11.4	12.6	V	CE# = OE# =V _{IL} , WE# = V _{IH}
I _H	Supervoltage Current for A ₉ pin		200	μA	CE# = OE# = V _{IL} , WE# = V _{IH} , A ₉ = V _H Max.

333PGMT9.5

TABLE 9: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
T _{PU-READ} ⁽¹⁾	Power-up to Read Operation	100	μs
T _{PU-WRITE} ⁽¹⁾	Power-up to Program/Erase Operation	100	μs

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TABLE 10: CAPACITANCE (Ta = 25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
C _{I/O} ⁽¹⁾	I/O Pin Capacitance	V _{I/O} = 0V	12 pF
C _{IN} ⁽¹⁾	Input Capacitance	V _{IN} = 0V	6 pF

Note: (1) This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

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TABLE 11: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N _{END} ⁽¹⁾	Endurance	10,000	Cycles	JEDEC Standard A117
T _{DR} ⁽¹⁾	Data Retention	100	Years	JEDEC Standard A103
V _{ZAP_HBM} ⁽¹⁾	ESD Susceptibility Human Body Model	2000	Volts	JEDEC Standard A114
V _{ZAP_MM} ⁽¹⁾	ESD Susceptibility Machine Model	200	Volts	JEDEC Standard A115
I _{LTH} ⁽¹⁾	Latch Up	100 + I _{DD}	mA	JEDEC Standard 78

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Note: (1) This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.



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AC CHARACTERISTICS

TABLE 12: READ CYCLE TIMING PARAMETERS $V_{DD} = 2.7-3.6V$

Symbol	Parameter	SST39VF016Q-70		SST39VF016Q-90		Units
		Min	Max	Min	Max	
T_{RC}	Read Cycle Time	70		90		ns
T_{CE}	Chip Enable Access Time		70		90	ns
T_{AA}	Address Access Time		70		90	ns
T_{OE}	Output Enable Access Time		35		45	ns
$T_{CLZ}^{(1)}$	CE# Low to Active Output	0		0		ns
$T_{OLZ}^{(1)}$	OE# Low to Active Output	0		0		ns
$T_{CHZ}^{(1)}$	CE# High to High-Z Output		20		30	ns
$T_{OHZ}^{(1)}$	OE# High to High-Z Output		20		30	ns
$T_{OH}^{(1)}$	Output Hold from Address Change	0		0		ns

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TABLE 13: PROGRAM/ERASE CYCLE TIMING PARAMETERS

Symbol	Parameter	Min	Max	Units
T_{BP}	Byte-Program Time		20	μs
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	30		ns
T_{CS}	WE# and CE# Setup Time	0		ns
T_{CH}	WE# and CE# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	10		ns
T_{CP}	CE# Pulse Width	40		ns
T_{WP}	WE# Pulse Width	40		ns
$T_{WPH}^{(1)}$	WE# Pulse Width High	30		ns
$T_{CPH}^{(1)}$	CE# Pulse Width High	30		ns
T_{DS}	Data Setup Time	30		ns
$T_{DH}^{(1)}$	Data Hold Time	0		ns
$T_{IDA}^{(1)}$	Software ID Access and Exit Time		150	ns
T_{SE}	Sector-Erase		25	ms
T_{BE}	Block-Erase		25	ms
T_{SCE}	Chip-Erase		100	ms

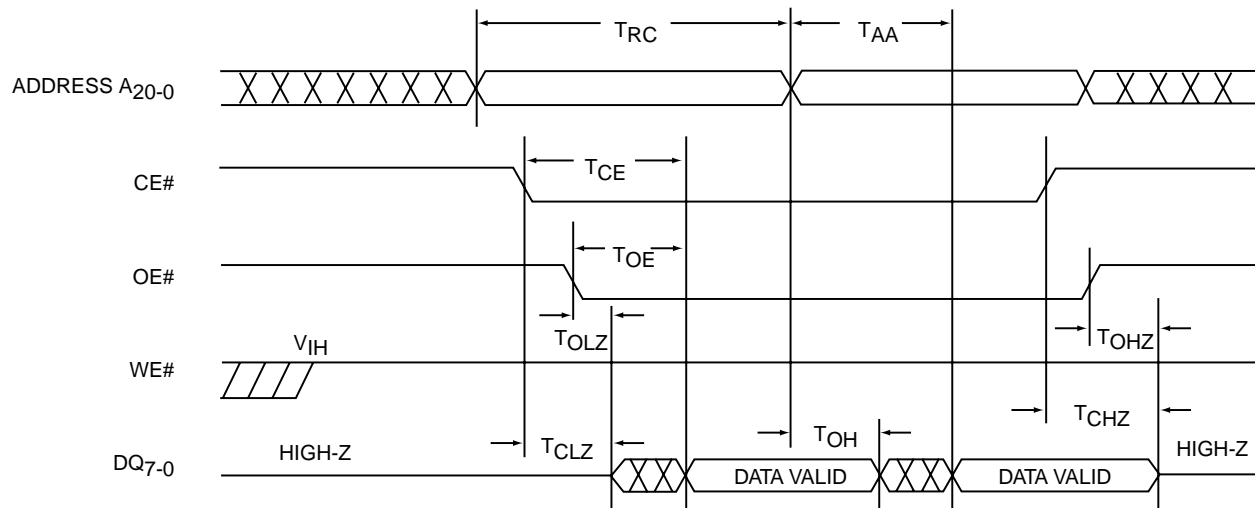
333 PGM T14.2

Note: (1) This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.



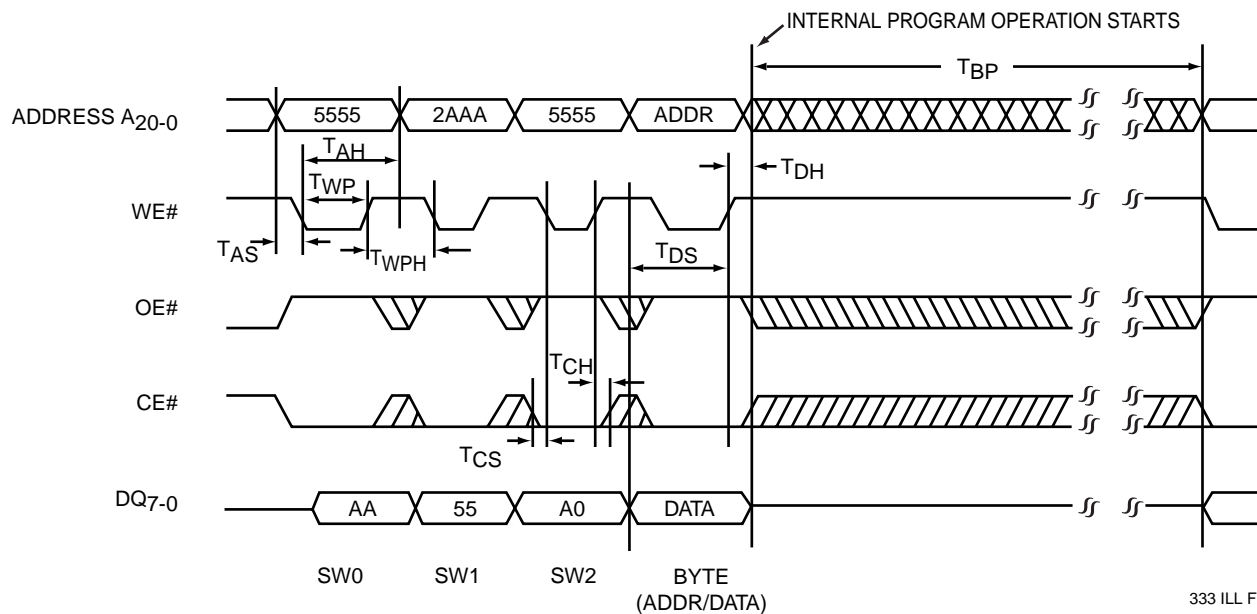
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333 ILL F02.0

FIGURE 2: READ CYCLE TIMING DIAGRAM



333 ILL F03.0

FIGURE 3: WE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM



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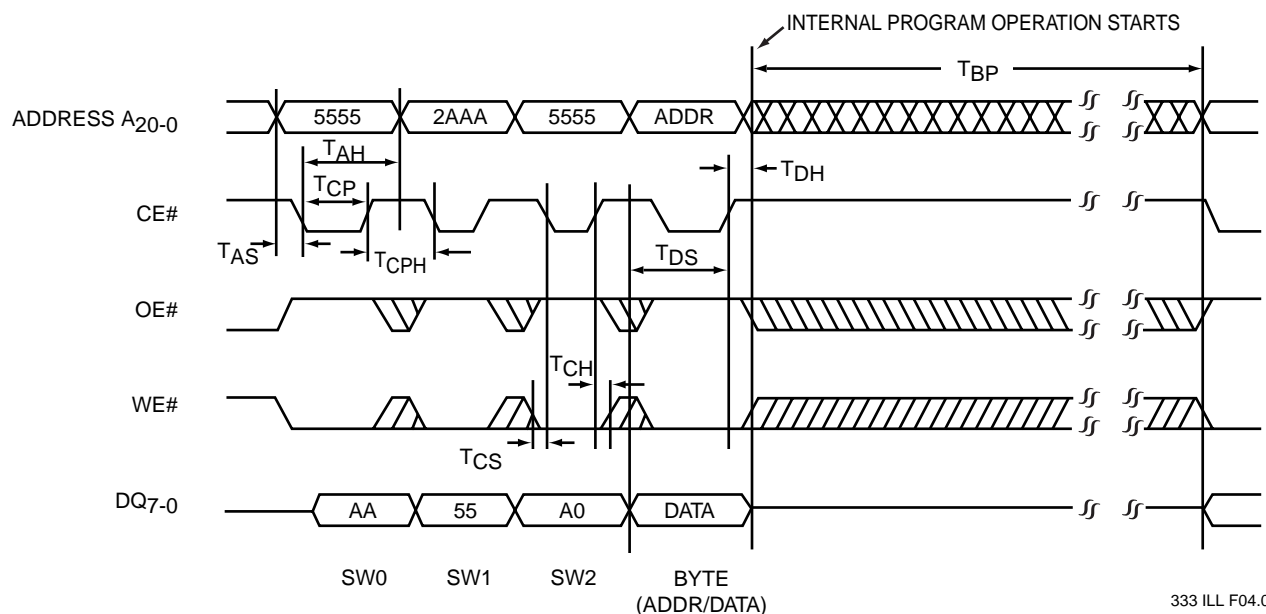


FIGURE 4: CE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM

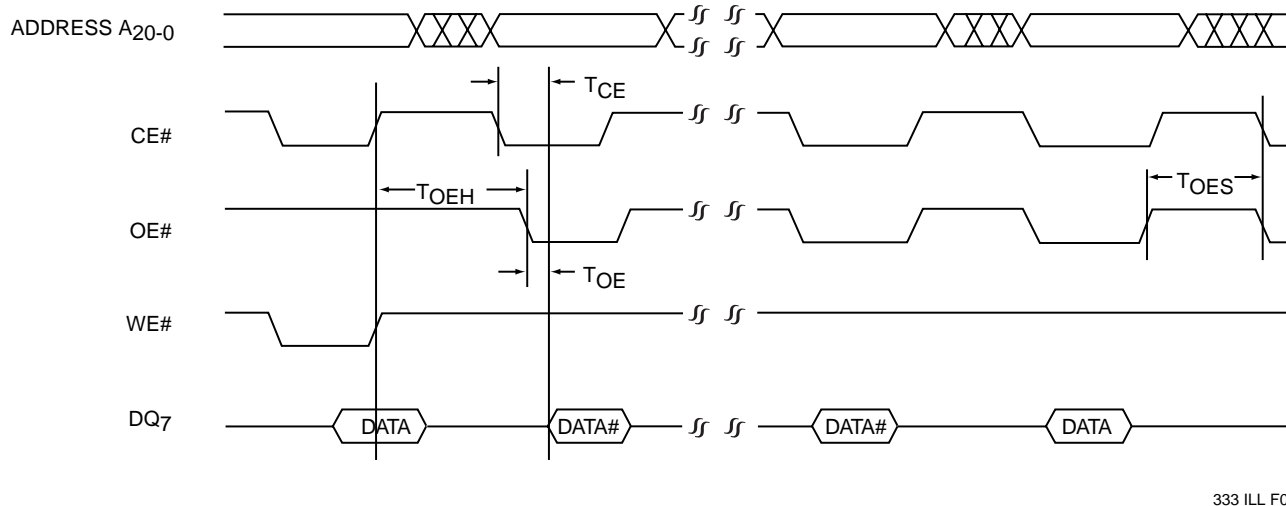


FIGURE 5: DATA# POLLING TIMING DIAGRAM



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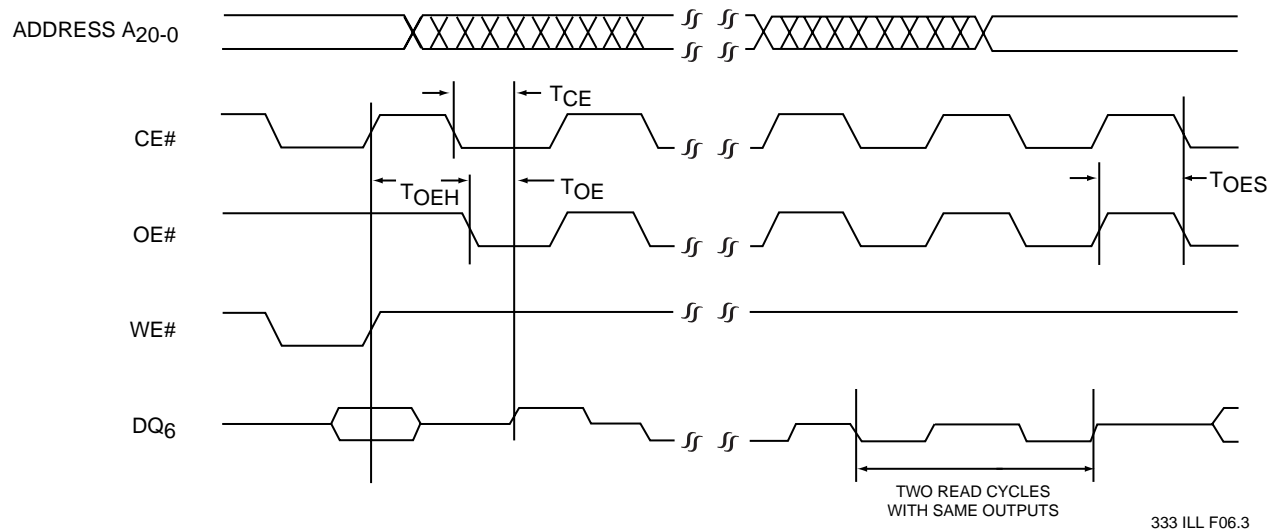
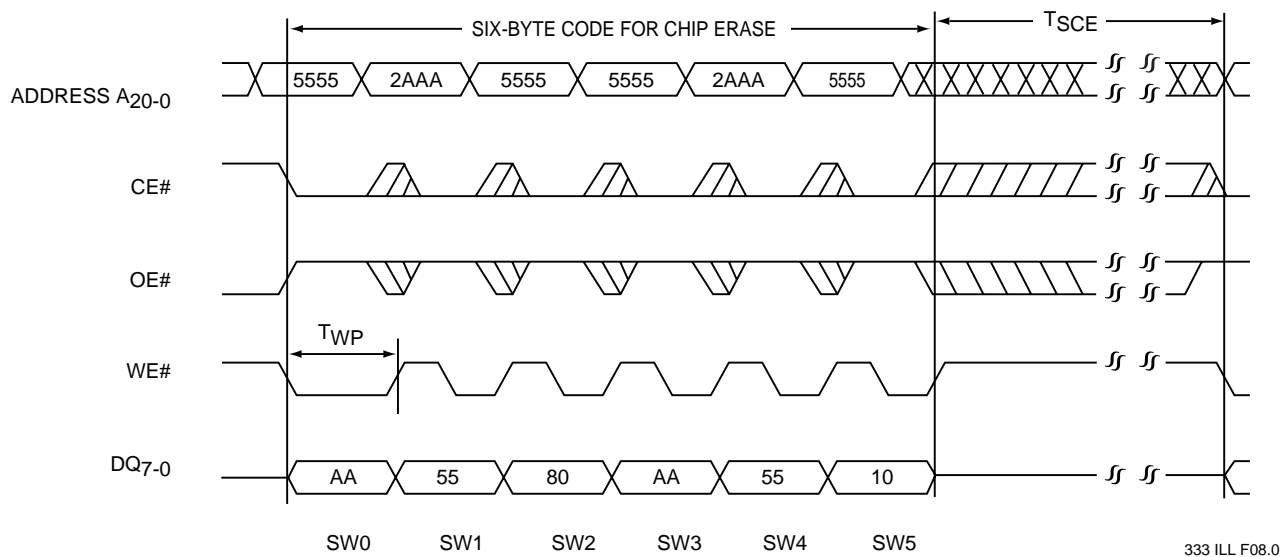


FIGURE 6: TOGGLE BIT TIMING DIAGRAM



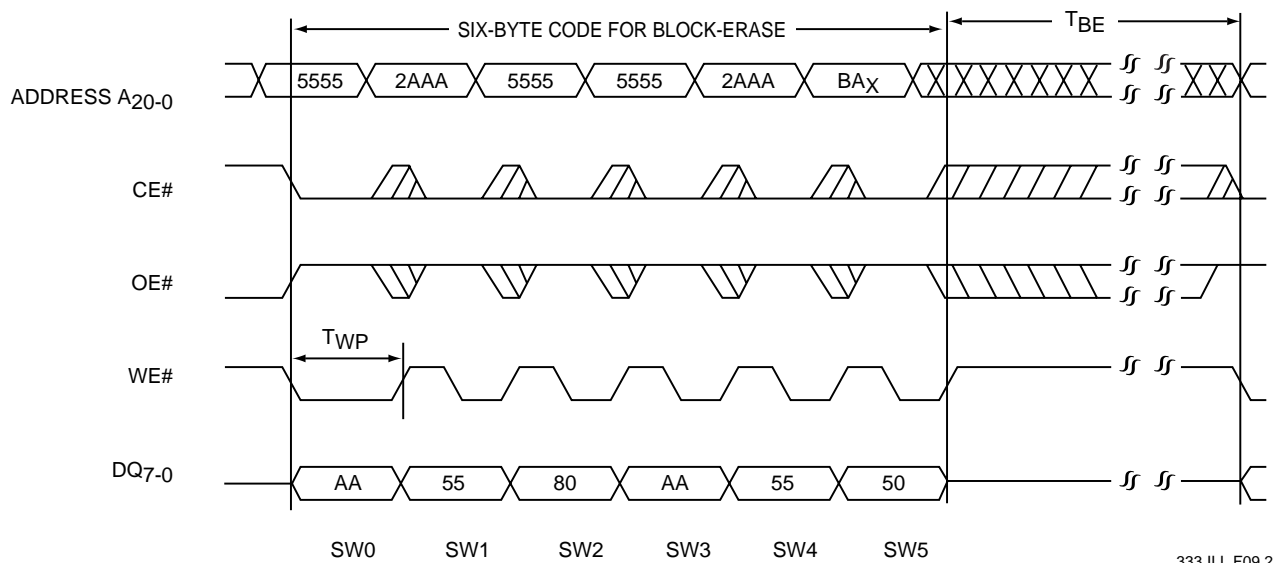
Note: The device also supports CE# controlled Chip-Erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met. (See Table 13)

FIGURE 7: WE# CONTROLLED CHIP-ERASE TIMING DIAGRAM



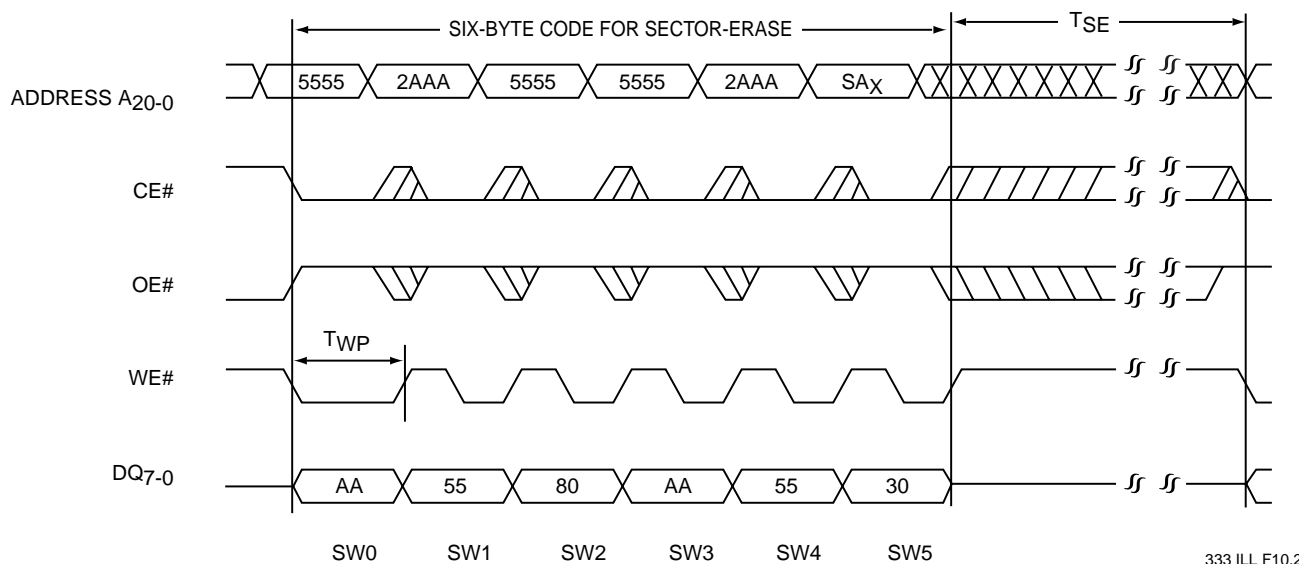
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Note: The device also supports CE# controlled Block-Erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met. (See Table 13)
BA_x = Block Address

FIGURE 8: WE# CONTROLLED BLOCK-ERASE TIMING DIAGRAM



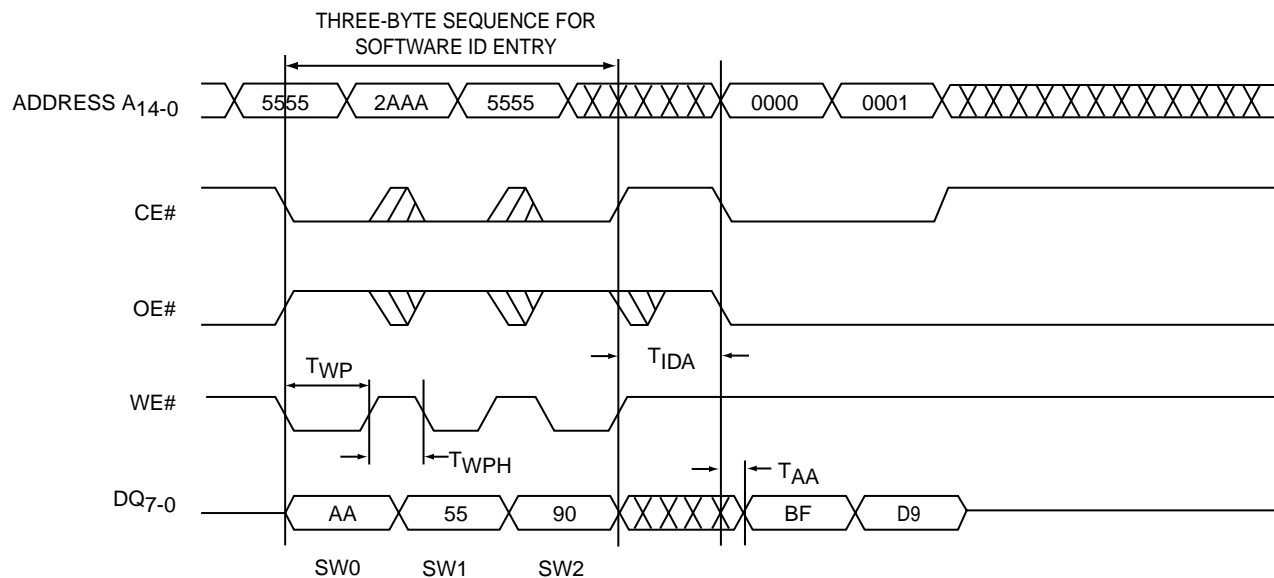
Note: The device also supports CE# controlled Sector-Erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met. (See Table 13)
SA_x = Sector Address

FIGURE 9: WE# CONTROLLED SECTOR-ERASE TIMING DIAGRAM



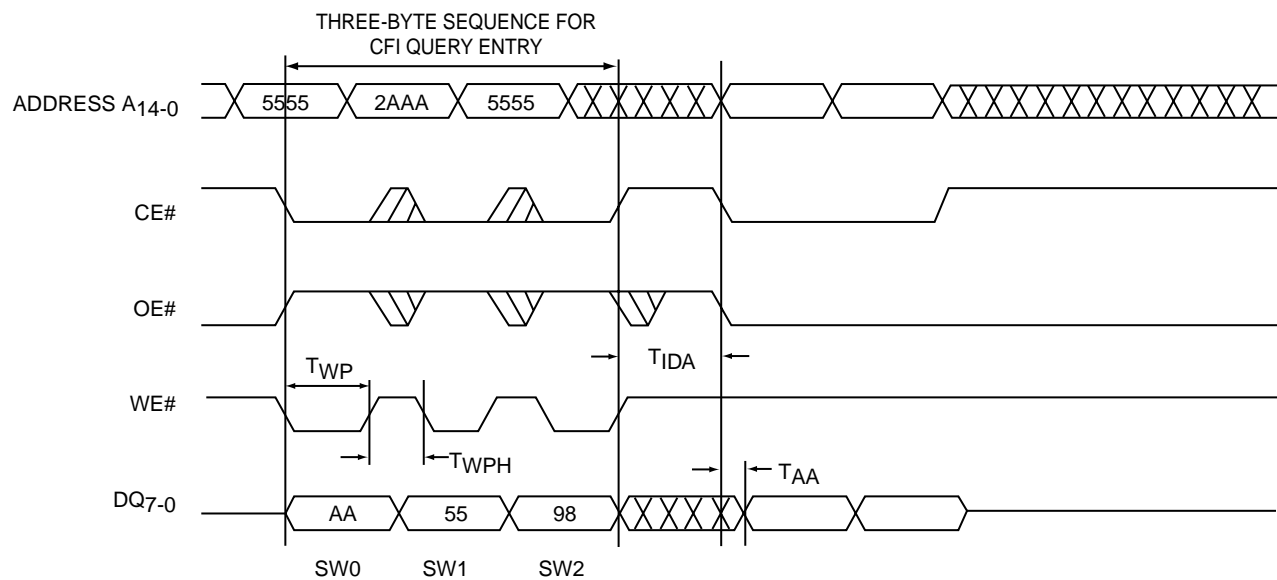
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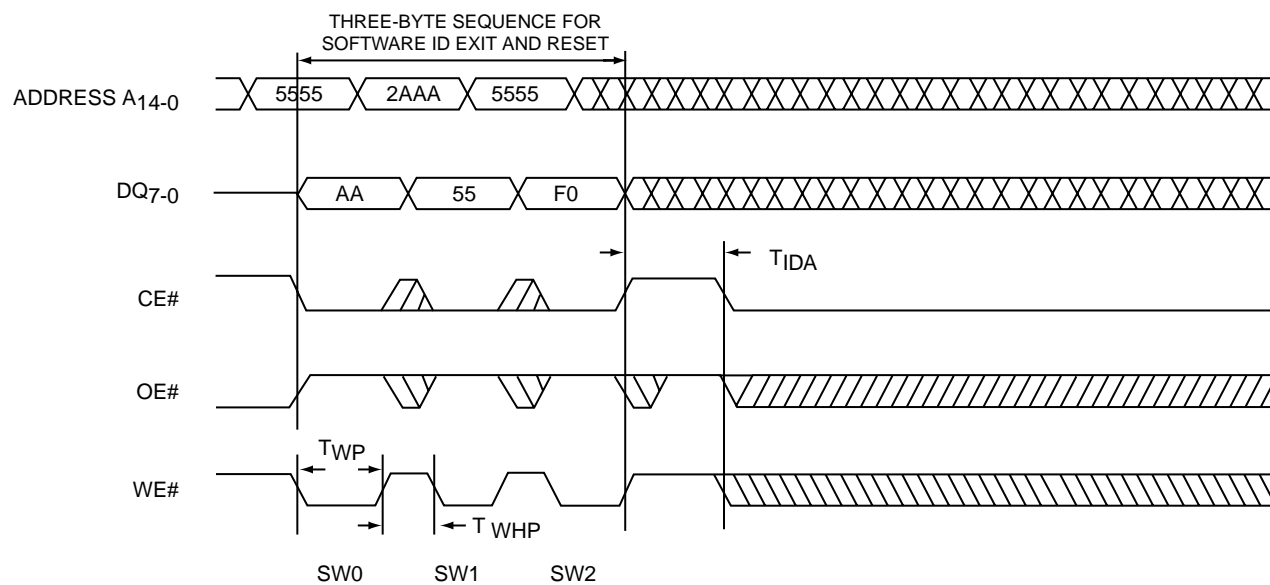
333 ILL F11.1

FIGURE 10: SOFTWARE ID ENTRY AND READ



333 ILL F12.1

FIGURE 11: CFI QUERY ENTRY AND READ



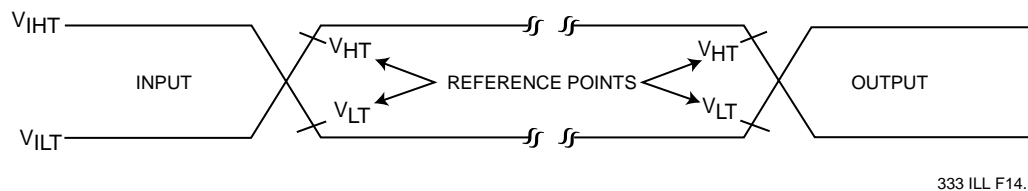
333 ILL F13.0

FIGURE 12: SOFTWARE ID EXIT/CFI EXIT



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AC test inputs are driven at V_{IHT} (2.4 V) for a logic "1" and V_{ILT} (0.4 V) for a logic "0". Measurement reference points for inputs and outputs are V_{HT} (2.0 V) and V_{LT} (0.8 V). Inputs rise and fall times (10% \leftrightarrow 90%) are <10 ns.

Note: V_{HT} — V_{HIGH} Test
 V_{LT} — V_{LOW} Test
 V_{IHT} — V_{INPUT} HIGH Test
 V_{ILT} — V_{INPUT} LOW Test

FIGURE 13: AC INPUT/OUTPUT REFERENCE WAVEFORMS

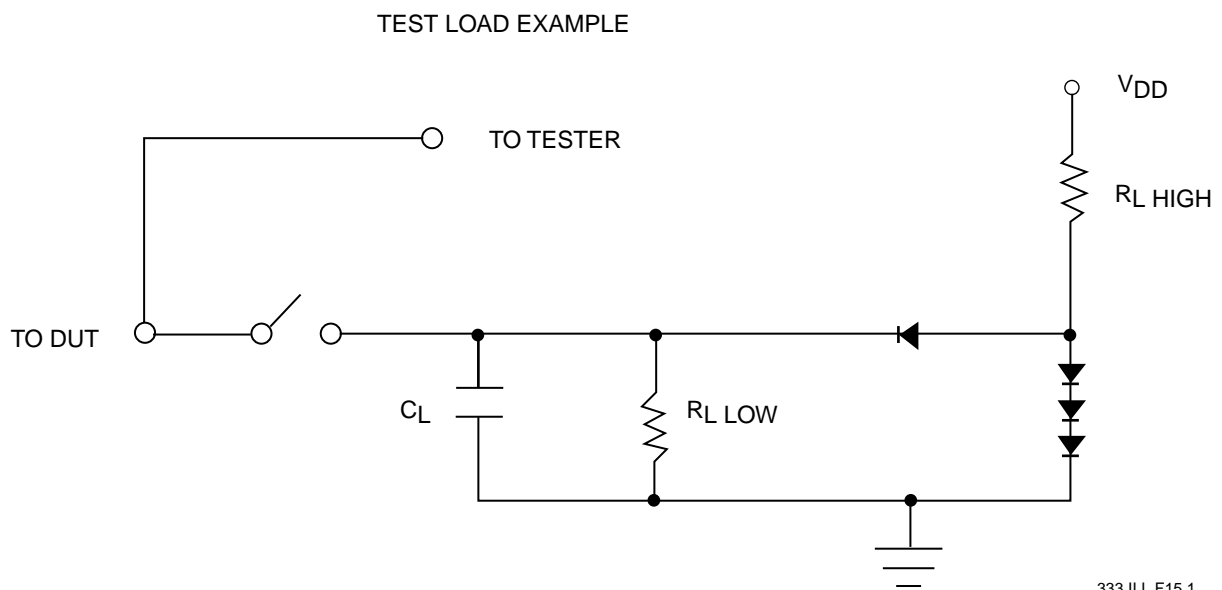


FIGURE 14: A TEST LOAD EXAMPLE

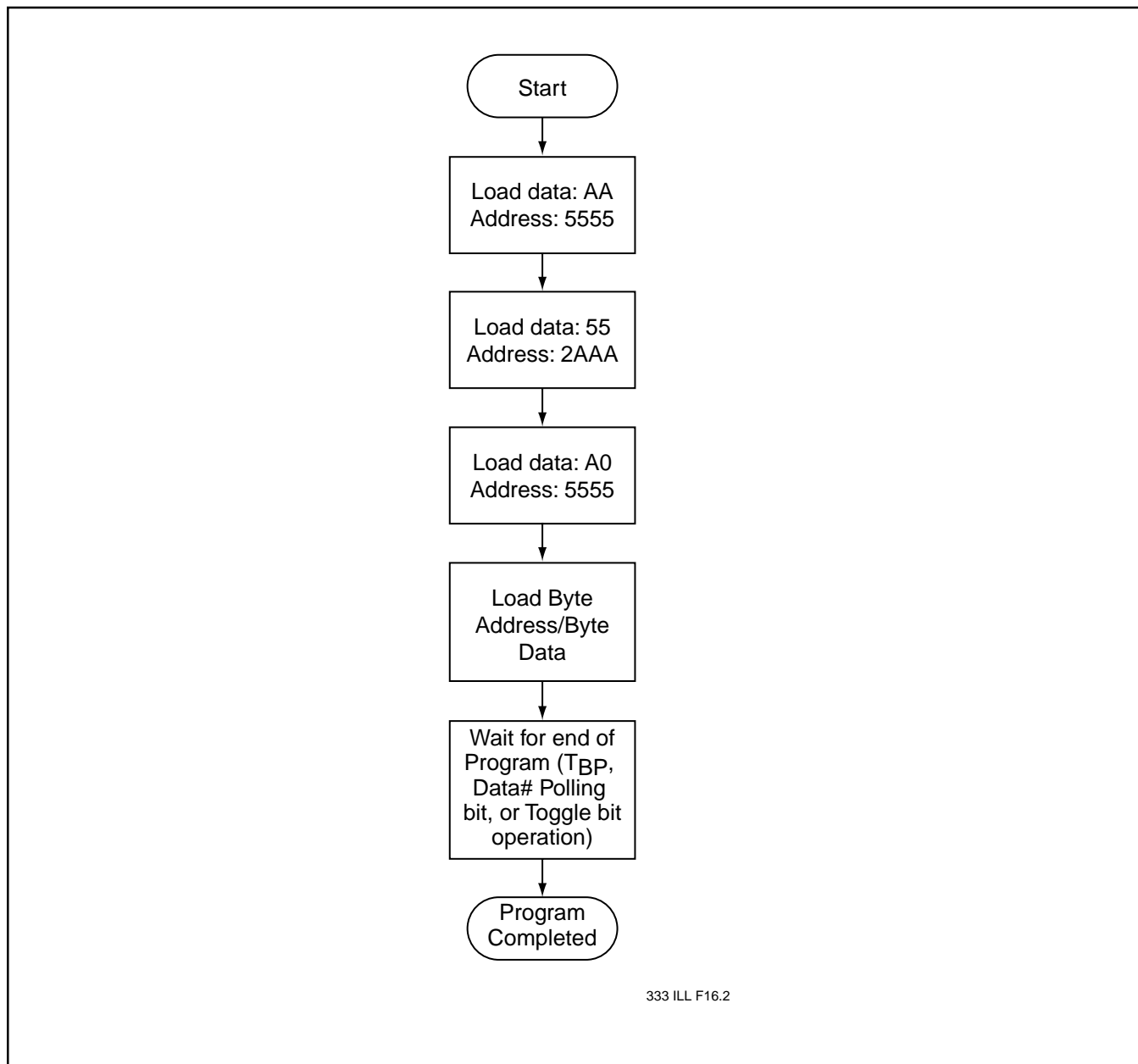


FIGURE 15: BYTE-PROGRAM ALGORITHM



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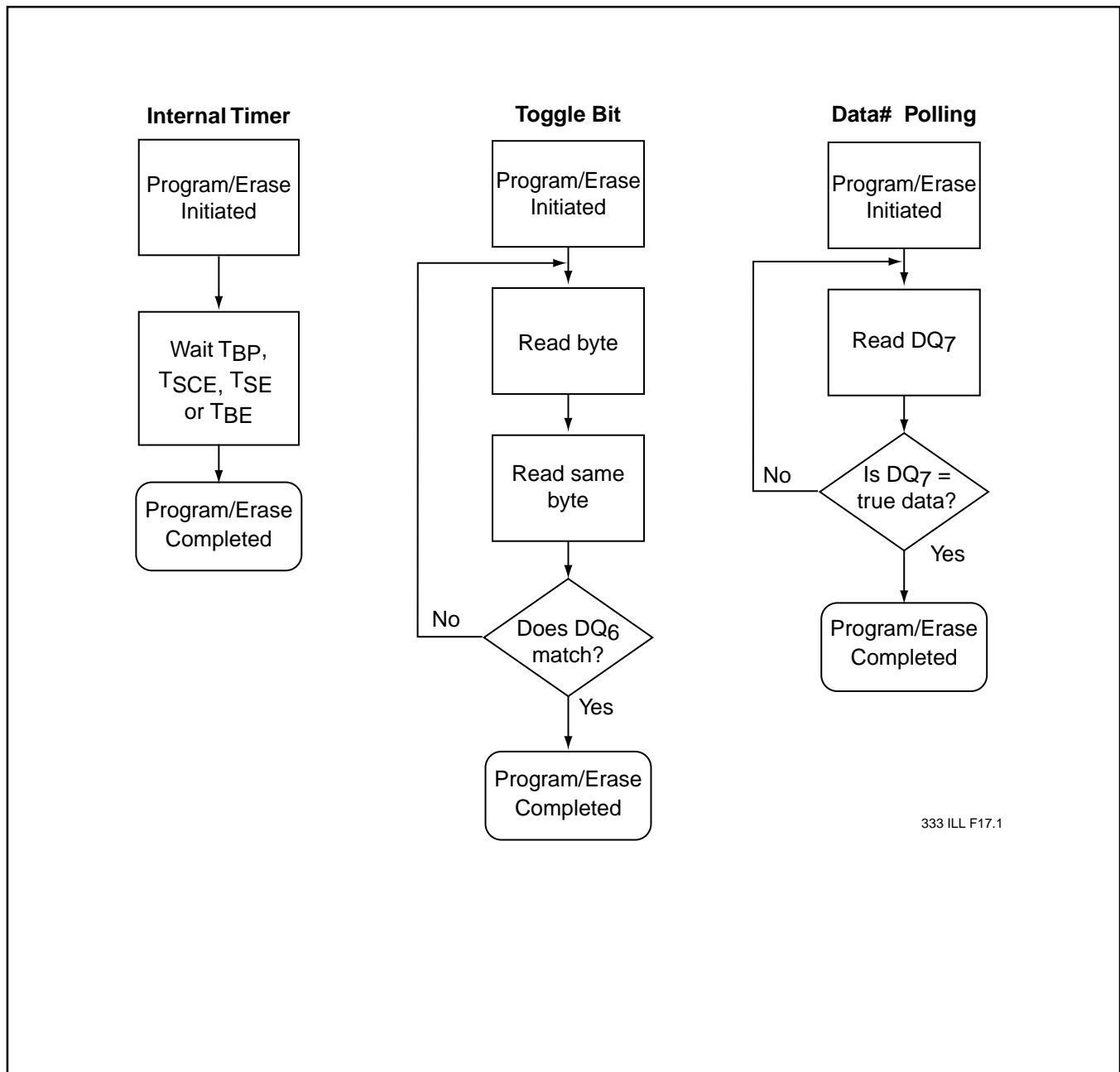


FIGURE 16: WAIT OPTIONS

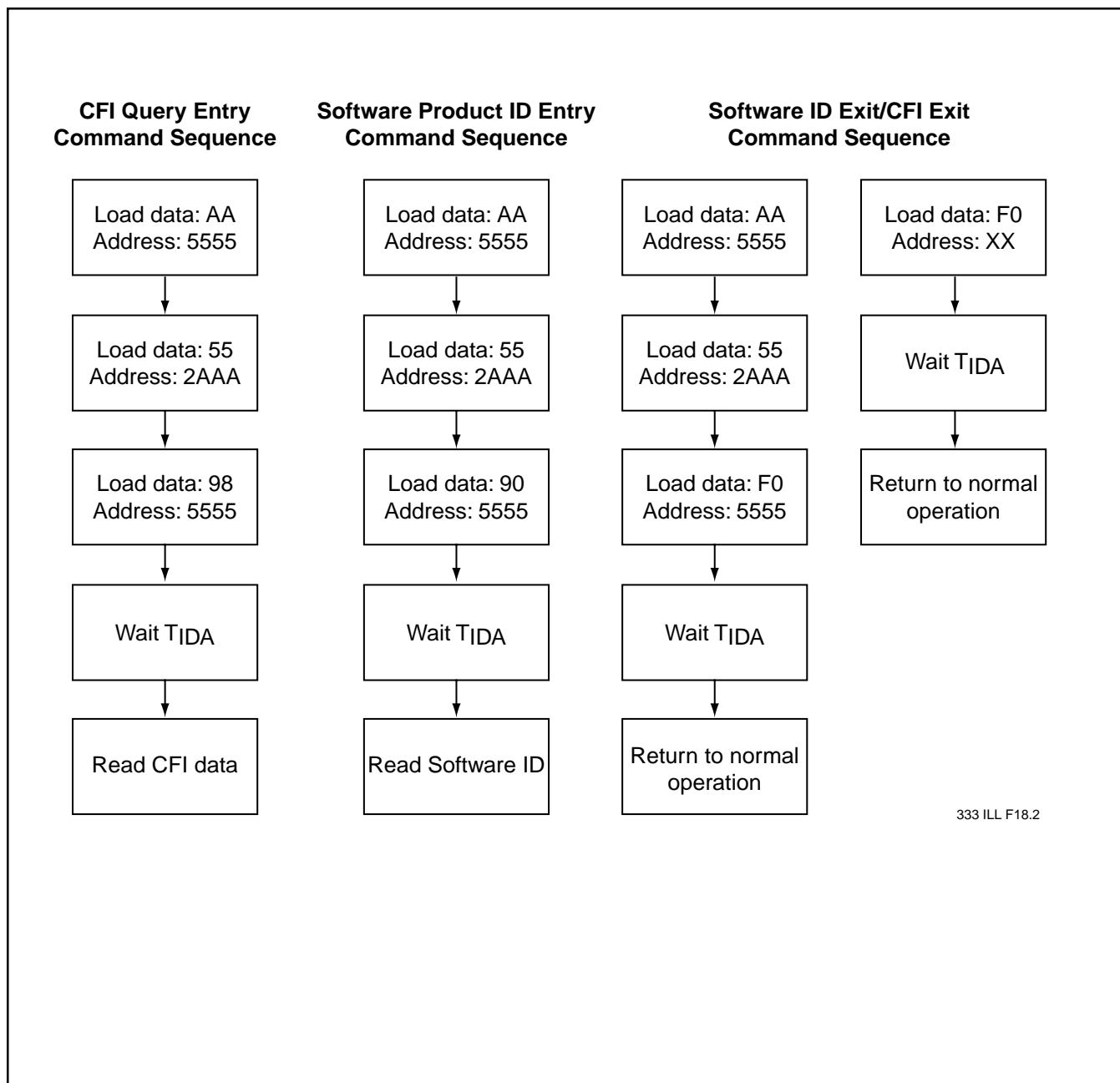


FIGURE 17: SOFTWARE PRODUCT ID/CFI COMMAND FLOWCHARTS



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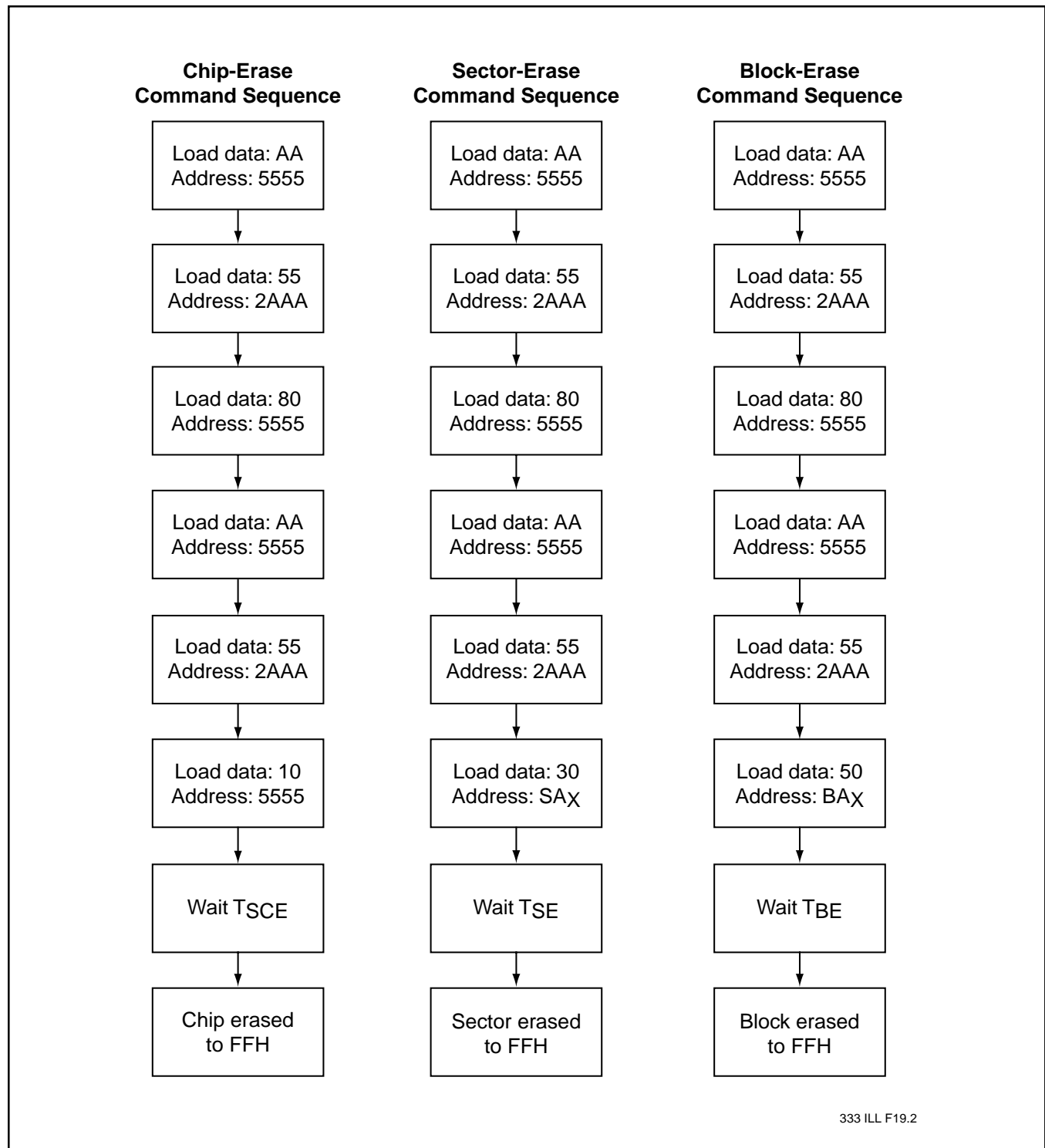
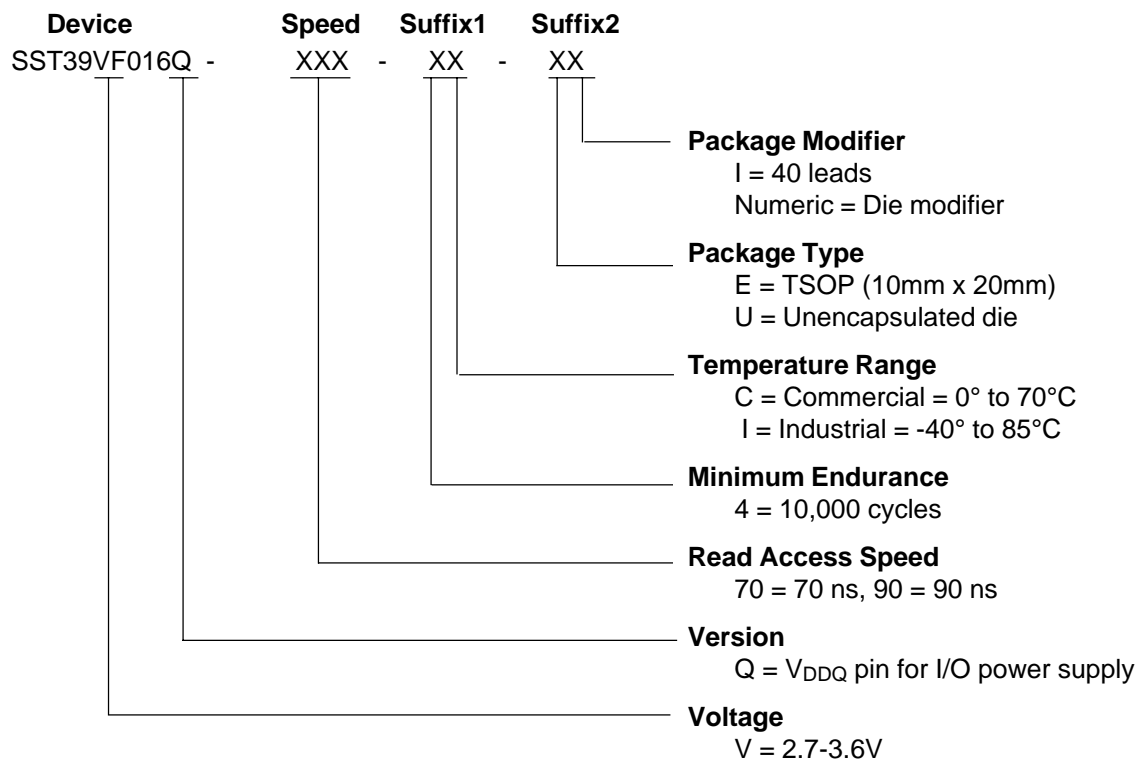


FIGURE 18: ERASE COMMAND SEQUENCE



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SST39VF016Q Valid combinations

SST39VF016Q-70-4C-EI

SST39VF016Q-90-4C-EI

SST39VF016Q-90-4C-U1

SST39VF016Q-70-4I-EI

SST39VF016Q-90-4I-EI

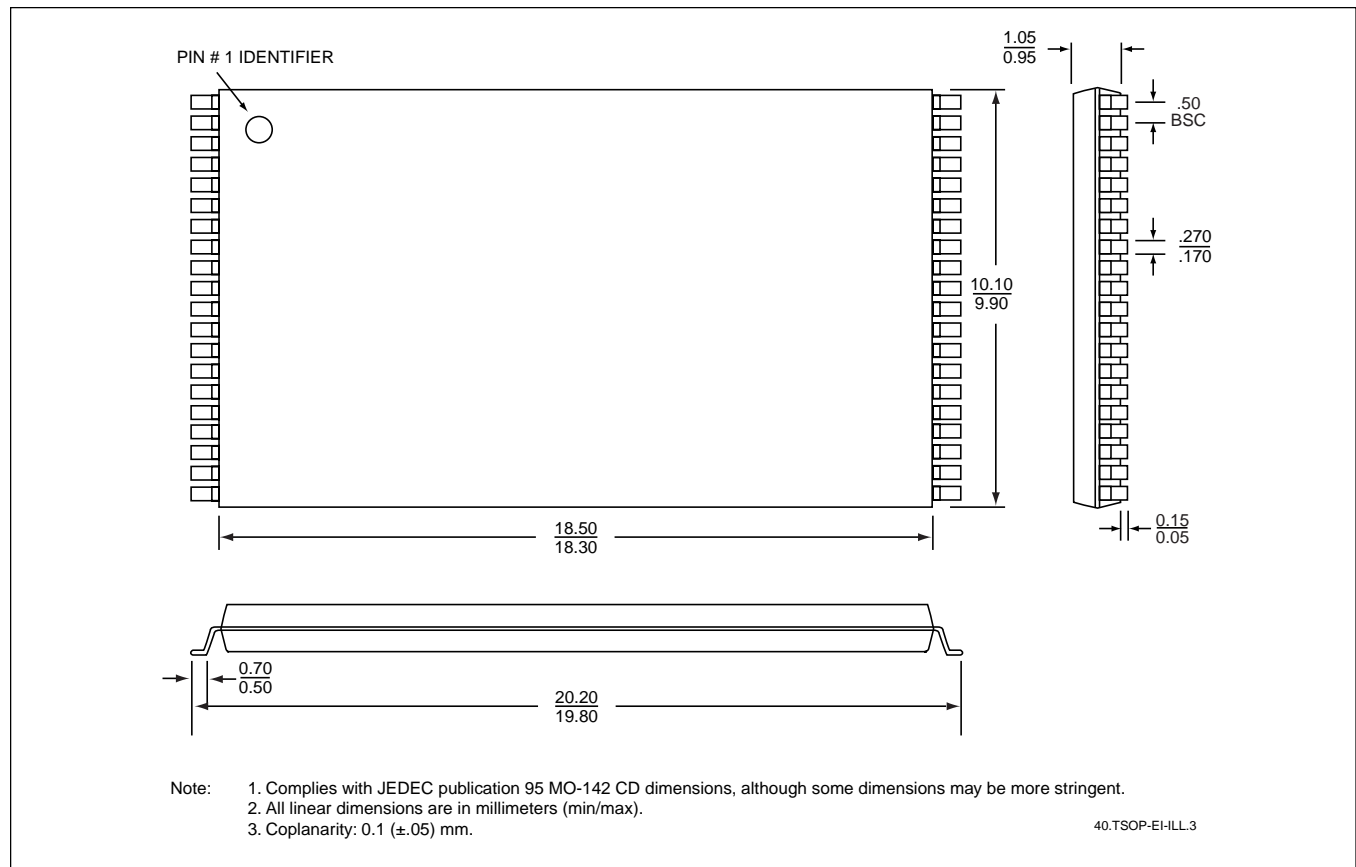
Example : Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.



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PACKAGING DIAGRAMS



40-LEAD THIN SMALL OUTLINE PACKAGE (TSOP)

SST PACKAGE CODE: EI



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Revised 3-11-99

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333-09 12/99