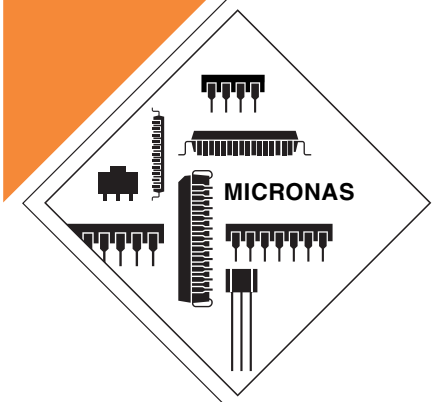

PRELIMINARY DATA SHEET

UAC 3552A
Universal Serial Bus DAC

USB
UNIVERSAL SERIAL BUS

Edition Nov. 9, 1999
6251-487-1PD

MICRONAS

Contents

Contents, continued

Universal Serial Bus DAC

1. Introduction

The UAC 3552A is the first member of Micronas' USB audio controller family of ICs targeting a wide variety of audio applications on the USB. The UAC 3552A is a single-chip, high-precision digital-to-analog audio converter. It includes a high-quality audio sample rate converter and is able to support a wide range of sample rates, as well as different audio formats.

The IC contains a complete USB transceiver that allows direct connection to the USB. An on-chip EEPROM allows storing of manufacturer-specific data or product identification. The EEPROM can be programmed directly via the USB.

Baseband audio processing is handled by an internal, powerful DSP. Apart from basic audio features, like tone and volume control, there is enough processing power left to realize customer-specific applications.

The audio DAC uses Micronas' proprietary multibit sigma-delta technique. It features very low sensitivity to clock jitter, high linearity, and a superior S/N ratio. The UAC 3552A provides an on-chip headphone/ speaker amplifier. Moreover, mixing additional analog audio sources to the D/A-converted signal is supported.

The IC is designed for all kinds of USB audio applications, such as USB active speakers, USB headphones, and USB interfaces to home stereo equipment, etc.

Any existing analog speaker set can easily be upgraded to USB by just including the UAC 3552A according to the application circuit on page 27. No software development is required, because all drivers are already part of the operating system which supports USB (e. g. Windows™ 98).

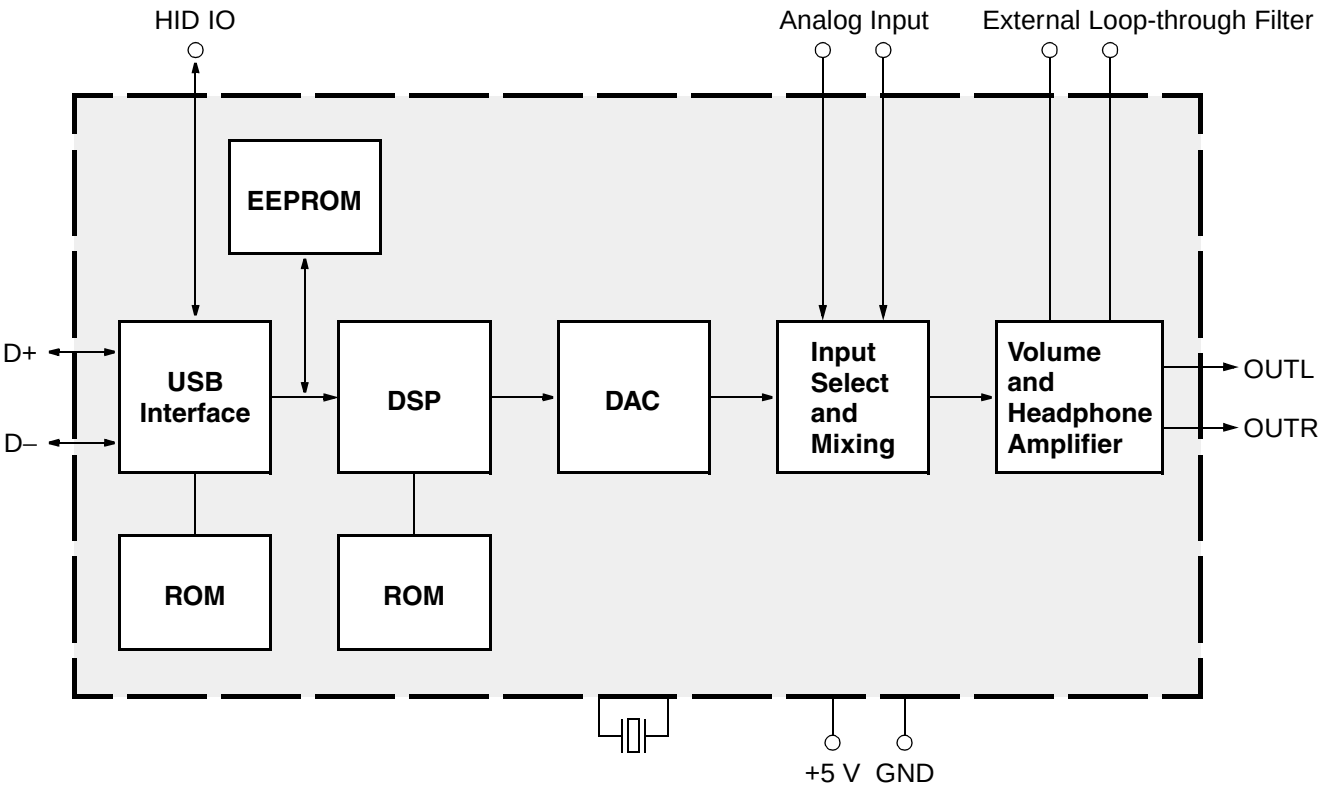

Fig. 1–1: Block diagram of the UAC 3552A

1.1. Features

- single-chip, USB specification 1.0/1.1 compliant, stereo audio D/A converter
- 12-Mbit/s USB transceiver
- adaptive isochronous endpoint for USB Audio
- USB-programmable vendor IDs (1024-bit EEPROM on chip)
- four general purpose input pins and four output pins (human interface pins)
- customizable I/O functionality by download-software
- supports 16-bit mono/stereo and 24-bit stereo audio data
- adaptive sample rate converter for 5 to 50 kHz input sampling rate
- audio baseband control: bass, treble, volume, and balance, additional analog volume, mute
- bass boost
- automatic gain control (AGC)
- “PerfectSpeaker” digital speaker equalizer
- THD better than 0.01 %, SNR of 96 dB
- integrated low-power stereo headphone amplifier
- on-chip op amps for external analog filter
- analog stereo input (AUX) with source selection and mixing
- single 5-V power supply

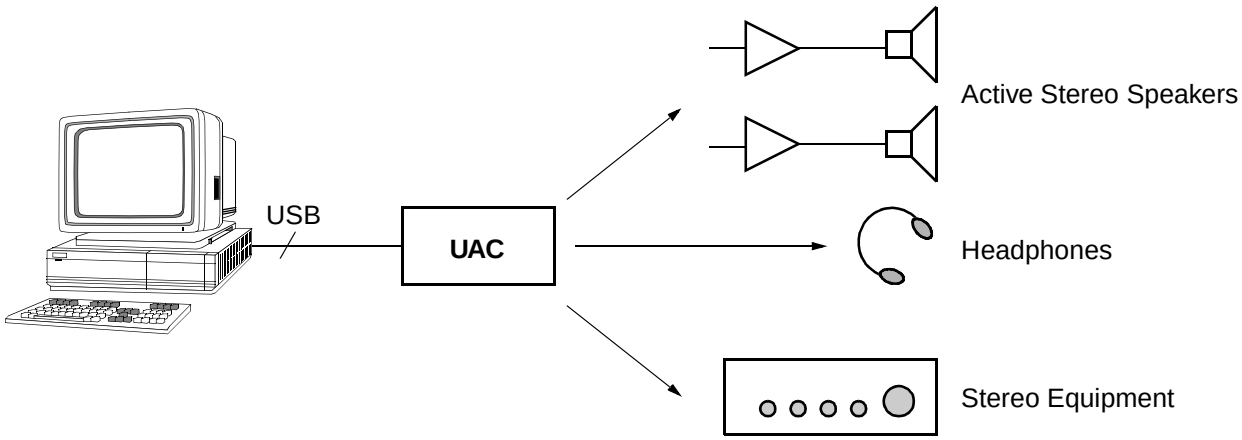

Fig. 1–2: System application diagram

2. Functional Description

2.1. Hardware

A detailed block diagram of the UAC 3552A is depicted in Fig. 2–1. The functions of the blocks are explained in the following sections.

2.1.1. USB Interface

2.1.1.1. Transceiver

The differential input receiver is used to accept the USB data signal according to the full-speed (12 MB/s) USB driver characteristics (USB SPEC 1.1 - 7.1.4).

2.1.1.2. Interface Engine

The interface engine comprises two major sections: the transceiver logic and the receiver logic. The transceiver logic transmits data packets built in memory by the microcontroller. These packets are converted from a serial to a parallel data stream. This includes NRZI encoding, bit stuffing, CRC-computation, and addition of SYNC field and EOP. The receiver logic will receive USB data and stores these packets in its memory for processing by the microcontroller. Serial USB data is converted to a byte-wide parallel data stream and stored in system memory. In addition to USB basic data decoding, the Rx logic performs a PID check and protocol layer checks.

2.1.1.3. Microcontroller

The microcontroller manages buffers for all enabled endpoints and interacts with the interface engine. The buffers are built and decoded in memory. This way, the microcontroller realizes the USB protocol handling, like USB reset, enumeration, and all chapter 9 processing, error handling, as well as class-specific endpoint handling, like audio class and HID class. The audio-class processing consists of interpreting the USB audio commands and accordingly controlling the DSP-audio function through a dedicated audio-control-interface to the DSP. HID class processing means polling keys providing the corresponding key-codes to the host-computer's requests. These keys are connected to the GPIO-pins. The RAM can be accessed by the microcontroller and by the interface-engine's DMA-controller. All endpoint communication is realized with intelligent buffer management built up in the RAM.

A part of the RAM is reserved for download software. This allows adding extra functionality to the GPIO pins, like I^2C-handling or any other control of external components via USB. Downloading is handled by an extra driver which allows direct RAM/ROM access via USB.

The ROM contains the USB drivers for the microcontroller as well as the complete descriptor table including the report descriptor for the HID-class. Some parts of the descriptor which are subjected to be changed by the customer, however, reside in the EEPROM.

The EEPROM is built to keep static customer-related data that will customize the UAC 3552A-based USB device during production.

The 128×8 bit EEPROM contains the customer specific information of the USB device descriptor, like vendor ID, product ID, as well as strings for manufacturer, product and serial number. Apart from this USB-related information, the EEPROM holds customer-specific parameters for the PerfectSpeaker equalizer.

The UAC 3552A is shipped with a preprogrammed EEPROM that allows normal USB functionality even if no reprogramming is performed on the customer's side.

The EEPROM can be programmed via USB by means of UAC 3552A application tools.

2.1.2. Audio Control Interface

The audio control interface links the microcontroller to the DSP and is used to initialize the DSP and to transmit audio-related USB control data, like volume setting, tone control etc.

2.1.3. Audio Streaming Interface

The audio streaming interface directly connects the serial interface engine to the DSP in order to transmit the digital audio data. The interface collects and buffers the burst audio data for further processing by the audio processing unit.

2.1.4. Audio Processing Unit

The audio processing unit is a powerful DSP core which allows high-quality sample conversion, baseband audio processing, and interpolation filtering used for oversampling DAC, as well as customized algorithms. For more details on the software see Section 2.2.2. "Audio Processing Software" on page 11.

2.1.5. Analog Back-end

The analog back-end comprises the audio DAC, analog filters, input mixer, op amps for optimal external postfiltering, analog volume and mute, and the output amplifier.

2.1.5.1. DAC

The DAC uses oversampling technique with 3rd-order multibit noise-shaping. This technique results in extremely low quantization noise in the audio band.

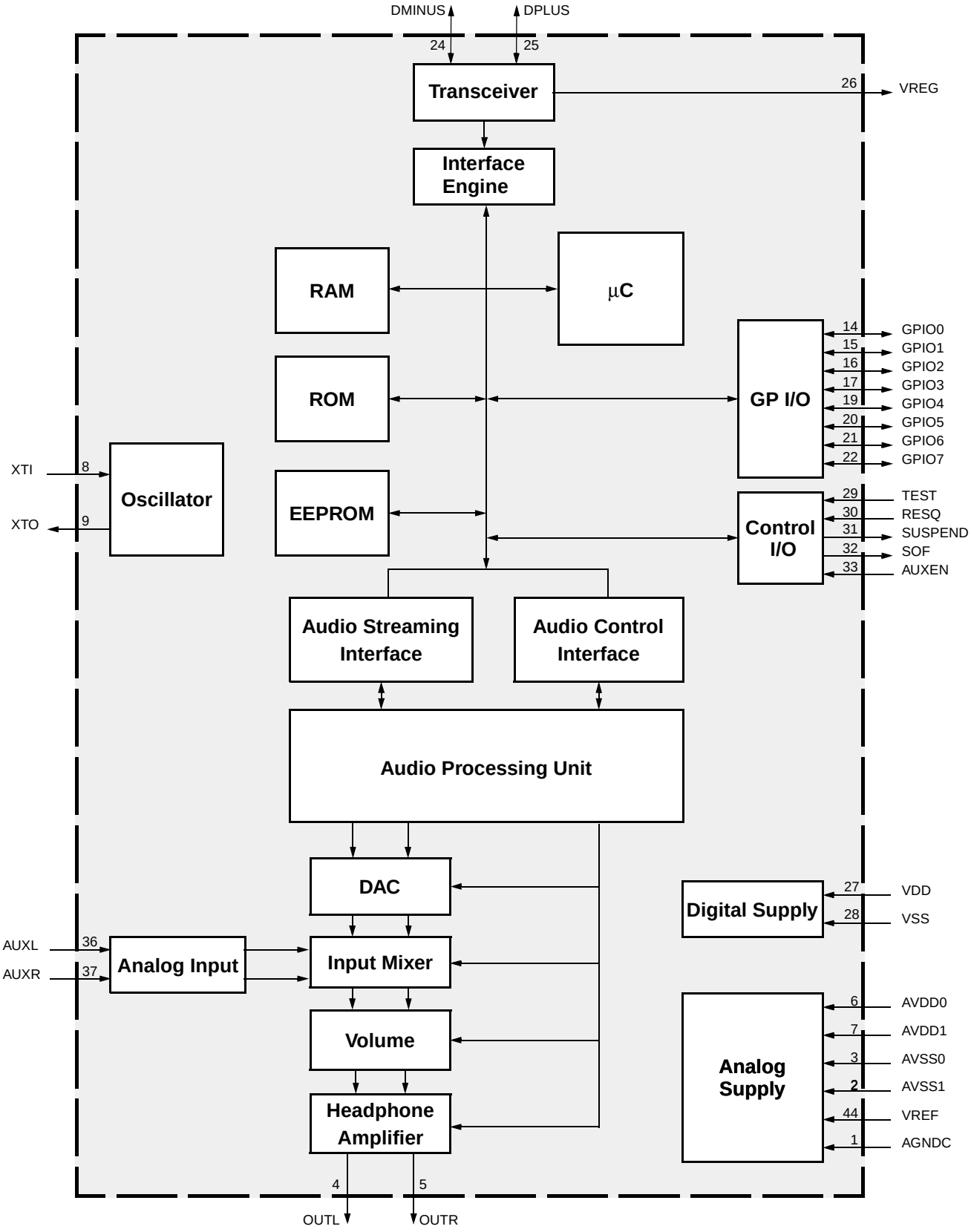

Fig. 2–1: Detailed block diagram of the UAC 3552A

2.1.5.2. Analog Low-pass

The output of the DAC is filterted by an analog low-pass filter with a cut-off frequency of approximately 1.4 MHz. This filter removes the high-frequency components of the noise-shaping signal.

2.1.5.3. Postfilter Op Amps

This block contains the active components for the optional analog postfilters. It is recommended to use a second-order filter (see Section 4. “Applications” on page 26) in order to attenuate the out-of-band noise caused by the noise shaper The op amps and all I/O-pins for this block are shown in Fig. 2–2.

2.1.5.4. Input Mixer

This block is used to mix the auxiliary inputs and the signals coming from the DAC. This allows to use an UAC 3552A-based USB speaker in a non-USB environment, like WIN 3.11 or other operating systems. On the other hand, it allows to connect additional analog sources, like CD-player or Walkman even while the speaker is connected to the USB. The input mixer is hardware-controlled by the AUXEN pin.

Table 2–1: AUXEN pin

AUXEN	
0	AUX not selected
1	AUX selected

This allows to use a jack that switches the AUXEN to low when an analog source is plugged in, according to the application note Section 4. “Applications” on page 26. The DAC-signal is permanently connected to the mixer because the DAC is extremely quiet if no USB audio is applied.

The AUXEN pin also keeps the UAC 3552A from entering the low-power mode when an analog source is connected. Please note that in this mode, the UAC 3552A is not USB-compliant. If the USB is not connected the GPIO pins work as an USB-independent volume control (see Table 2–2). BassBoost is not supported in this mode.

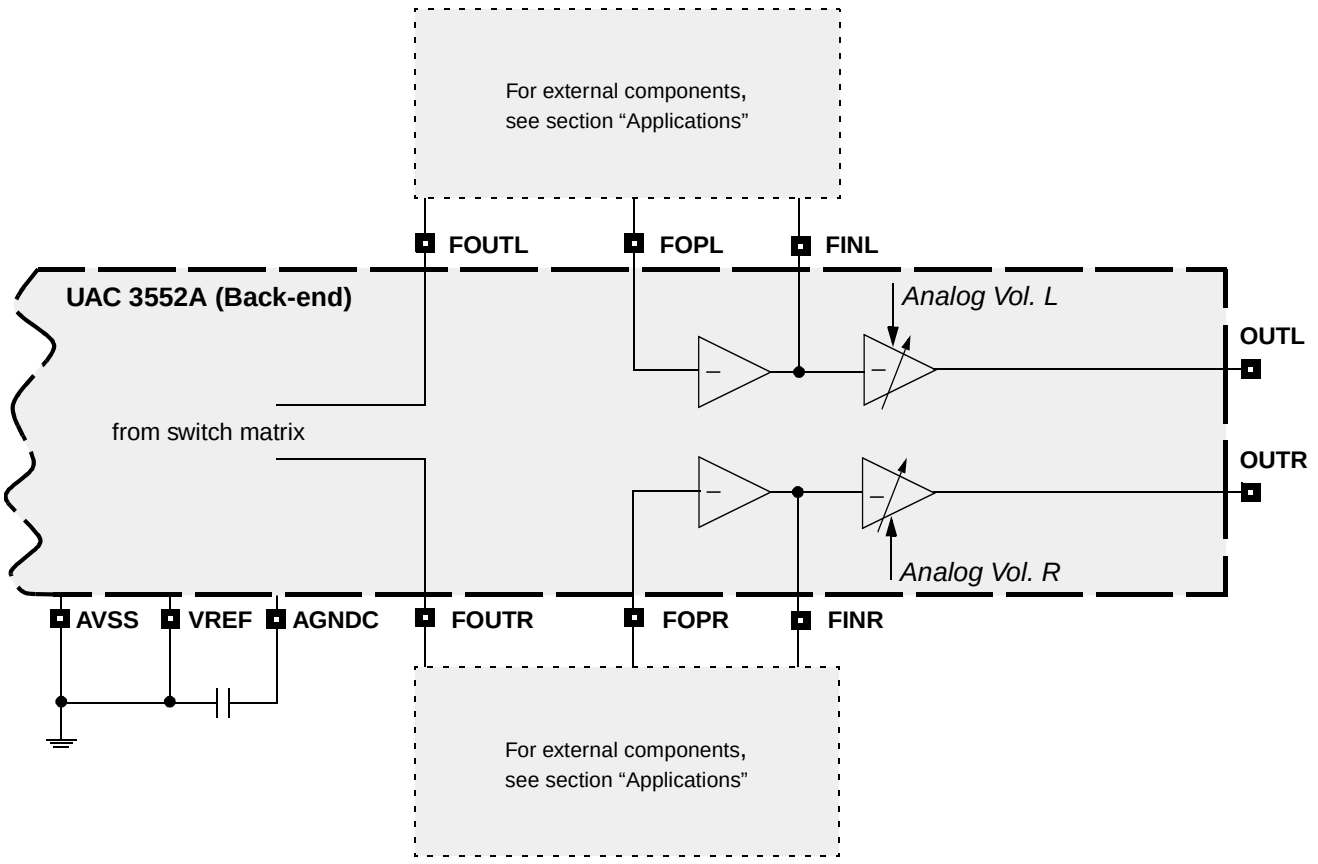

Fig. 2–2: Postfilter op amps and analog volume

2.1.5.5. Analog Volume Control

The analog volume control covers a range from 0 dB to −75 dB plus an additional mute position.

The analog step size is split into a 3-dB and a 1.5-dB range:

−75 dB...–54 dB: 3 dB step size
–54 dB...0 dB: 1.5 dB step size

The overall volume system, however, consists not only of the analog volume. An additional digital volume control allows a step size of 0.5 dB over the complete range. See Section 2.2.2.7. “Volume and Balance Control” on page 13.

Please note that analog input signals (AUXL, AUXR) do not have the additional digital volume control.

2.1.5.6. Line-out/Headphone Amplifier

The line-out/headphone amplifier output is provided at the OUTL and OUTR pins connected either to stereo headphones or to the power amplifier within an USB speaker. The stereo headphones require external 47-Ω serial resistors in both channels. See Section 4. “Applications” on page 26.

2.1.6. General Purpose I/O

The GPIO pins are used to connect keys which are related to the USB HID class or for vendor-specific control functions and LEDs in order to indicate on/off states for example. The standard configuration defines the GPIOs as four input pins (GPIO0...GPIO3) and four output pins (GPIO4...GPIO7). The function of the input pins is shown in Table 2–2.

Table 2–2: Standard Key Configuration

Pin	Function	Key Code	Usage ID
GPIO0	Volume Up	1	E9
GPIO1	Volume Down	2	EA
GPIO2	MuteToggle	4	E2
GPIO3	BassBoost Toggle	8	E5

The keys are polled by the microcontroller and the corresponding key codes are transmitted to the host on request. The relation between key code and usage ID (see Universal Bus HID Usage Tables, Version 1.0, Chapter 14 – Consumer Page) is defined in the HID report descriptor (see Section 2.2.1.4. “HID Report Descriptor” on page 11) which is transmitted to the host along with the configuration descriptor during the bus enumeration.

When the device is not connected to USB, the functionality of the volume-control and mute pins are preserved. In this case, however, the parameters are directly transferred to the DSP-core. This allows using the device in stand-alone mode providing volume and mute control for analog sources.

The output pins are not predefined and therefore not related to any USB functions. They can be set or reset by vendor-specific software.

The standard configuration can be changed also by vendor-specific USB software, but in this case, Table 2–2 is no longer valid.

2.1.7. Special I/O

2.1.7.1. SOF (Start of Frame)

The SOF-pin provides a 1-ms signal which is synchronous to the USB 1-ms frame rate. It can be used for test purpose or as an USB-synchronous reference for vendor-specific external circuitry.

2.1.7.2. AUXEN

This is a digital input that has to be used if an analog signal is connected to the AUX R/L pins. It triggers the microcontroller to switch the input mixer to the analog input (the DAC signal always remains active!) and it keeps the device from entering the low-power mode which can be requested by the host PC or by disconnecting the device from the USB.

2.1.7.3. SUSPEND

The SUSPEND pin indicates the low-power mode. It can be used to power down external circuitry, like power amplifiers in an USB speaker.

Table 2–3: SUSPEND pin

SUSPEND	
low	normal power
high	low power

2.1.8. Clock System

The UAC 3552A requires a 12-MHz clock source, which is realized as an on-chip oscillator with external crystal. Also an external oscillator can be used. In this case, the clock has to be connected to XTI. The 12 MHz is the input clock for a PLL circuit which generates all clocks needed within the IC.

2.2. Software

The functionality of the UAC 3552A is mainly defined by software. The internal µ-controller handles the USB requests whereas the Audio Processing Unit processes the sound features.

2.2.1. USB Microcontroller Software

2.2.1.1. Chapter 9 Functions

The chapter 9 of the USB Spec 1.1 defines the USB device framework which is the middle layer of the USB protocol hierarchy (see USB Spec 1.1 page 175). It handles routing data between the bus interface and various endpoints. The endpoint is a source or sink for data within the device.

2.2.1.2. Device Descriptor

Unlike the configuration descriptor, which is located in ROM, the device descriptor is more flexible. The manufacturer-related data are stored in the on-chip EEPROM, and can be adapted individually. In detail these data are

– vendor ID
– product ID
– device release number
– manufacturer string
– product string
– serial number string

A comfortable programming tool allows this data to be defined and writes it into the corresponding EEPROM location.
The UAC 3552A is shipped with the Micronas device descriptor and allows USB functionality without any EEPROM reprogramming.

2.2.1.3. String Descriptor

The string descriptor is located in the EEPROM. The UAC 3552A holds three strings. The programming tool handles the programming of strings and will take care of string length control also.
The UAC 3552A is shipped with the Micronas string descriptor and allows USB functionality without any EEPROM reprogramming.

2.2.1.4. HID Report Descriptor

The HID report descriptor defines the functionality of the GPIO Pins. The basic information here are the usage IDs for the key inputs. These IDs are stored in the EEPROM and can therefore be modified if the default configuration does not fit the application. The UAC 3552A, however, only supports the default functions: volume up/down, mute on/off and BassBoost on/off. This means, that all nonstandard usage IDs will be transmitted to the host on request and can be used with vendor specific software, but only the default IDs will work together with the operating system.

2.2.2. Audio Processing Software

All audio processing is realized by DSP-software, apart from volume control which is located in the analog back-end. The audio building blocks split into USB-independent features, like sample rate conversion and oversampling filters and blocks which belong to the so called USB feature unit, defined in the USB Device Class Definition for Audio Devices. The feature unit provides basic manipulation of the incoming logical channels. The UAC 3552A supports two logical channels (i.e. left & right). Multichannel or surround systems, however, can also be realized using more than one UAC 3552A, because phase or delay distortion is eliminated by locking the audio processing to the USB frame rate. An overview of the architecture is given in Fig. 2–3.

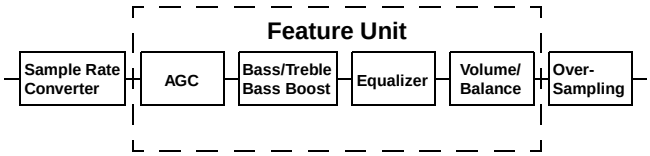

Fig. 2–3: Audio processing

2.2.2.1. Sample Rate Converter

The purpose of the sample rate converter is first to transform the block transferred audio data into a continuous data stream and second to convert all incoming sample rates to a fixed 50-kHz sample rate. This technique eliminates input data jitter. Furthermore, all audio algorithms and the DAC run on a single sample rate and no parameter switching is required on change of audio sampling rate. Furthermore, all audio clocks, such as sampling clock, noise-shaping clock, and DAC-clock can be derived from a single free-running 12-MHz oscillator. This mechanism allows continuous input sampling rates from 5 kHz up to 50 kHz.

2.2.2.2. Automatic Gain Control

The Automatic Gain Control (AGC) is one of the building blocks of the feature unit (USB Device Class Definition for Audio Devices 1.0, page 39).

Different sound sources fairly often do not have the same volume level. The Automatic Gain Control solves this problem by equalizing the volume levels within a defined range. Below a theshold level the signals are not affected. The level-adjustment is performed with time constants in order to avoid short-time adjustments due to signal peaks.

2.2.2.3. Bass Control

The bass control provides gain or attenuation to frequency components below a corner frequency of 120 Hz. The characteristic is shown in Fig. 2–4.

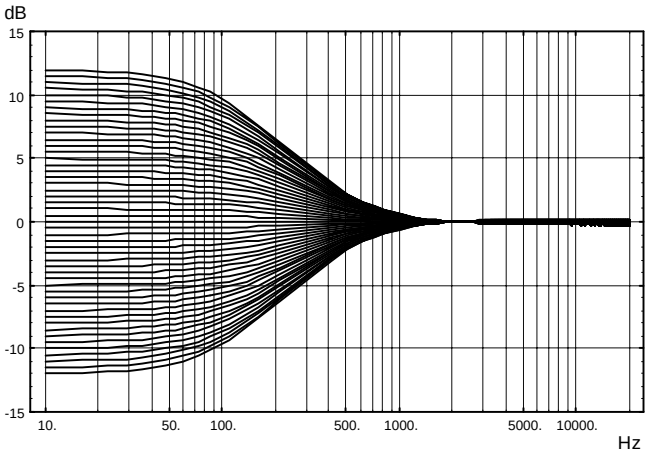

Fig. 2–4: Bass control

The bass control works identically on both channels.

Table 2–4: Bass Control Characteristics

Min	Max	Step
–12 dB	+12 dB	0.5 dB

2.2.2.4. Treble Control

The treble control provides gain or attenuation to frequency components above a corner frequency of 6 kHz. The characteristic is shown in Fig. 2–5.

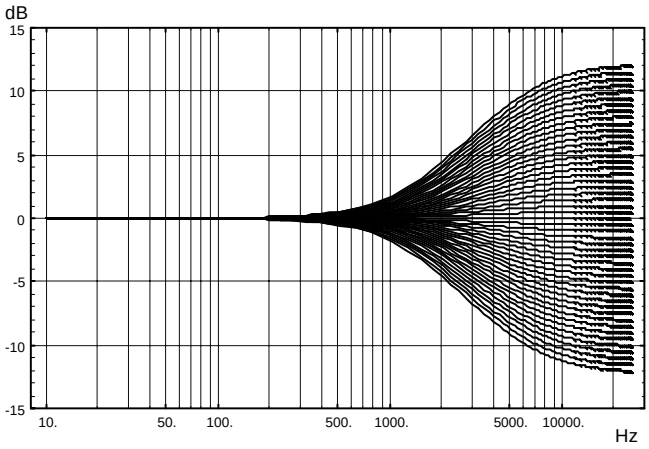

Fig. 2–5: Treble control

The treble control works identically on both channels.

Table 2–5: Treble Control Characteristics

Min	Max	Step
–12 dB	+12 dB	0.5 dB

2.2.2.5. Bass Boost Control

The bass boost algorithm provides an additional 12-dB gain for the low-frequency components. The characteristic is shown in Fig. 2–6.

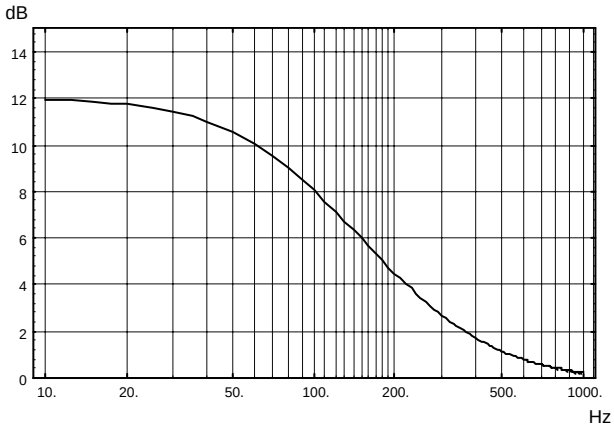

Fig. 2–6: Bass boost

The bass boost works on both channels and can be switched on and off under USB control.

2.2.2.6. Parametric Equalizer

The parametric equalizer is a non-USB audio feature. It allows the compensation of unwanted frequency responses of a speaker. Alternatively, frequency responses can be set to suit individual tastes. The equalizer consists of 5 individually adjustable bands. The control parameters and the parameter range for each band is shown in Table 2–6.

Table 2–6: Equalizer Parameters

Parameter	Min	Max
center frequency	50 Hz	15 kHz
gain/attenuation	–6 dB	+6 dB
filter quality (Q)	0.5	3

The adjustment of the equalizer is supported by an application program that allows to set up frequency responses and to download the corresponding filter coefficients into the UAC 3552A. When the frequency response fits the target, it can be programmed into the on-chip EEPROM. The UAC 3552A is shipped with a flat frequency response.

2.2.2.7. Volume and Balance Control

The volume and balance control operate separately on the left and right channel.

Table 2–7: Volume and Balance Control

Min	Max	Step
–75 dB	0 dB	0.5 dB

The volume control is realized in the analog back-end. This preserves high audio quality (SNR) at low volume settings because signal and noise are attenuated in the same way, which is not the case for pure digital volume control. The UAC 3552A uses digital volume control only for the fine tuning of the 0.5 dB step size. The volume setting is smoothed by an internal ramping algorithm in order to avoid audible clicks during volume change.

The splitting between analog and digital volume is handled by the UAC 3552A automatically.

2.2.3. Mute Control

The mute control is part of the volume system in the UAC 3552A. It functions simultaneously on both channels and can be switched on and off under USB control. As with the volume control, clicks are avoided by a ramping algorithm.

2.2.3.1. Oversampling

The oversampling filter increases the audio sampling rate by a factor of 4. The final upsampling to the noise-shaping rate is handled by a sample and hold circuit. The pass-band characteristic of the oversampling filter is shown in Fig. 2–7.

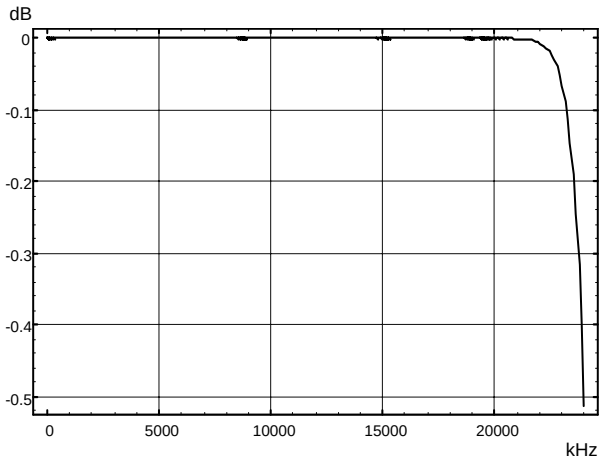

Fig. 2–7: 1 to 4 Oversampling filter, pass-band

3. Specifications

3.1. Outline Dimensions

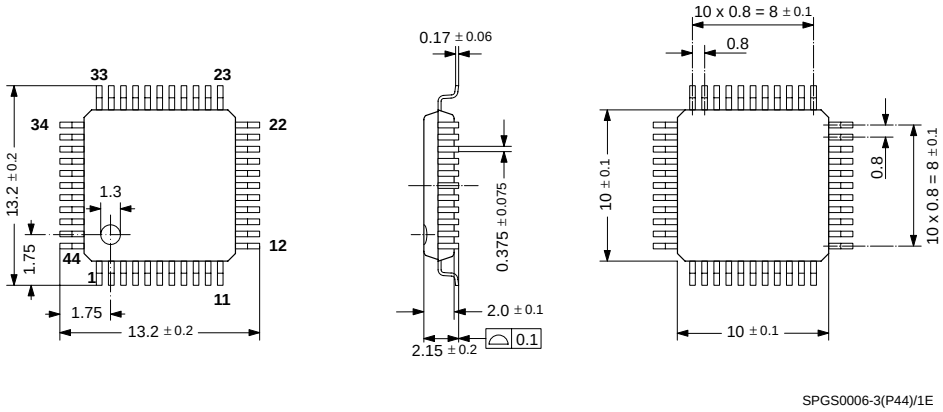

Fig. 3–1:
44-Pin Plastic Metric Quad Flat Pack
(PMQFP44)
Weight approximately 0.4 g
Dimensions in mm

3.2. Pin Connections and Short Descriptions

NC = not connected, leave vacant
LV = if not used, leave vacant
VSS = if not used, connect to VSS

X = obligatory; connect as described in circuit diagram
VDD = connect to VDD

Pin No.	Pin Name	Type	Connection (If not used)	Short Description
1	AGNDC	IN/OUT	X	Analog reference voltage
2	AVSS1	IN	X	VSS 1 for audio back-end
3	AVSS0	IN	X	VSS 0 for audio output amplifiers
4	OUTL	OUT	LV	Audio Output: Headphone left or Speaker +
5	OUTR	OUT	LV	Audio Output: Headphone right or Speaker –
6	AVDD0	IN	X	VDD 0 for audio output amplifiers
7	AVDD1	IN	X	VDD 1 for audio back-end
8	XTI	IN	X	quartz oscillator pin 1
9	XTO	OUT	X	quartz oscillator pin 2
10	NC		LV	Not connected
11	NC		LV	Not connected
12	NC		LV	Not connected
13	NC		LV	Not connected
14	GPIO 0	IN	VSS	HID IO 0
15	GPIO 1	IN	VSS	HID IO 1

Pin No.	Pin Name	Type	Connection (If not used)	Short Description
16	GPIO 2	IN	VSS	HID IO 2
17	GPIO 3	IN	VSS	HID IO 3
18	NC		LV	Not connected
19	GPIO 4	OUT	LV	HID IO 4
20	GPIO 5	OUT	LV	HID IO 5
21	GPIO 6	OUT	LV	HID IO 6
22	GPIO 7	OUT	LV	HID IO 7
23	TRDY	OUT	LV	Test Output Pin
24	DMINUS	IN/OUT	X	USB DATA MINUS
25	DPLUS	IN/OUT	X	USB DATA PLUS
26	VREG	OUT	X	Capacitor for internal supply
27	VDD	IN	X	digital VDD
28	VSS	IN	X	digital VSS
29	TEST	IN	X	Test Enable
30	RESQ	IN	VDD	Power On Reset, active low
31	SUSPEND	OUT	LV	Low-Power Mode Indicator
32	SOF	OUT	LV	1-ms Start-Of-Frame Signal
33	AUXEN	IN	VSS	Enable AUX Input
34	NC		LV	Not connected
35	NC		LV	Not connected
36	AUXL	IN	VSS	AUX Input Left
37	AUXR	IN	VSS	AUX Input Right
38	FOUTL	OUT	X	Output to left external filter
39	FOPL	IN/OUT	X	Filter op amp inverting input, left
40	FINL	IN/OUT	X	Input for FiltoutL or filter op amp output (line out)
41	FOUTR	OUT	X	Output to right filter op amp
42	FOPR	IN/OUT	X	Right Filter op amp inverting input
43	FINR	IN/OUT	X	Input for FILTOUTR or Filter op amp output (line out)
44	VREF	IN	X	Analog reference Ground

3.3. Pin Descriptions

3.3.1. Power Supply Pins

The UAC 3552A combines various analog and digital functions which may be used in different modes. For optimized performance, major parts have their own power supply pins. All VSS power supply pins must be connected.

VDD (27)
VSS (28)
The VDD and VSS power supply pair are connected internally with all digital parts of the UAC 3552A**.**

AVDD0 (6)
AVSS0 (3)
AVDD0 and AVSS0 are separate power supply pins that are exclusively used for the on-chip headphone/ loudspeaker amplifiers.

AVDD1 (7)
AVSS1 (2)
The AVDD1 and AVSS1 pins supply the analog audio processing parts, except the headphone/loudspeaker amplifiers.

3.3.2. Analog Audio Pins

AGNDC (1)
Reference for analog audio signals. This pin is used as reference for the internal op amps. This pin must be blocked against VREF with a 3.3-µF capacitor.

Note: The pin has a typical DC-level of 2.25 V. It can be used as reference input for external op amps when no current load is applied.

VREF (44)
Reference ground for the internal band-gap and biasing circuits. This pin should be connected to a clean ground potential. Any external distortions on this pin will affect the analog performance of the UAC 3552A.

DMINUS (24)
DPLUS (25)
Differential USB port pins.

AUXL (36)
AUXR (37)
The AUX pins provide two analog stereo inputs. Auxiliary input signals, e.g. the output of a conventional receiver circuit or the output of a tape recorder can be connected with these inputs. The input signals have to be connected by capacitive coupling.

FOUTL (38)
FOPL (39)
FINL (40)
FOUTR (41)
FOPR (42)
FINR (43)
Filter op amps are provided in the analog baseband signal paths. These inverting op amps are freely accessible for external use by these pins.

The FOUTL/R pins are connected with the buffered output of the internal switch matrix. The FOPL/R-pins are directly connected with the inputs of the inverting filter op amps. The FINL/R pins are connected with the outputs of the op amps.

OUTL (4)
OUTR (5)
The OUTL/R pins are connected to the internal output amplifiers. They can be used for either line-out or stereo headphones.

Caution: A short circuit at these pins for more than a momentary period may result in destruction of the internal circuits.

XTI (8)
XTO (9)
The XTI pin is connected to the input of the internal crystal oscillator; the XTO pin to its output. Both pins should be directly connected to the crystal and two ground-connected capacitors (see application diagram).

3.3.3. Other Pins

TEST (29)
Test enable. This pin is for test purposes only and must always be connected to VSS.

VREG (26)
This pin is used to connect an external buffer capacitor to stabilize the internal supply for the USB transceiver.

RESQ (30)
This pin may be used to reset the chip.

GPIO 0 ... GPIO 7 (14,15,16,17,19,20,21,22)
These pins are configurable to be either input or output and can be used to connect audio function keys or signalling LEDs.

SUSPEND (31)
This pin indicates that the host PC sets the USB bus to the suspend-mode state.

SOF(32)
Start of Frame Signal. 1-ms signal that can be used for external application circuits.

AUXEN (33)
Aux enable. This pin must be connected to VSS if an analog source is connected to the AUX input. Otherwise connect to VDD.

TRDY (23)
Test Output Pin. This pin is intended for test purposes only and must not be connected.

3.4. Pin Configuration

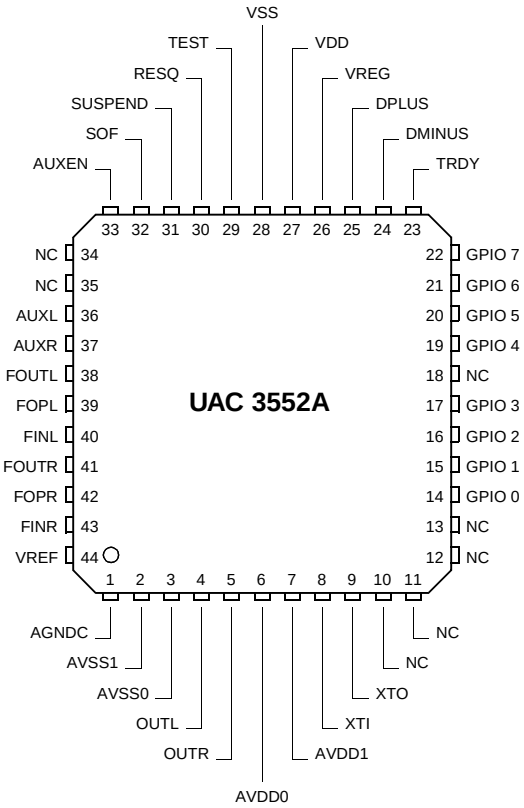

Fig. 3–2: 44-pin PMQFP package

3.5. Pin Circuits

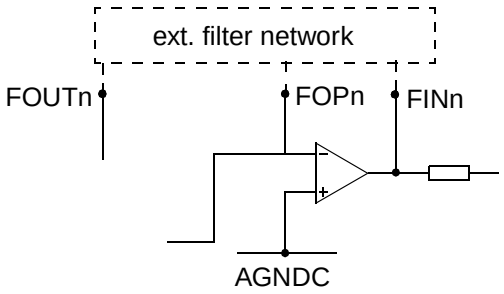

Fig. 3–3: Pins FINR, FOPR, FINL, FOPL

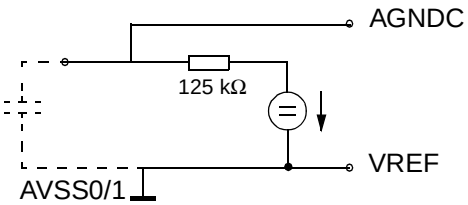

Fig. 3–4: Pins AGNDC, VREF

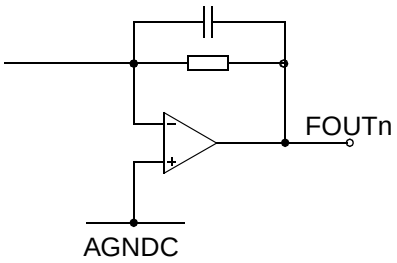

Fig. 3–5: Output Pins FOUTL, FOUTR

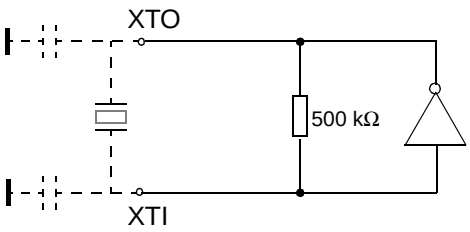

Fig. 3–6: Output/Input Pins XTI, XTO

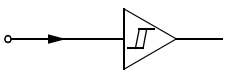

Fig. 3–7: Input Pins RESQ, TEST, AUXEN

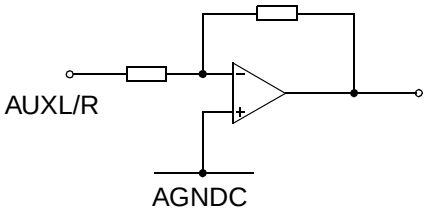

Fig. 3–8: Input Pins AUXL/R

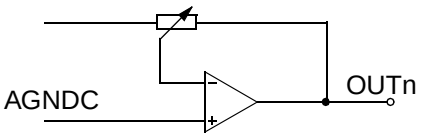

Fig. 3–9: Output Pins OUTL, OUTR

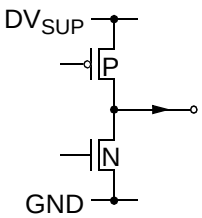

Fig. 3–10: Digital Output Pins SOF, SUSPEND

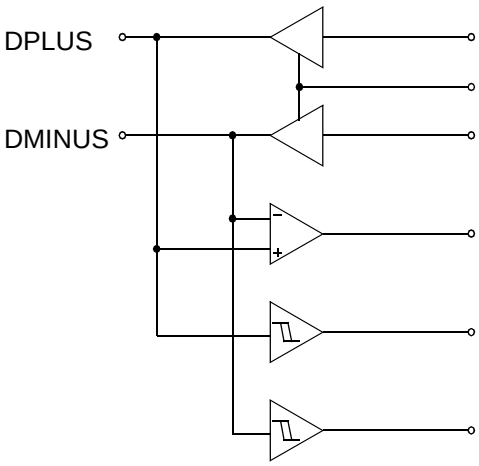

Fig. 3–11: Digital Input/Output Pins DMINUS, DPLUS

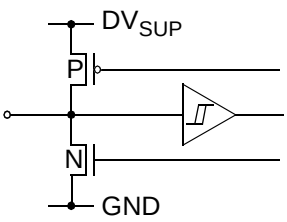

Fig. 3–12: Input/Output Pins GPIO0...GPIO7

3.6. Electrical Characteristics

3.6.1. Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Min.	Max.	Unit
T_A	Ambient Operating Temperature		0	70	°C
T_S	Storage Temperature		–40	125	°C
P_{Pmax}	Power Dissipation		–	900	mW
V_{SUPA}	Analog Supply Voltage[1)]	AVDD0/1	–0.3	6	V
V_{SUPD}	Digital Supply Voltage		–0.3	6	V
V_{Idig}	Input Voltage, all digital inputs		–0.3	V_{SUPD} + 0.3	V
I_{Idig}	Input Current, all digital inputs		–5	+0.5	mA
I_{Idig}	Input Current, all digital outputs		–8	8	mA
I_{Odig}	Output Current, all digital outputs		–14.8	14.8	mA
V_{Iana}	Input Voltage, all analog inputs		–0.3	V_{SUPA} + 0.3	V
I_{Iana}	Input Current, all analog inputs		–5	–5	mA
I_{Oaudio}	Output Current, audio output[2)]	OUTL/R		0.2	A

1) Both have to be connected together!
2) These pins are NOT short-circuit proof!

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

3.6.2. Recommended Operating Conditions

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
Temperature Ranges and Supply Voltages						
T_A	Ambient Temperature Range		0		70	°C
V_{SUPA1}	Analog Audio Supply Voltage	AVDD0/1	4.5	5.0	5.5	V
V_{SUPD}	Digital Supply Voltage	VDD	4.5	5.0	5.5	V
Relative Supply Voltages						
V_{SUPA}	Analog Audio Supply Voltage in relation to the Digital Supply Voltage	AVDD0/1	V_{SUPD} –0.25 V		5.5 V	
V_{IL}	Input Voltage Low	GPI[7:0], AUXEN,			0.25	V_{SUPD}
V_{IH}	Input Voltage high	GPI[7:0], AUXEN	0.75			V_{SUPD}
V_{RIL}	Reset Input high-low transition voltage	RESQ			0.45	V_{SUPD}
V_{RIH}	Reset Input low-high transition voltage	RESQ	0.8			V_{SUPD}
T_{RL}	Reset low time after VDD stable and oscillator start-up	RESQ	5			µs
Analog Reference						
C_{AGNDC1}	Analog Reference Capacitor	AGNDC	1.0	3.3		µF
C_{AGNDC2}	Analog Reference Capacitor	AGNDC		10		nF
Analog Audio Inputs						
V_{AI}	Analog Input Voltage AC	AUXL/R		0.525	1.05	V_{rms}
Analog Filter Input and Output						
Z_{AFLO}	Analog Filter Load Output[1)]	FOUTL/R	7.5		6	kΩ pF
Z_{AFLI}	Analog Filter Load Input[1)]	FINL/R	5.0		7.5	kΩ pF
Analog Audio Output						
Z_{AOL_HP}	Analog Output Load HP (47 Ω Series Resistor required)	OUTL/R		32 400		Ω pF

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
Quartz Characteristics						
T_{AC}	Ambient Temperature Range		0		70	°C
F_P	Load Resonance Frequency at C_l = 20 pF			12		MHz
$\Delta F/F_s$	Accuracy of Adjustment		–20		20	ppm
$\Delta F/F_s$	Frequency Variation versus Temperature		–20		20	ppm
R_{EQ}	Equivalent Series Resistance			12	30	Ω
C_0	Shunt (parallel) Capacitance			3	5	pF
Voltage Regulator						
C_{VREG1}	Voltage Regulator Capacitor	VREG	1.0	3.3		µF
C_{VREG2}	Voltage Regulator Capacitor	VREG		10		nF
Transceiver						
R_{USB}	Input Serial Resistance	DPLUS/ DMINUS	24 (±0.5 %)			Ω
C_{USB}	Shunt Capacitor	DPLUS/ DMINUS	22			pF

[1] Please refer to Section 4.1. “Recommended Low-Pass Filters for Analog Outputs” on page 26.

3.6.3. Characteristics

At T_A = 0 to 70 °C, V_{SUPD} = 4.75 V to 5.25 V, V_{SUPA} = 4.75 V to 5.25 V; typical values at T_J = 27 °C, V_{SUPD} = V_{SUPA} = 5.0 V, quartz frequency = 12 MHz, duty cycle = 50 %, positive current flows into the IC bass/treble: 0 dB, bass boost: off, AGC: off, equalizer: off

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Digital Supply							
I_{VDD}	Current Consumption[1)]	VDD		100	125.5	mA	V_{SUPD}=5 V
Digital Input Pin – Leakage							
I_I	Input Leakage Current	GPIO[7:0], AUXEN, RESQ			±1	µA	$V_{GND} \le V_I \le V_{SUP}$
Digital Output Pin							
V_{OH}	Output High Voltage	GPIO[7:0], SUSPEND, SOF	V_{SUPD} – 0.4			V	I_{out}=8 mA
V_{OL}	Output Low Voltage				0.4	V	
Analog Supply							
I_{AVDD}	Current Consumption Analog Audio			11 2	15	mA mA	SUSPD = 0, Mute SUSPD = 1, Mute
$PSRR_{AA}$	Power Supply Rejection Ratio for Analog Audio Output	AVDD0/1, OUTL/R		50		dB	1 kHz sine at 100 mV_{rms}
				20		dB	≤ 100 kHz sine at 100 mV_{rms}
Reference Frequency Generation							
V_{DCXTI}	DC Voltage at Oscillator Pins	XTI/O		0.5 * V_{SUPA}		V	
C_{LI}	Input Capacitance at Oscillator Pin	XTI		3		pF	
C_{LO}	Input Capacitance at Oscillator Pin	XTO		3		pF	
$V_{XTALOUT}$	Voltage Swing at Oscillator Pins (peak-peak)	XTI/O	0.6 * V_{SUPA}		1.0 * V_{SUPA}	V	
	Oscillator Start-Up Time				10	ms	
EEPROM							
	EEPROM unpowered data retention			10		year	
	Number of write cycles			100			

[1)] no load attached to GPIO's

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
USB Transceiver							
V_{REG}	Regulator Voltage	VREG	3.25	3.4	3.55	V	C_L=1µF
R_O	Driver Output Resistance including the 24-Ω external serial resistor	DPLUS/ DMINUS	28		43	Ω	static, LOW or HIGH
t_r / t_f	Rise and Fall Times	DPLUS/ DMINUS	4		20	ns	C_L=50 pF, driver mode
MA_TRTF	Rise/Fall Time Matching	DPLUS/ DMINUS	90		111.1	%	C_L=50 pF, driver mode
V_{XOVER}	Crossover Voltage	DPLUS/ DMINUS	1.3		2.0	V	C_L=50 pF, driver mode
V_{CM_DREC}	Differential Receiver Common-Mode Range	DPLUS/ DMINUS	0.8		2.5	V	
V_{T_SREC}	Single-ended Receiver Threshold Voltage	DPLUS/ DMINUS	0.8		2.0	V	
Analog Audio							
V_{AGNDC}	Analog Reference Voltage	AGNDC		2.25		V	R_L >> 10 MΩ, referred to VREF
R_{IAUX}	Input Resistance at Input Pins	AUXL/R	12.1 11.6	15	17.9 19.0	kΩ kΩ	T_J = 27 °C T_A = 0 to 70 °C Input selected, SUSPD = 0 i = ± 10 µA, referred to VREF
			24.2 23.3	30	35.8 37.9	kΩ kΩ	T_J = 27 °C T_A = 0 to 70 °C Input not selected SUSPD = 1 i = ± 10 µA, referred to VREF
R_{OOUT}	Output Resistance at Output Pins	OUTL/R		700		Ω	T_J = 27 °C SUSPD = 1 i = ± 200 µA, referred to VREF
R_{OFILT}	Output Resistance of Filter Pins	FINL		15		kΩ	SUSPD = 1, Mute i = ± 10 µA, referred to VREF
		FINR		11.25		kΩ	
V_{OffI}	Offset Voltage at Input Pins	AUXL/R	–20		20	mV	SUSPD = 0, referred to AGNDC
V_{OffO}	Offset Voltage at Output Pins	OUTL/R	–10		10	mV	SUSPD = 0, Mute referred to AGNDC
V_{OffFI}	Offset Voltage at Filter Output Pins	FOUTL/R	–20		20	mV	SUSPD = 0, referred to AGNDC
V_{OffFO}	Offset Voltage at Filter Input Pins	FINL/R	–20		20	mV	SUSPD = 0, referred to AGNDC
dV_{DCPD}	Difference of DC Voltage at Output Pins after Back-end Low Power Sequence	OUTL/R	–10		10	mV	Analog Gain = Mute, SUSPD switched from 0 to 1

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
$R_{D/A}$	D/A Pass Band Ripple	OUTL/R, FOUTL/R		0.01		dB	0...22 kHz (no external filters used)
$A_{D/A}$	D/A Stop Band Attenuation			60		dB	31 kHz...164 kHz (no external filters used)
BW_{AUX}	Bandwidth for Auxiliary Inputs	AUXL/R, FINL/R		760		kHz	
THD_{HP}	Total Harmonic Distortion	OUTL/R			0.05	%	BW = 20 Hz...0.5 fs, unweighted, $R_L \geq 32\ \Omega$ (47 Ω series resistor required), Analog Gain = 0 dB, Input 1 kHz at –3 dBFS
SNR_{AUX}	Signal-to-Noise Ratio from Analog Input to Outputs	AUXn, OUTL/R		96		dB	input –40 dB below 1.05 V_{rms}
SNR_1	Signal-to-Noise Ratio	OUTL/R	89	91		dB	$R_L \geq 32\ \Omega$ (external 47 Ω series resistor required) BW =20 Hz...0.5 fs unweighted, Analog Gain = 0 dB, Input = –20 dBFS
SNR_2	Signal-to-Noise Ratio	OUTL/R	58	62		dB	$R_L \geq 32\ \Omega$ (external 47 Ω series resistor required) BW = 20 Hz..0.5 fs unweighted Analog Gain = –40.5 dB, Input = –3 dBFS
Lev_{Mute}	Mute Level	OUTL/R		–110		dBV	BW = 20 Hz...22 kHz unweighted, no digital input signal, Analog Gain = Mute
V_{AO}	Analog Output Voltage AC	OUTL/R	1.0	1.05	1.1	V_{rms}	$R_L > 5\ k\Omega$, Analog Gain = 0 dB Input = 0 dBFS digital
G_{AUX}	Gain from Auxiliary Inputs to Outputs	AUXL/R, OUTL/R	–0.5	0	0.5	dB	f = 1 kHz, sine wave, $R_L > 5\ k\Omega$ 0.5 V_{rms} to AUXL/R
P_{HP}	Output Power (Headphone)	OUTL/R		12		mW	$R_L = 32\ \Omega$, Analog Gain = +2 dB, distortion < 1%, external 47 Ω series resistor required

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
G_{AO}	Analog Output Gain Setting Range	OUTL/R	–75		18	dB	
dG_{AO1}	Analog Output Gain Step Size	OUTL/R		3.0		dB	Analog Gain: –75 dB...-54 dB
dG_{AO2}	Analog Output Gain Step Size	OUTL/R		1.5		dB	Analog Gain: –54 dB...+18 dB
E_{GA1}	Analog Output Gain Error	OUTL/R	–2		2	dB	Analog Gain = –54 dB
E_{GA2}	Analog Output Gain Error	OUTL/R	–1		1	dB	Analog Gain = –45 dB
E_{GA3}	Analog Output Gain Error	OUTL/R	–0.5		0.5	dB	Analog Gain = –39 dB
E_{dGA}	Analog Output Gain Step Size Error	OUTL/R	–0.5		0.5	dB	Analog Gain = –48 dB
$XTALK_{HP}$	Crosstalk Left/Right Channel (Headphone)	OUTL/R	–70	–80		dB	f = 1 kHz, sine wave, OUTL/R: $R_L \geq 32\ \Omega$ (47 Ω series resistor required) Analog Gain = 0 dB, Input = –3 dBFS or 0.7 V_{rms} to AUXL/R
$XTALK_2$	Crosstalk between Input Signal Pairs	AUXnL/R	–70	–80		dB	f = 1 kHz, sine wave, FOUTL/R: $R_L > 7.5\ k\Omega$ OUTL/R: $R_L \geq 32\ \Omega$ (47-Ω series resistor required) Analog Gain = 0 dB, Input = –3 dBFS and 0.7 V_{rms} to AUXL/R

4. Applications

4.1. Recommended Low-Pass Filters for Analog Outputs [1)]

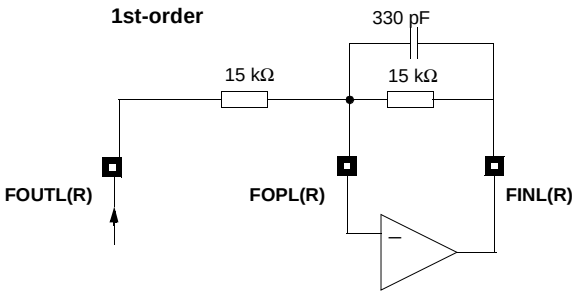

Fig. 4–1: 1st-order low-pass filter

Table 4–1: Attenuation of 1st-order low-pass filter

Frequency	Gain
24 kHz	–2.2 dB
30 kHz	–3.0 dB

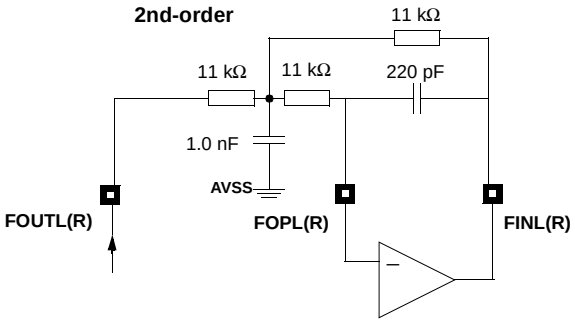

Fig. 4–2: 2nd-order low-pass filter

Table 4–2: Attenuation of 2nd-order low-pass filter

Frequency	Gain
24 kHz	–1.5 dB
30 kHz	–3.0 dB

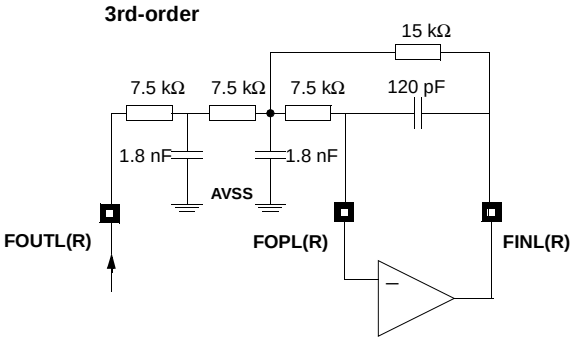

Fig. 4–3: 3rd-order low-pass filter

Table 4–3: Attenuation of 3rd-order low-pass filter

Frequency	Gain
18 kHz	0.17 dB
24 kHz	–0.23 dB
30 kHz	–3.00 dB

[1)] without deemphasis circuit

4.2. Typical Application

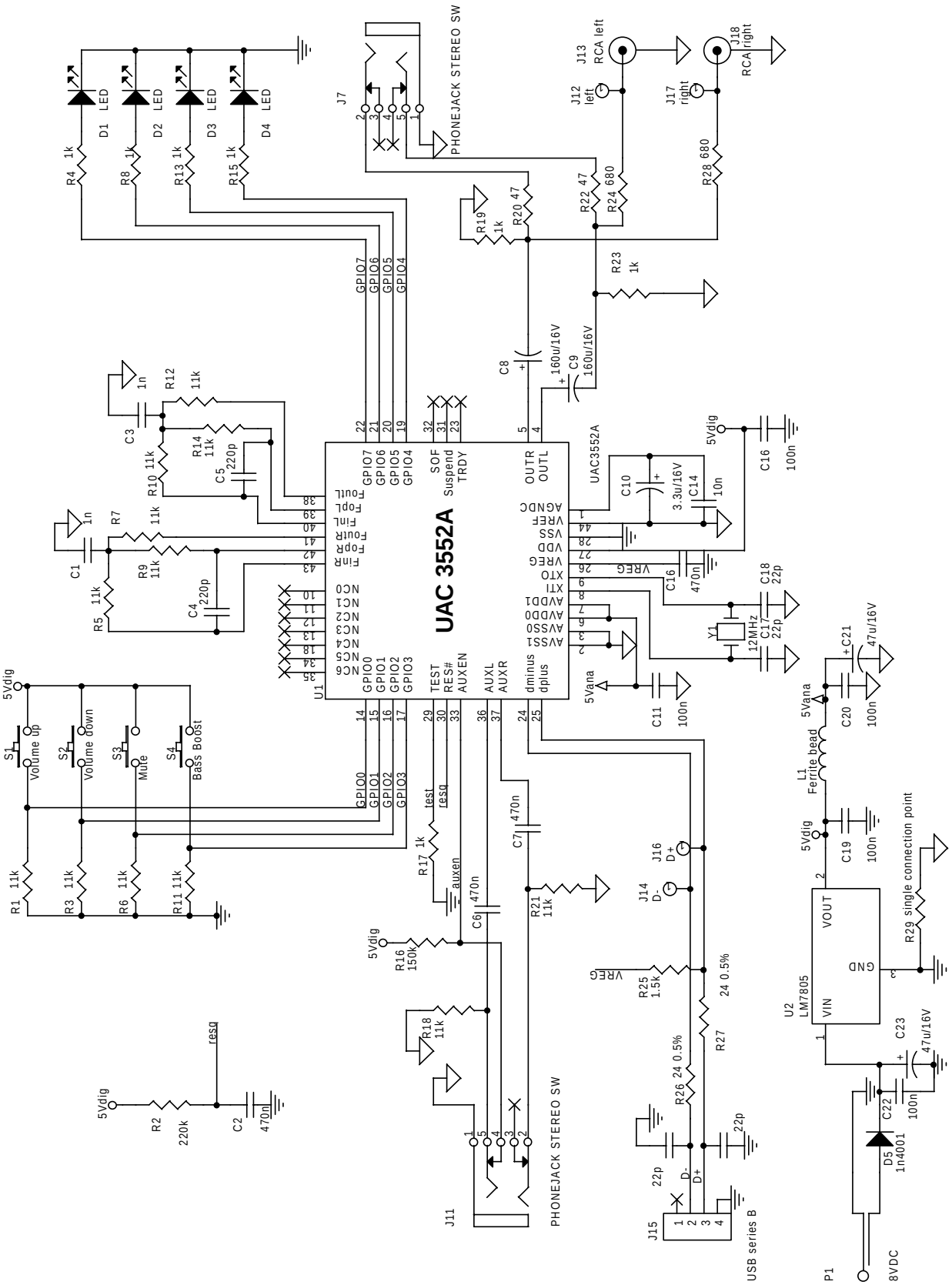

Fig. 4–4: Application circuit

5. Data Sheet History

1. Preliminary data sheet: “UAC 3552A Universal Serial Bus DAC, Nov. 9, 1999, 6251-487-1PD. First release of the preliminary data sheet.

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