

IN74HC299

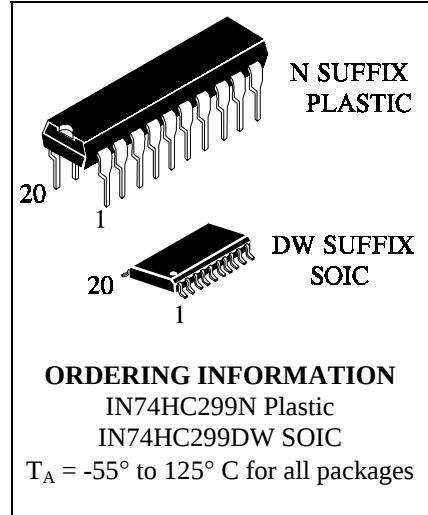
8-Bit Bidirectional Universal Shift Register with Parallel I/O High-Performance Silicon-Gate CMOS

The IN74HC299 is identical in pinout to the LS/ALS299. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

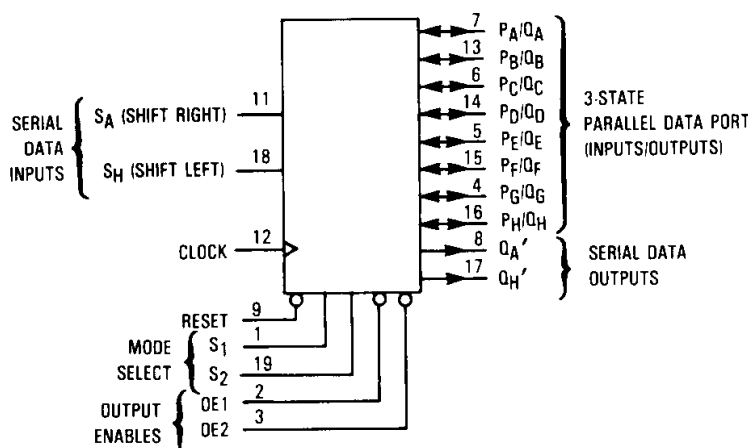
The IN74HC299 features a multiplexed parallel input/output data port to achieve full 8-bit handling in a 20 pin package. Due to the large output drive capability and the 3-state feature, this device is ideally suited for interface with bus lines in a bus-oriented system.

Two Mode-Select inputs and two Output Enable inputs are used to choose the mode of operation as listed in the Function Table. Synchronous parallel loading is accomplished by taking both Mode-Select lines, S_1 and S_2 , high. This places the outputs in the high-impedance state, which permits data applied to the data port to be clocked into the register. Reading out of the register can be accomplished when the outputs are enabled. The active-low asynchronous Reset overrides all other inputs.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices



LOGIC DIAGRAM



PIN 20 = V_{CC}
PIN 10 = GND

PIN ASSIGNMENT

S_1	1	20	V_{CC}
$OE1$	2	19	S_2
$OE2$	3	18	S_H
P_G/Q_G	4	17	Q_H'
P_E/Q_E	5	16	P_H/Q_H
P_C/Q_C	6	15	P_F/Q_F
P_A/Q_A	7	14	P_D/Q_D
Q_A'	8	13	P_B/Q_B
RESET	9	12	CLOCK
GND	10	11	S_A

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{IN}	DC Input Current, per Pin	± 20	mA
I_{OUT}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1) $V_{CC} = 2.0\text{ V}$ $V_{CC} = 4.5\text{ V}$ $V_{CC} = 6.0\text{ V}$	0 0 0	1000 500 400	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 µA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V _{IL}	Maximum Low - Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 µA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 20 µA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 6.0 mA (P/Q) I _{OUT} ≤ 7.8 mA (P/Q)	4.5 6.0	3.98 5.48	3.84 5.34	3.7 5.2	
		V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA (Q') I _{OUT} ≤ 5.2 mA (Q')	4.5 6.0	3.98 5.48	3.84 5.34	3.7 5.2	
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} = V _{IL} or V _{IH} I _{OUT} ≤ 20 µA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 6.0 mA (P/Q) I _{OUT} ≤ 7.8 mA (P/Q)	4.5 6.0	0.26 0.26	0.33 0.33	0.4 0.4	
		V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA (Q') I _{OUT} ≤ 5.2 mA (Q')	4.5 6.0	0.26 0.26	0.33 0.33	0.4 0.4	
I _{IN}	Maximum Input Leakage Current	V _{IN} =V _{CC} or GND	6.0	±0.1	±1.0	±1.0	µA
I _{OZ}	Maximum Three-State Leakage Current (Q _A thru Q _H)	Output in High-Impedance State V _{IN} = V _{IL} or V _{IH} V _{OUT} =V _{CC} or GND	6.0	±0.5	±5.0	±10	µA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} =V _{CC} or GND I _{OUT} =0µA	6.0	8.0	80	160	µA

AC ELECTRICAL CHARACTERISTICS($C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

Symbol	Parameter	V _{CC}	Guaranteed Limit			Unit
		V	25 °C to -55°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 5)	2.0 4.5 6.0	5.0 25 29	4.0 20 24	3.4 17 20	MHz
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q _A ’ or Q _H ’ (Figures 1 and 5)	2.0 4.5 6.0	170 34 29	215 43 37	255 51 43	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q _A thru Q _H (Figures 1 and 5)	2.0 4.5 6.0	160 32 27	200 40 34	240 48 41	ns
t _{PHL}	Maximum Propagation Delay, Reset to Q _A ’ or Q _H ’ (Figures 2 and 5)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t _{PHL}	Maximum Propagation Delay, Reset to Q _A thru Q _H (Figures 2 and 5)	2.0 4.5 6.0	190 38 32	240 48 41	285 57 48	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay , OE1, OE2, S1, or S2 to Q _A thru Q _H (Figures 3 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay , OE1, OE2, S1, or S2 to Q _A thru Q _H (Figures 3 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Q _A thru Q _H (Figures 1 and 5)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Q _A ’ thru Q _H ’ (Figures 1 and 5)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{IN}	Maximum Input Capacitance)	-	10	10	10	pF
C _{OUT}	Maximum Three-State I/O Capacitance (I/O in High-Impedance State), Q _A thru Q _H	-	15	15	15	pF

C _{PD}	Power Dissipation Capacitance (Per Package), Output Enable	Typical @25°C,V _{CC} =5.0 V			pF
	Used to determine the no-load dynamic power consumption: P _D =C _{PD} V _{CC} ² f+I _{CC} V _{CC}	240			

TIMING REQUIREMENTS($C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25 °C to-55°C	≤85°C	≤125°C	
t_{su}	Minimum Setup Time, Mode Select S1 or S2 to Clock (Figure 4)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t_{su}	Minimum Setup Time, Data Inputs S _A , S _H , P _A thru P _H to Clock (Figure 4)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t_h	Minimum Hold Time, Clock to Mode Select S1 or S2 (Figure 4)	2.0	120	150	180	ns
		4.5	24	30	36	
		6.0	20	26	31	
t_h	Minimum Hold Time, Clock to Data Inputs, S _A , S _H , P _A thru P _H (Figure 4)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

FUNCTION TABLE

Inputs									Response									
Mode	Reset	Mode Select		Output Enables		Clock	Serial Inputs		P _A /Q _A	P _B /Q _B	P _C /Q _C	P _D /Q _D	P _E /Q _E	P _F /Q _F	P _G /Q _G	P _H /Q _H	Q _A '	Q _H '
		S ₂	S ₁	OE1 [↑]	OE2 [↑]		D _A	D _H										
Reset	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	Q _A through Q _H =Z								L	L
Shift Right	H	L	H	H	X		D	X	Shift Right: Q _A through Q _H =Z; D _A →F _A ; F _A →F _B ; etc								D	Q _G
	H	L	H	X	H		D	X	Shift Right: Q _A through Q _H =Z; D _A →F _A ; F _A →F _B ; etc								D	Q _G
	H	L	H	L	L		D	X	Shift Right: D _A →F _A =Q _A ; F _A →F _B =Q _B ; etc								D	Q _G
Shift Left	H	H	L	H	X		X	D	Shift Left: Q _A through Q _H =Z; D _H →F _H ; F _H →F _G ; etc								Q _B	D
	H	H	L	X	H		X	D	Shift Left: Q _A through Q _H =Z; D _H →F _H ; F _H →F _G ; etc								Q _B	D
	H	H	L	L	L		X	D	Shift Left: D _H →F _H =Q _H ; F _H →F _G =Q _G ; etc								Q _B	D
Parallel Load	H	H	H	X	X		X	X	Parallel Load: P _N →F _N								P _A	P _H
Hold	H	L	L	H	X	X	X	X	Hold: Q _A through Q _H =Z; F _N =F _N								P _A	P _H
	H	L	L	X	H	X	X	X	Hold: Q _A through Q _H =Z; F _N =F _N								P _A	P _H
	H	L	L	L	L	X	X	X	Hold: Q _N =Q _H								P _A	P _H

Z = high impedance

D = data on serial input

F = flip-flop (see Logic Diagram)

↑ When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

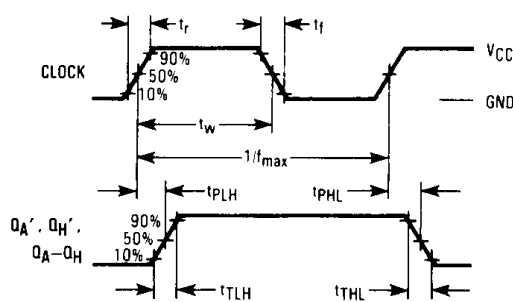


Figure 1. Switching Waveforms

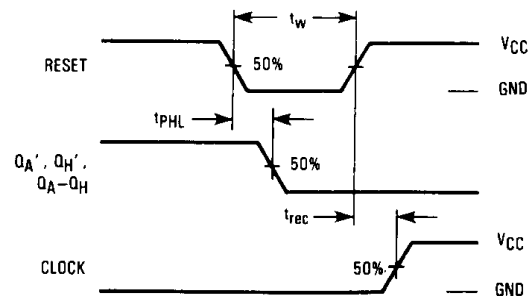


Figure 2. Switching Waveforms

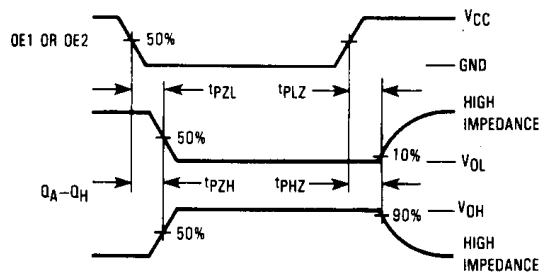


Figure 3a. Switching Waveforms

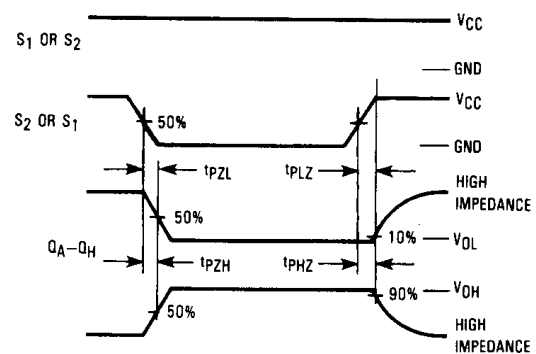


Figure 3b. Switching Waveforms

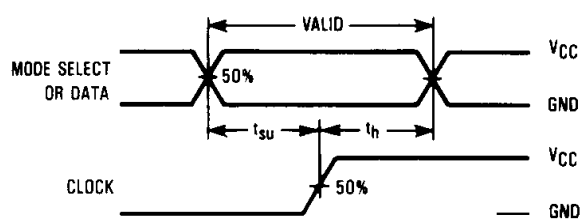
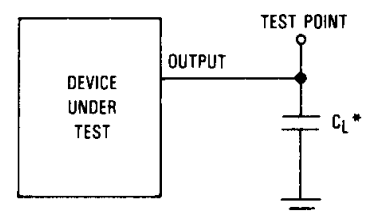
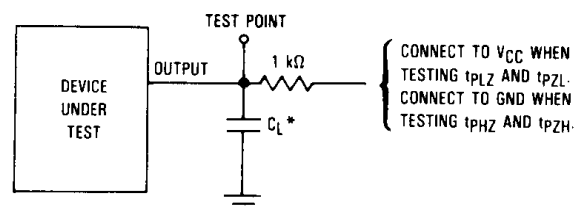


Figure 4. Switching Waveforms



*Includes all probe and jig capacitance.

Figure 5. Test Circuit



*Includes all probe and jig capacitance.

Figure 6. Test Circuit

EXPANDED LOGIC DIAGRAM

