

FEATURES

Low supply current: 250 μ A maximum
Very low input bias current: 1 pA maximum
Low offset voltage: 750 μ V maximum
Single-supply operation: 5 V to 26 V
Dual-supply operation: ± 2.5 V to ± 13 V
Rail-to-rail output
Unity-gain stable
No phase reversal

ENHANCED PRODUCT FEATURES

Supports defense and aerospace applications
 (AQEC standard)
Military temperature range (-55°C to $+125^{\circ}\text{C}$)
Controlled manufacturing baseline
1 assembly/test site
1 fabrication site
Enhanced product change notification
Qualification data available on request

APPLICATIONS

Line-/battery-powered instruments
Photodiode amplifiers
Precision current sensing
Precision filters
Portable audio

GENERAL DESCRIPTION

The AD8643-EP is a low power, precision JFET input amplifier featuring extremely low input bias current and rail-to-rail output. The ability to swing nearly rail-to-rail at the input and rail-to-rail at the output enables designers to buffer CMOS digital-to-analog converters (DACs), ASICs, and other wide output swing devices in single-supply systems. The outputs remain stable with capacitive loads of more than 500 pF.

PIN CONFIGURATION

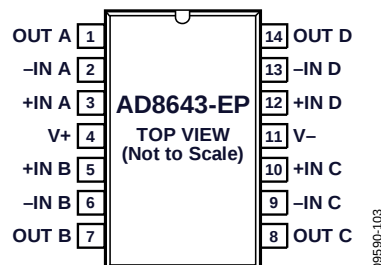


Figure 1. 14-Lead SOIC (R-14)

The AD8643-EP is suitable for applications using multichannel boards that require low power to manage heat. Other applications include photodiodes and battery management.

The AD8643-EP is fully specified over the military temperature range of -55°C to $+125^{\circ}\text{C}$. This device is available in a 14-lead SOIC.

Additional applications information is available in the [AD8643](#) data sheet.

Rev. 0

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REVISION HISTORY

1/11—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

$V_S = 5.0\text{ V}$, $V_{CM} = 2.5\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$-55^\circ\text{C} < T_A < +85^\circ\text{C}$ $+85^\circ\text{C} < T_A < +125^\circ\text{C}$, $V_{CM} = 1.5\text{ V}$		50	1000 1.8 1.9	μV mV mV
Input Bias Current	I_B	$-55^\circ\text{C} < T_A < +125^\circ\text{C}$		0.25	1	pA
Input Offset Current	I_{OS}	$-55^\circ\text{C} < T_A < +125^\circ\text{C}$			180	pA
Input Voltage Range		$-55^\circ\text{C} < T_A < +125^\circ\text{C}$	0		0.5	pA
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to } 2.5\text{ V}$	74	93	60	pA
Large Signal Voltage Gain	A_{VO}	$R_L = 10\text{ k}\Omega$, $V_O = 0.5\text{ to } 4.5\text{ V}$	80	140	3	V
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-55^\circ\text{C} < T_A < +125^\circ\text{C}$		2.5		$\mu\text{V}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_L = 1\text{ mA}$, $-55^\circ\text{C to } +125^\circ\text{C}$	4.95 4.94			V V
Output Voltage Low	V_{OL}	$I_L = 1\text{ mA}$, $-55^\circ\text{C to } +125^\circ\text{C}$			0.05	V
Output Current	I_{OUT}			0.01 ± 6	0.05	V mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 5\text{ V to } 26\text{ V}$	90	107		dB
Supply Current/Amplifier	I_{SY}	$-55^\circ\text{C} < T_A < +125^\circ\text{C}$		195	250 270	μA μA
DYNAMIC PERFORMANCE						
Slew Rate	SR			2		$\text{V}/\mu\text{s}$
Gain Bandwidth Product	GBP			2.5		MHz
Phase Margin	ϕ_m			50		Degrees
NOISE PERFORMANCE						
Voltage Noise	$e_N\text{ p-p}$	$f = 0.1\text{ Hz to } 10\text{ Hz}$		4.0		$\mu\text{V p-p}$
Voltage Noise Density	e_N	$f = 1\text{ kHz}$		28.5		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	i_N	$f = 1\text{ kHz}$		0.5		$\text{fA}/\sqrt{\text{Hz}}$

AD8643-EP

$V_S = \pm 13 \text{ V}$, $V_{CM} = 0 \text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$-55^\circ < T_A < +125^\circ\text{C}$		70	1000	μV
Input Bias Current	I_B	$-55^\circ\text{C} < T_A < +125^\circ\text{C}$		0.25	1	pA
Input Offset Current	I_{OS}	$-55^\circ\text{C} < T_A < +125^\circ\text{C}$			260	pA
Input Voltage Range		$-55^\circ\text{C} < T_A < +125^\circ\text{C}$			0.5	pA
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -13 \text{ V to } +10 \text{ V}$	-13		65	pA
Large Signal Voltage Gain	A_{VO}	$R_L = 10 \text{ k}\Omega$, $V_O = -11 \text{ V to } +11 \text{ V}$	90	107	+10	V
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-55^\circ\text{C} < T_A < +125^\circ\text{C}$	215	290		dB
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_L = 1 \text{ mA}$, $-55^\circ\text{C to } +125^\circ\text{C}$	12.95			V
Output Voltage Low	V_{OL}	$I_L = 1 \text{ mA}$, $-55^\circ\text{C to } +125^\circ\text{C}$	12.94		-12.95	V
Output Current	I_{OUT}			± 12	-12.94	V
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5 \text{ V to } \pm 13 \text{ V}$	90	107		dB
Supply Current/Amplifier	I_{SY}	$-55^\circ\text{C} < T_A < +125^\circ\text{C}$		200	290	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR			3		V/ μs
Gain Bandwidth Product	GBP			3.5		MHz
Phase Margin	ϕ_m			60		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_N p-p	$f = 0.1 \text{ Hz to } 10 \text{ Hz}$		4.2		$\mu\text{V p-p}$
Voltage Noise Density	e_N	$f = 1 \text{ kHz}$		27.5		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	i_N	$f = 1 \text{ kHz}$		0.5		fA/ $\sqrt{\text{Hz}}$

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
Supply Voltage	27.3 V
Input Voltage	V ₋ to V ₊
Differential Input Voltage	±Supply Voltage
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	–55°C to +125°C
Junction Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
14-Lead SOIC (R)	120	36	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

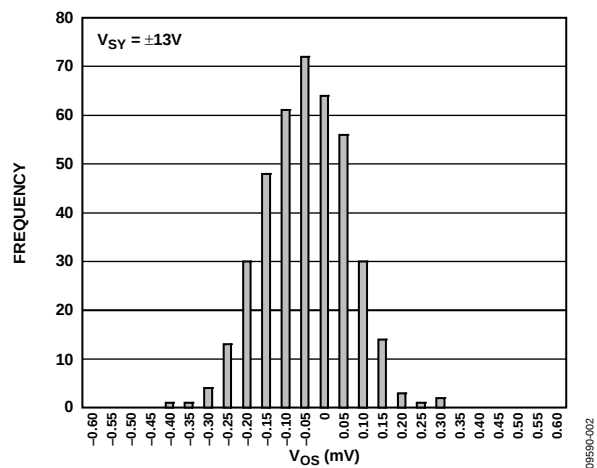


Figure 2. Input Offset Voltage

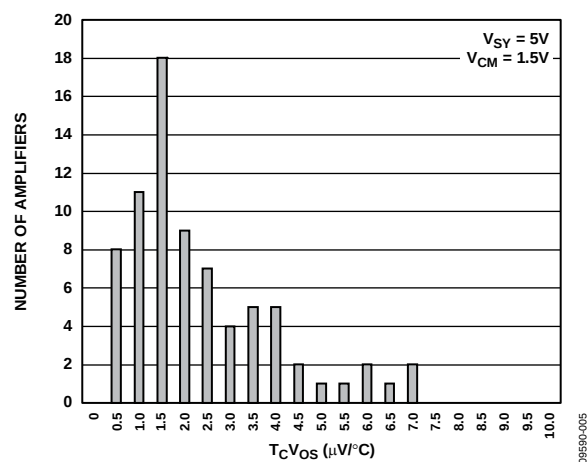


Figure 5. Offset Voltage Drift

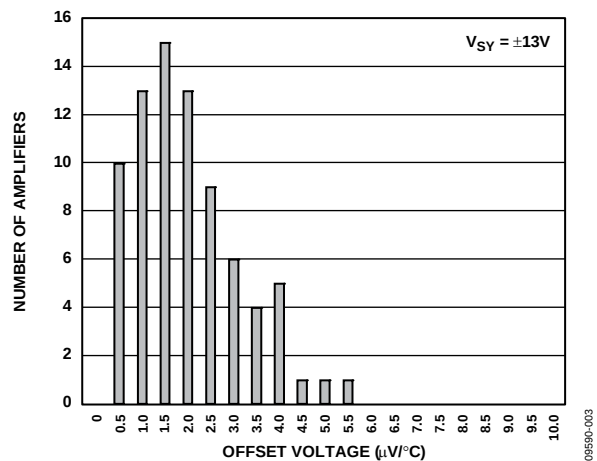


Figure 3. Offset Voltage Drift

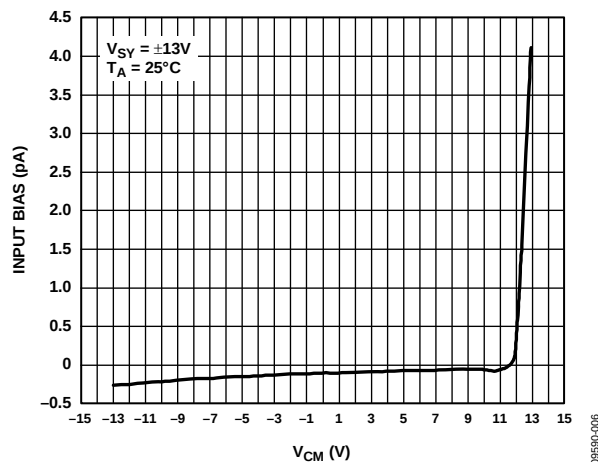


Figure 6. Input Bias Current vs. V_{CM}

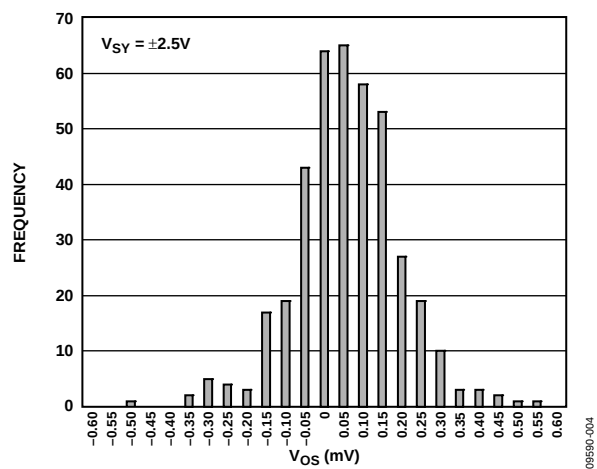


Figure 4. Input Offset Voltage

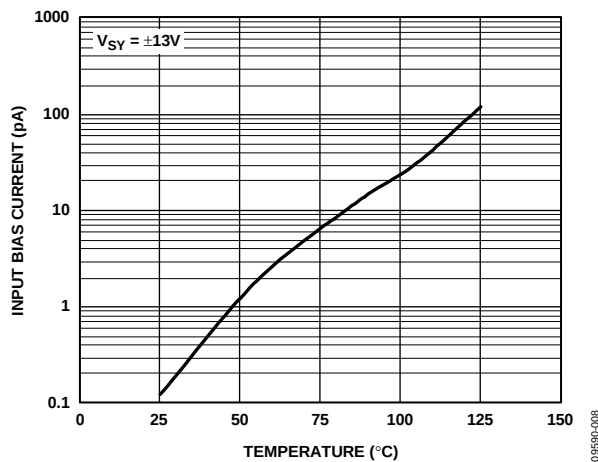


Figure 7. Input Bias Current vs. Temperature

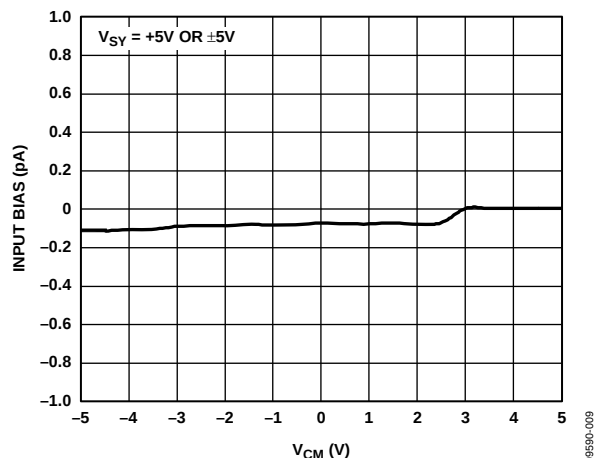


Figure 8. Input Bias Current vs. V_{CM}

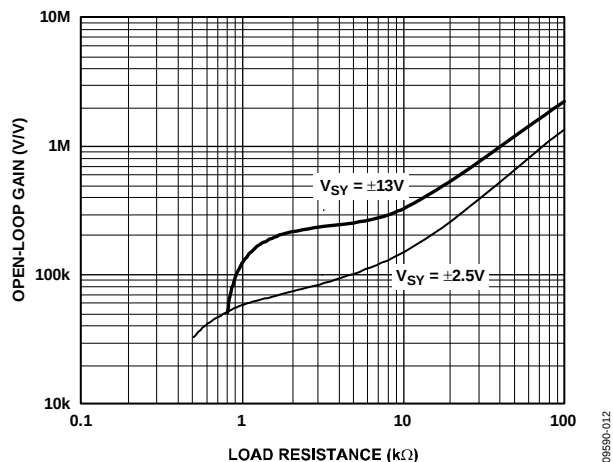


Figure 11. Open-Loop Gain vs. Load Resistance

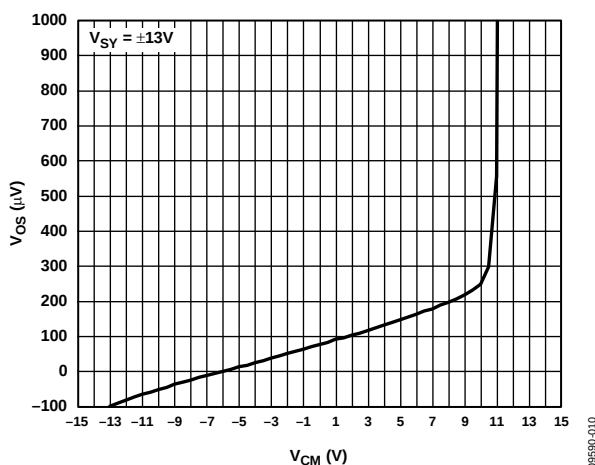


Figure 9. Input Offset Voltage (V_{OS}) vs. V_{CM}

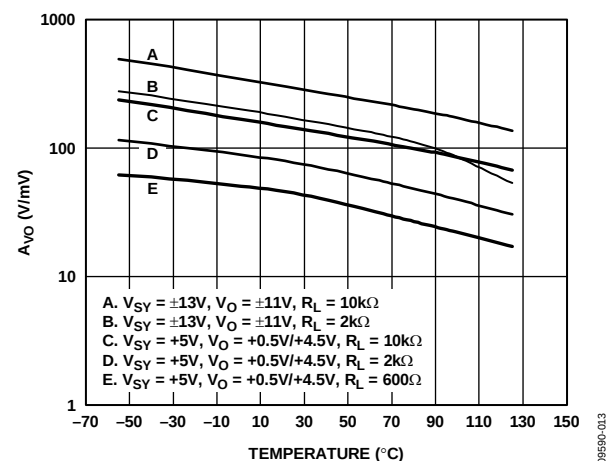


Figure 12. Open-Loop Gain vs. Temperature

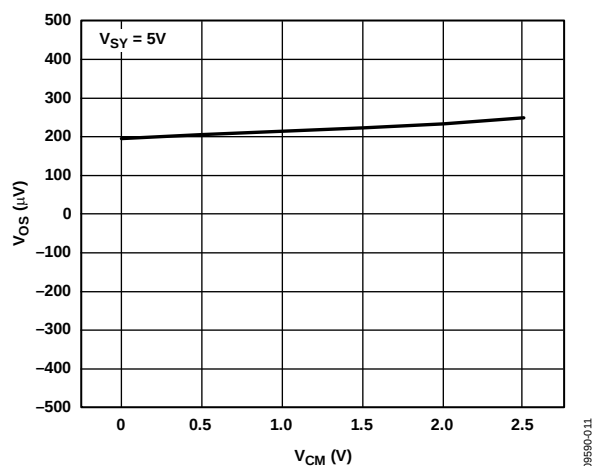


Figure 10. Input Offset Voltage vs. V_{CM}

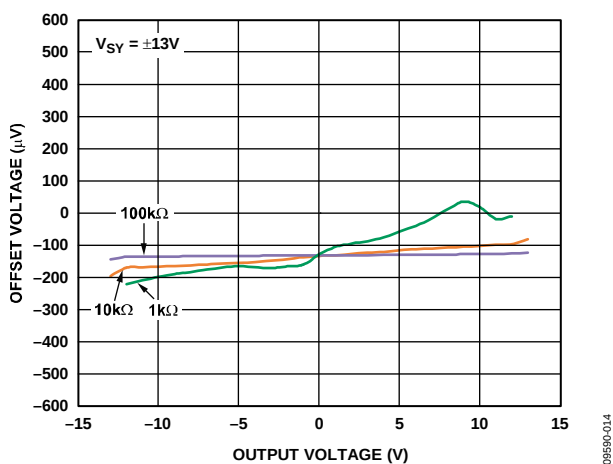


Figure 13. Input Error Voltage vs. Output Voltage for Resistive Loads

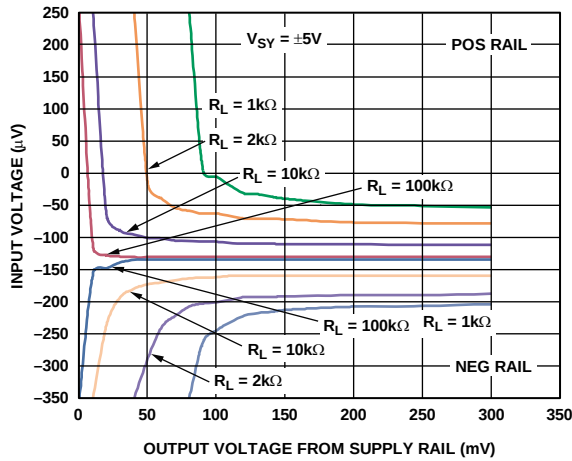


Figure 14. Input Error Voltage vs. Output Voltage Within 300 mV of Supply Rails

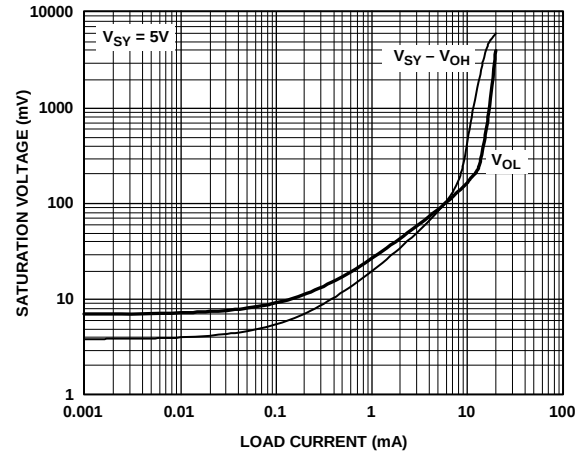


Figure 17. Output Saturation Voltage vs. Load Current

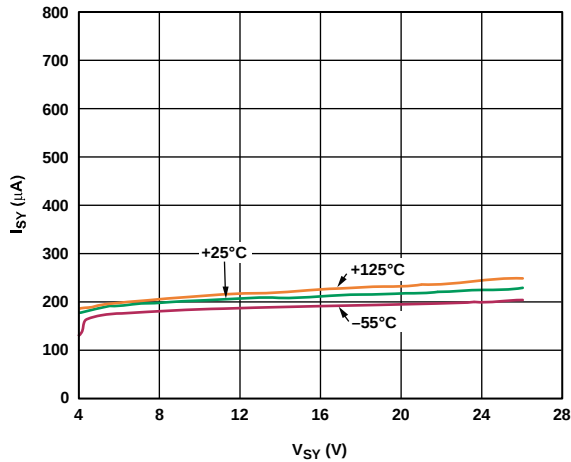


Figure 15. Quiescent Current vs. Supply Voltage at Different Temperatures

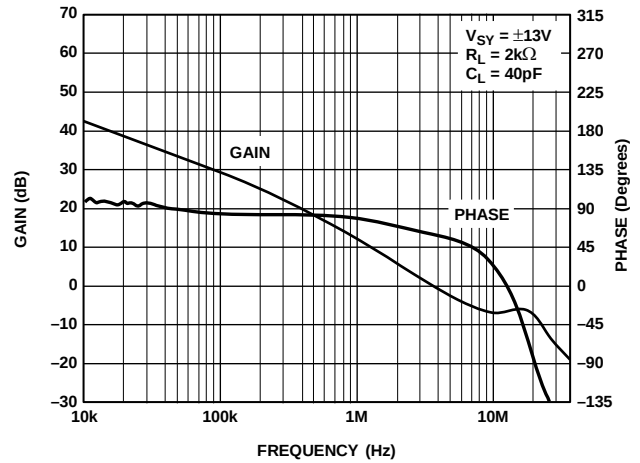


Figure 18. Open-Loop Gain and Phase Margin vs. Frequency

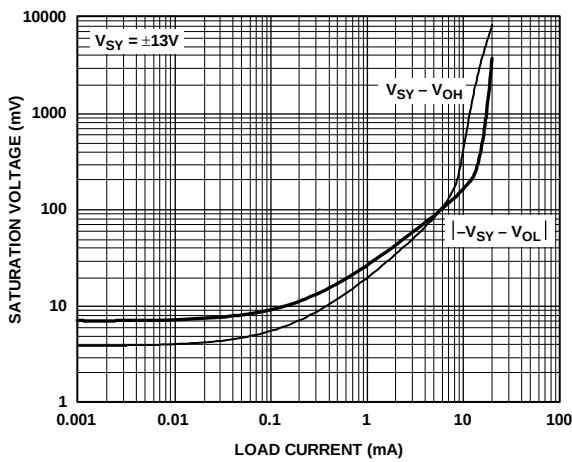


Figure 16. Output Saturation Voltage vs. Load Current

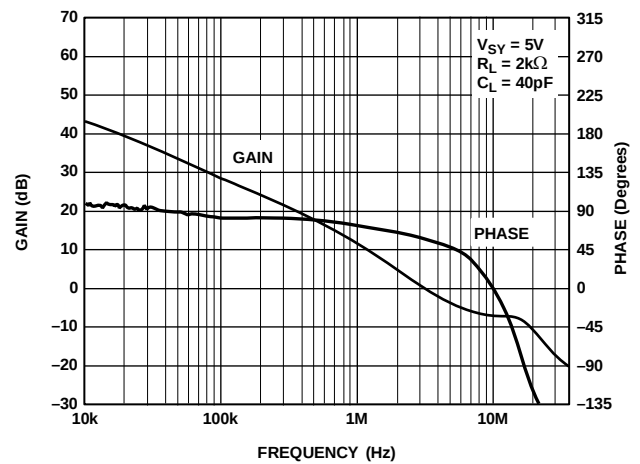


Figure 19. Open-Loop Gain and Phase Margin vs. Frequency

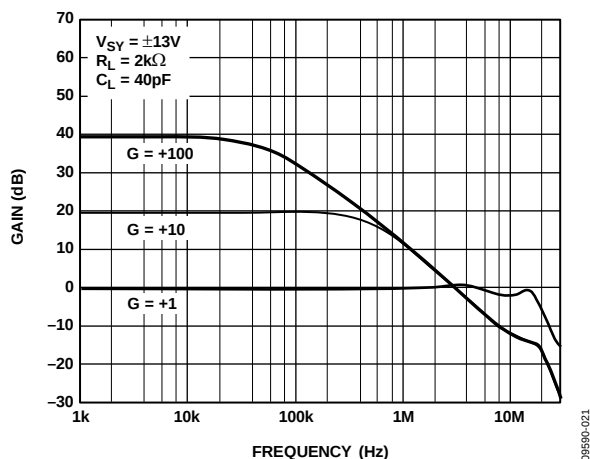


Figure 20. Closed-Loop Gain vs. Frequency

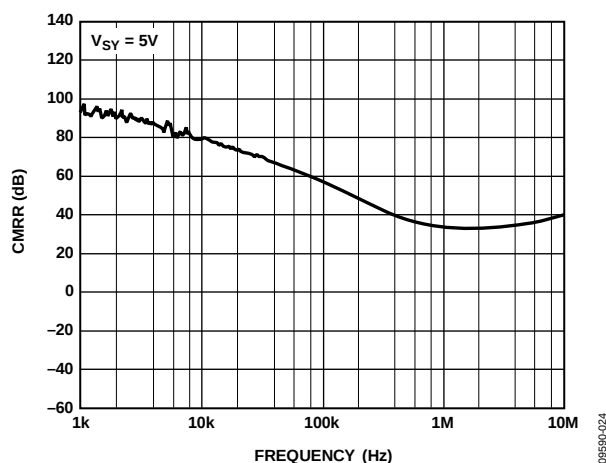


Figure 23. CMRR vs. Frequency

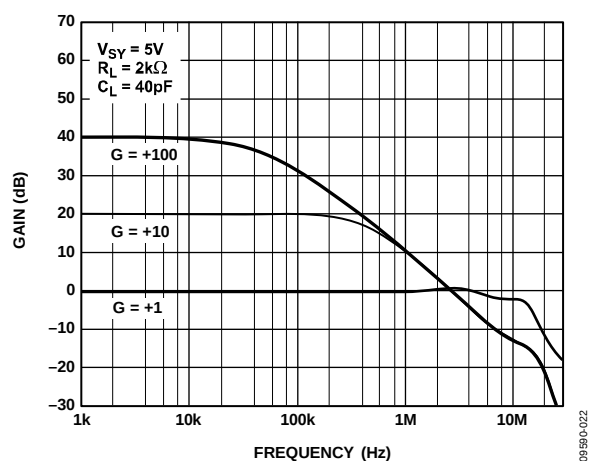


Figure 21. Closed-Loop Gain vs. Frequency

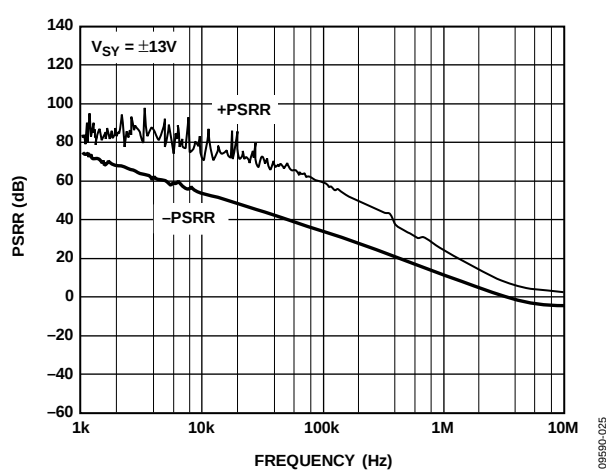


Figure 24. PSRR vs. Frequency

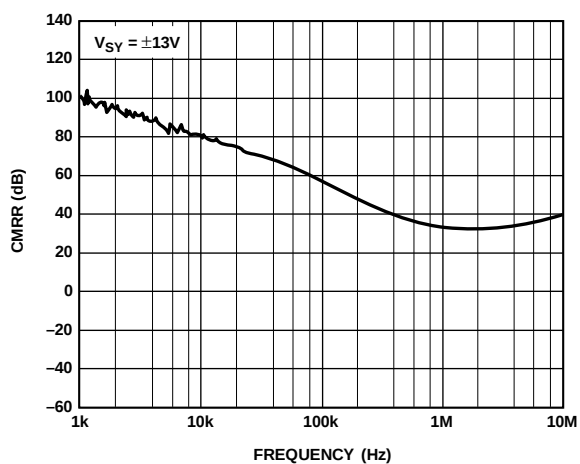


Figure 22. CMRR vs. Frequency

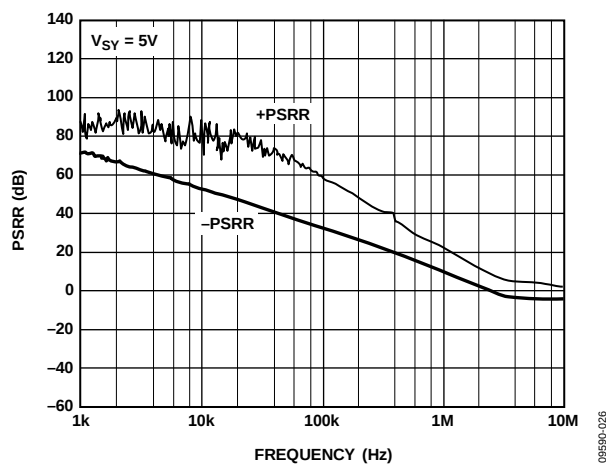


Figure 25. PSRR vs. Frequency

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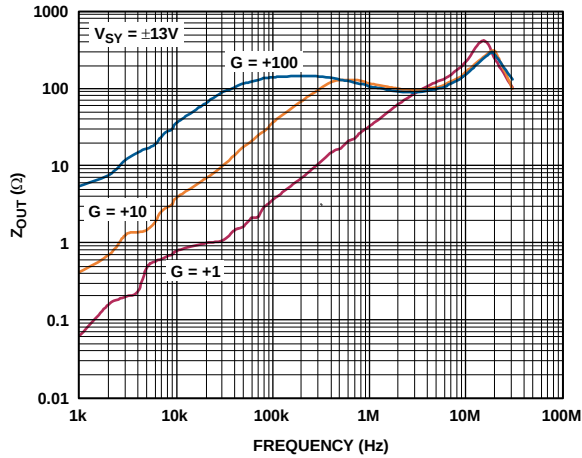


Figure 26. Output Impedance vs. Frequency

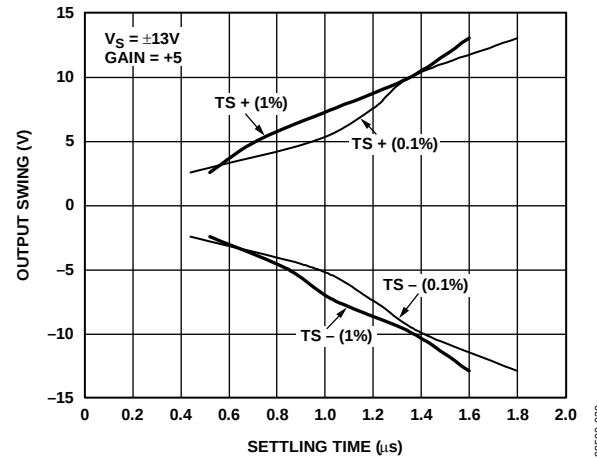


Figure 29. Output Swing and Error vs. Settling Time

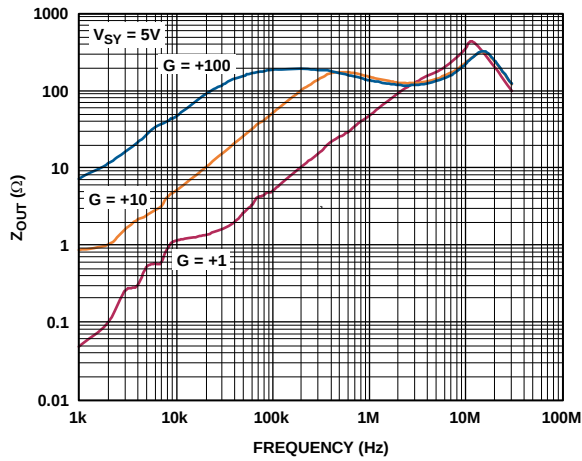


Figure 27. Output Impedance vs. Frequency

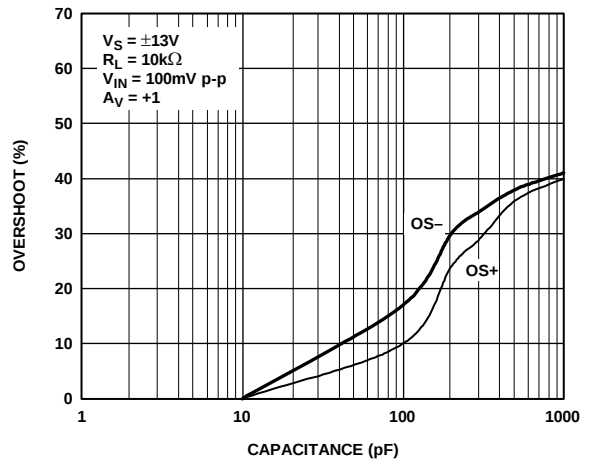


Figure 30. Small Signal Overshoot vs. Load Capacitance

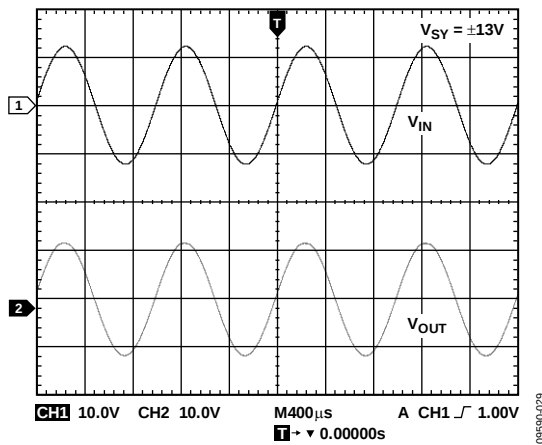


Figure 28. No Phase Reversal

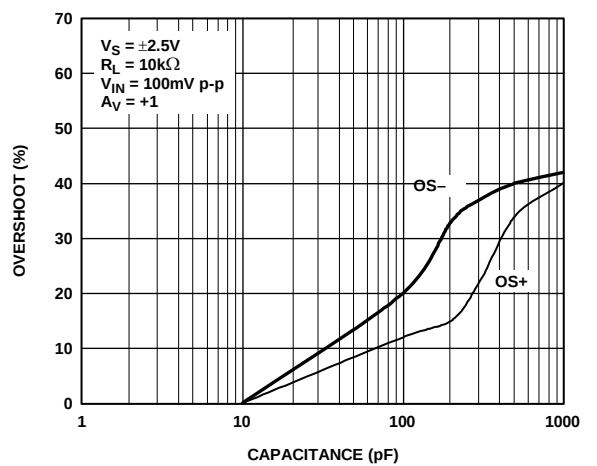


Figure 31. Small Signal Overshoot vs. Load Capacitance

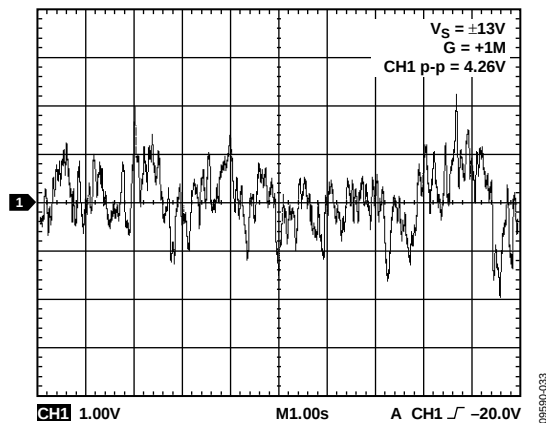


Figure 32. 0.1 Hz to 10 Hz Noise

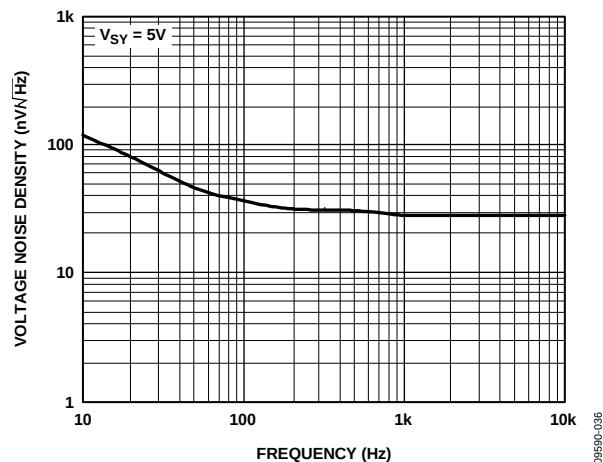


Figure 35. Voltage Noise Density

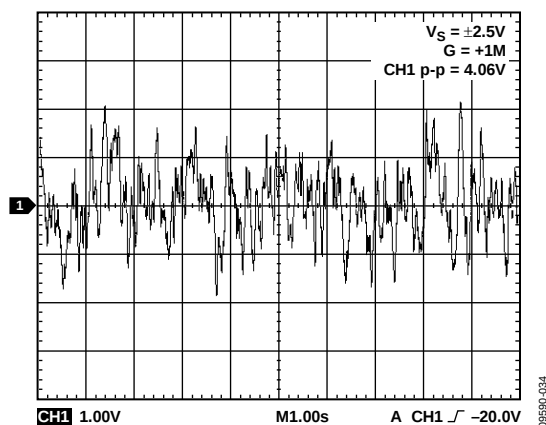


Figure 33. 0.1 Hz to 10 Hz Noise

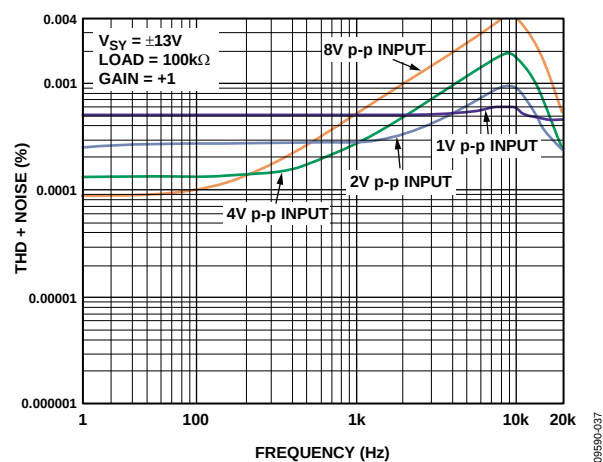


Figure 36. Total Harmonic Distortion + Noise vs. Frequency

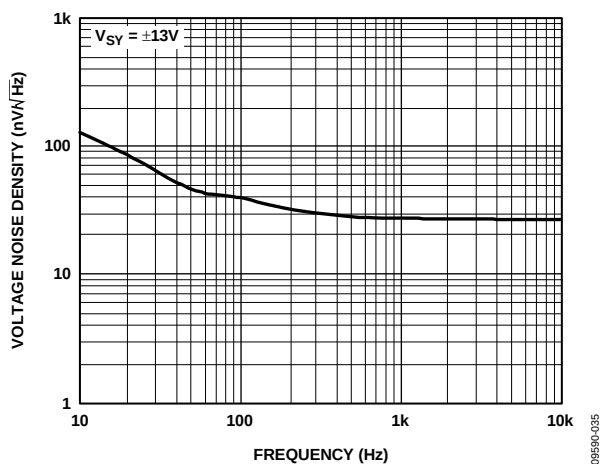


Figure 34. Voltage Noise Density

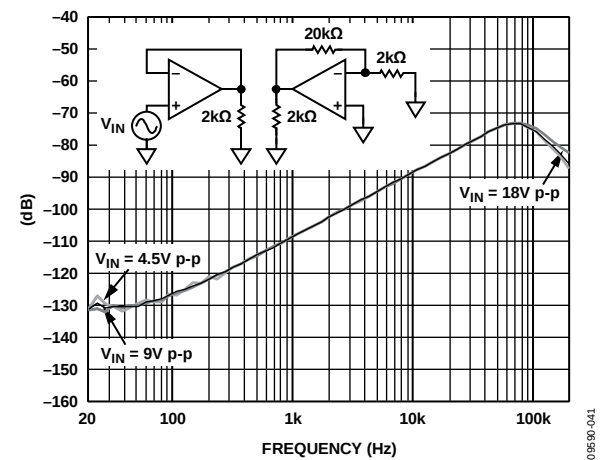
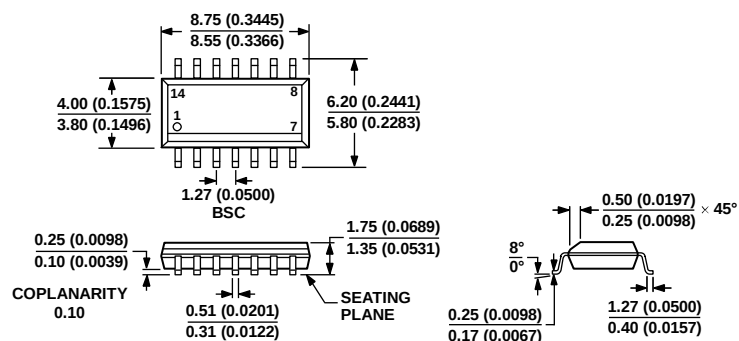


Figure 37. Channel Separation

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 38. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
AD8643TRZ-EP	−55°C to +125°C	14-lead SOIC_N	R-14
AD8643TRZ-EP-R7	−55°C to +125°C	14-lead SOIC_N	R-14

¹ Z = RoHS Compliant Part.