HI-8045

December 2001

CMOS HIGH VOLTAGE DISPLAY DRIVER

GENERAL DESCRIPTION

The HI-8045 high voltage display driver is a low cost plastic, 80-segment version of the Holt HI-8040 display driver series. The 20 mil package lead pitch allows the maximum number of display driver segments in the smallest space. All the features of the HI-8040 are available with the HI-8045. An optional negative converter can generate the negative display drive voltage. Test inputs facilitate opens and shorts testing. The backplane frequency is checked and, as long as power is available, the segments are shut "Off" if the frequency becomes too low.

The HI-8045 and the HI-80XX series of display drivers all control segment information in the same way. Data is serially clocked into the device and the data for all segment outputs are latched in parallel when the Load input transitions from high to low. With the Data Out from the shift register available, devices may be cascaded to obtain more segment outputs. The shift register is 85 bits long.

The die is metal mask programmable to provide for various package and/or cascade tap options. Consult your Holt Sales representative to explore the possibilities.

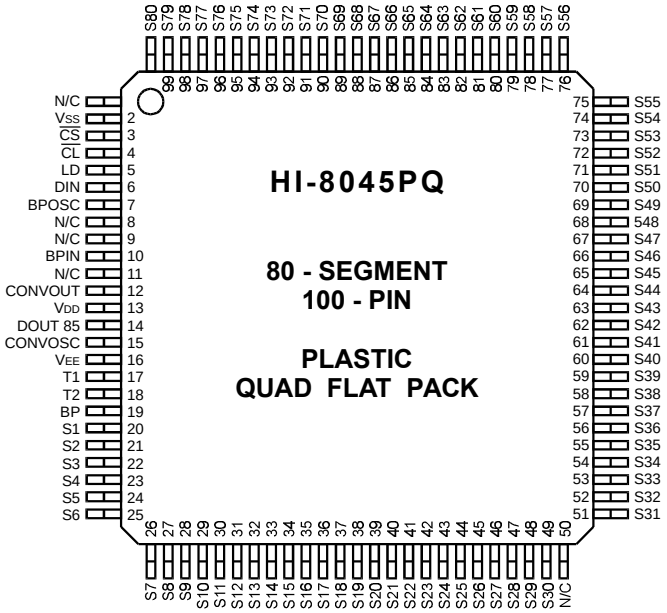
FEATURES

- 4 MHz serial input data rate
- 80 segment outputs
- Cascadable
- 5 Volt inputs translated to 35 Volts
- Test pins allow hardware all "ON", all "OFF" or alternating
- Monitors backplane oscillation and forces all segments to "OFF" condition if below 10Hz
- Negative voltage converter available on-chip
- CMOS low power
- Industrial and JEDEC processing available

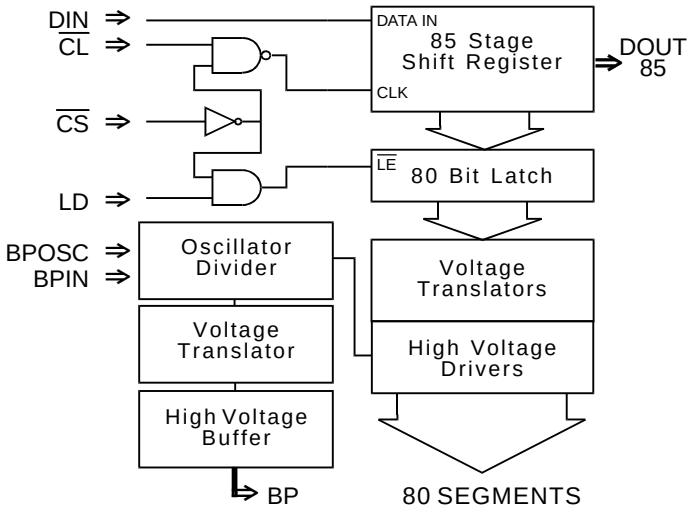
APPLICATIONS

- Dichroic Liquid Crystal Displays
- Standard Liquid Crystal Displays

PIN CONFIGURATION (Top View)



FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

INPUT LOGIC

$\overline{CS}$ must be held low to enter data into the shift register. The data is clocked on the negative edge of $\overline{CL}$. LD is normally held low and only pulsed high when new data is ready for display. When LD is high the latch is transparent. All four logic inputs are TTL compatible. A logic "1" at DIN that is eventually latched to the segment drivers will cause the segment to be at the opposite voltage level of the BP pin (out of phase).

BPOSC and BPIN

The user can either make an oscillator to create the backplane frequency or drive a signal into BPIN leaving BPOSC open. To make an oscillator, pins BPOSC and BPIN must be connected together and the appropriate R and C combination applied (See Figure 1). If the oscillator is used, the backplane frequency is approximately

$$f_{BP} = \frac{1}{256\ RC} \quad (\text{for } R = 180K\Omega\ \&\ C = 220pF,\ f_{BP} \approx 100Hz).$$

VEE & NEGATIVE VOLTAGE CONVERTER

VEE may be externally driven to a maximum -30V. Alternatively, there is a voltage converter that will provide -21.4 volts (See Figure 2). If the converter pins are left open circuit, an on-chip sense resistor will cause shut down of all current consumption associated with the converter. The converter will survive a shorted segment condition and continue to maintain VEE at -20 volts.

DOUT

The DOUT pin is available from segment 85 for cascading devices to drive more segments and for verifying the data integrity. However only the first 80 output segments are available to the user. This output can drive 2 TTL loads. It changes on the positive edge of $\overline{CL}$.

AUTOMATIC SEGMENTS OFF

The internal backplane signal is tested continuously to be at least 10Hz. If the detector senses f<10Hz, then the segments are forced to the same voltage as the backplane (all segments in "OFF" state). However, the detector is only functional while VDD is above the minimum operating voltage specification.

TEST INPUTS

The test functions available are:

T2	T1	Display
0	0	Normal
0	1	All Off
1	0	All On
1	1	Alternating On/Off Segments

The test inputs must be tied to the appropriate logic level for correct circuit operation.

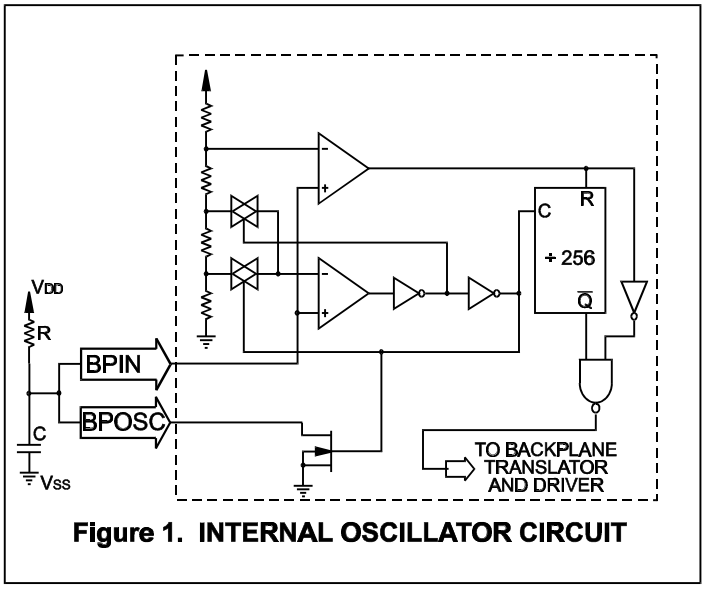


Figure 1. INTERNAL OSCILLATOR CIRCUIT

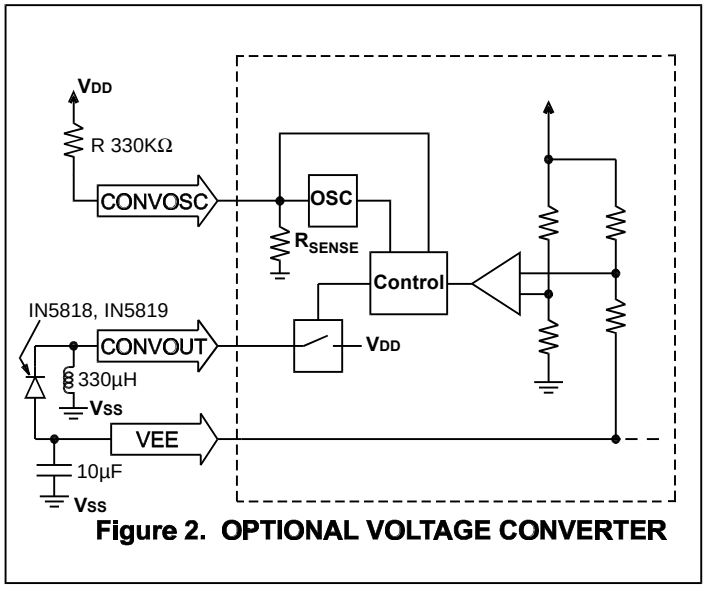


Figure 2. OPTIONAL VOLTAGE CONVERTER

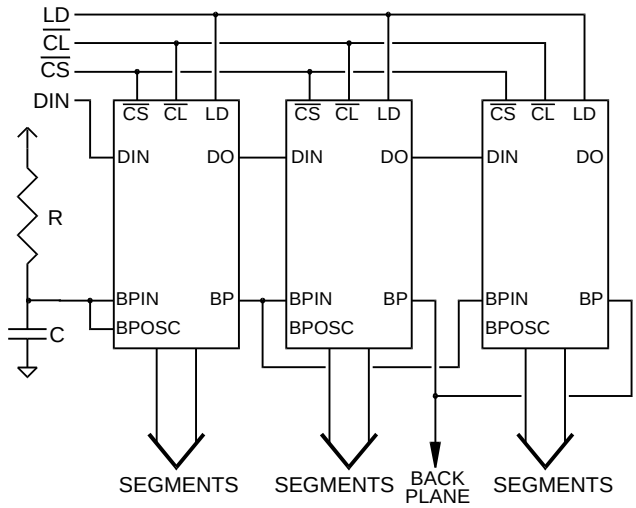


Figure 3. RC OSCILLATOR AND CASCADED DEVICES

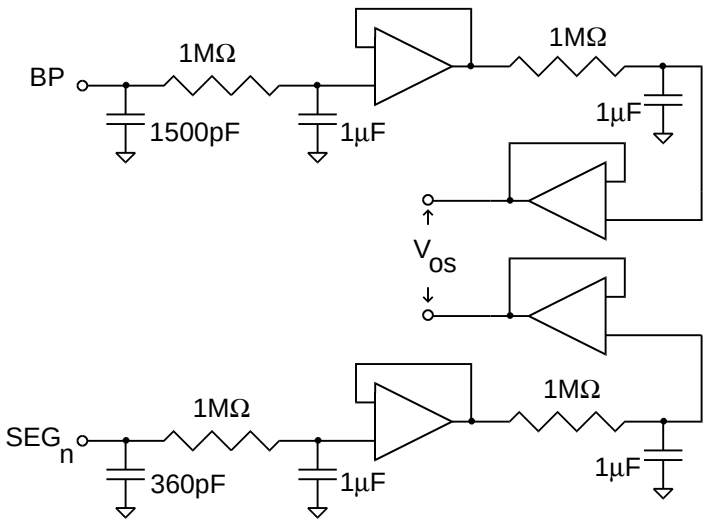


Figure 4. OFFSET MEASUREMENT

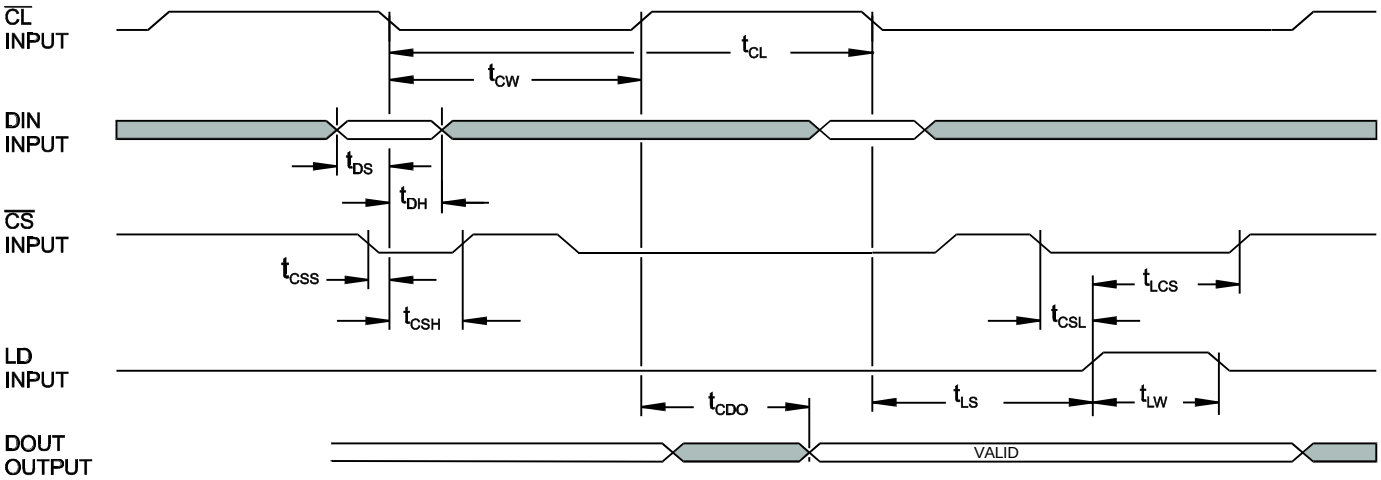


Figure 5. TIMING DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Voltages referenced to VSS = 0V

Supply Voltage VDD..... 0V to 7V VEE.....VDD-35V to 0V	Power Dissipation.....300 mW
Voltage at any input, except BPIN....-0.3 to VDD+0.3V	Operating Temperature Range - Industrial.....-40° to +85°C
Voltage at BPIN input.....VDD-35 to VDD+0.3V	Operating Temperature Range - Hi-Temp.....-55° to +125°C
DC Current any input pin.....10 mA	Storage Temperature Range.....-65° to +150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

VDD = 5V ±5%, VEE = -21.5V, VSS = 0V, TA = Operating temperature range (unless otherwise specified).

PARAMETER		SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Operating Voltage		VDD		3.0		7.0	V
Supply Current: (Converter Off, fBP = 100Hz)		IDD	Static, No Load			300	µA
		IEE	Static, No Load			120	µA
Input Low Voltage (excluding BPIN)		VIL		0		0.8	V
Input High Voltage (excluding BPIN)		VIH		2		VDD	V
Input Low Voltage (BPIN)		VILX		VEE		0.6 VDD	V
Input High Voltage (BPIN)		VIHX		0.8 VDD		VDD	V
Input Current		IIN	VIN = 0 to 5V			100	nA
Input Capacitance (Guaranteed, not tested)		CI				5	pF
Segment Output Impedance		RSEG	IL = 10µA			15,000	Ω
Backplane Output Impedance		RBP	IL = 10µA			600	Ω
Data Out Current:	Source Current	IDOH	VOH = 4.5			-3.0	mA
	Sink Current	IDOL	VOL = 0.4	3.2			mA
Voltage Converter:	@ No Load	VEE_c	See Fig. 2	-22	-21.5	-21	V
(VDD - VSS = 5V, TA = 25°C)	@ 0.1mA Load	IDD	See Fig. 2			1.8	mA
	@ 10KΩ Load	VEE_c	See Fig. 2	-20			V
Offset Voltage (Guaranteed, not tested)		VOS	See Fig. 4			25	mV

AC ELECTRICAL CHARACTERISTICS

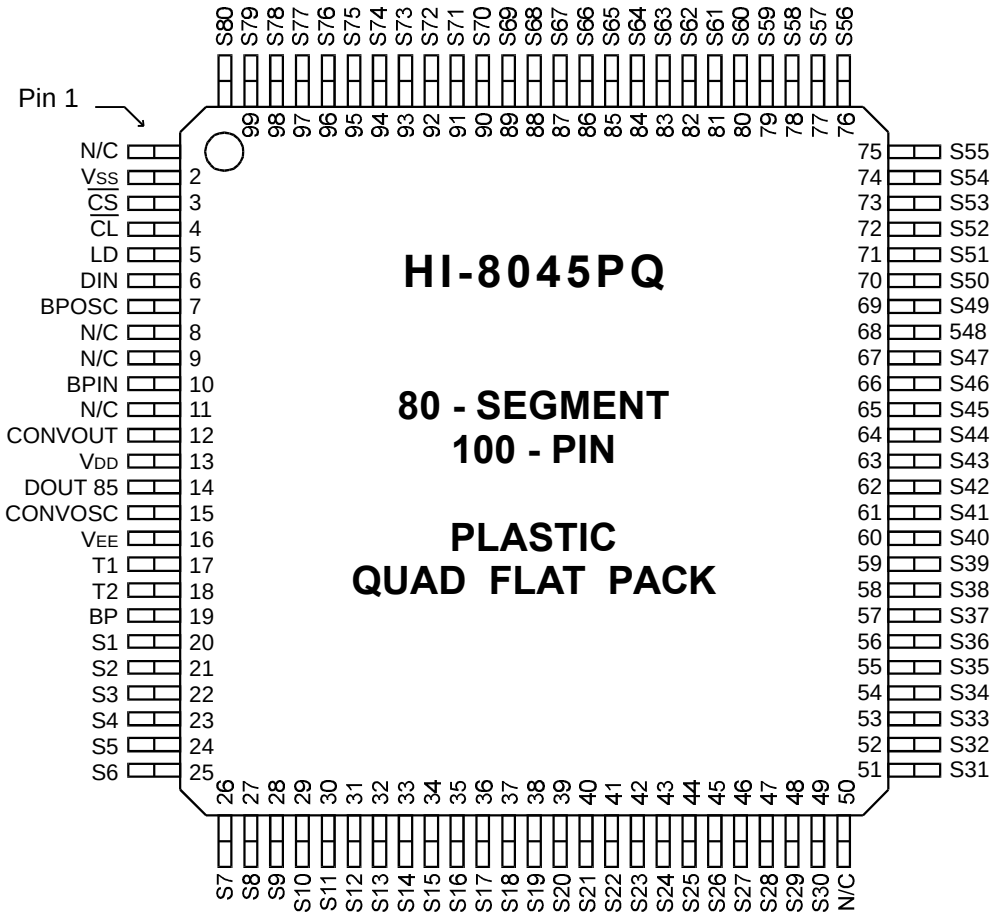
VDD = 5V , VEE = -21.5V, VSS = 0V, TA = Operating temperature range (unless otherwise specified).

PARAMETER		SYMBOL	VDD	MIN	TYP	MAX	UNITS
Clock Period	non-cascaded	tCL	5V	250			ns
	cascaded	tCL	5V	500			ns
Clock Pulse Width	non-cascaded	tCW	5V	125			ns
	cascaded	tCW	5V	250			ns
Data In - Setup		tDS	5V	80			ns
Data In - Hold		tDH	5V	80			ns
Chip Select - Setup to Clock		tCSS	5V	100			ns
Chip Select - Hold to Clock		tCSH	5V	120			ns
Load - Setup to Clock		tLS	5V	120			ns
Chip Select - Setup to Load		tCSL	5V	0			ns
Load Pulse Width		tLW	5V	130			ns
Chip Select - Hold to Load		tLCS	5V	120			ns
Data Out Valid, from Clock		tCDO	5V			170	ns

ORDERING INFORMATION

PART NUMBER	PACKAGE DESCRIPTION	TEMPERATURE RANGE	FLOW	LEAD FINISH
HI-8045PQ	100-PIN PLASTIC QUAD FLAT PACK (PQFP)	-40°C to +85°C	I	SOLDER
HI-8045PQT	100-PIN PLASTIC QUAD FLAT PACK (PQFP)	-55°C to +125°C	T	SOLDER

MAGNIFIED VIEW OF PIN ASSIGNMENTS



100-PIN PLASTIC QUAD FLAT PACK (PQFP)

Package Type: 100PQS