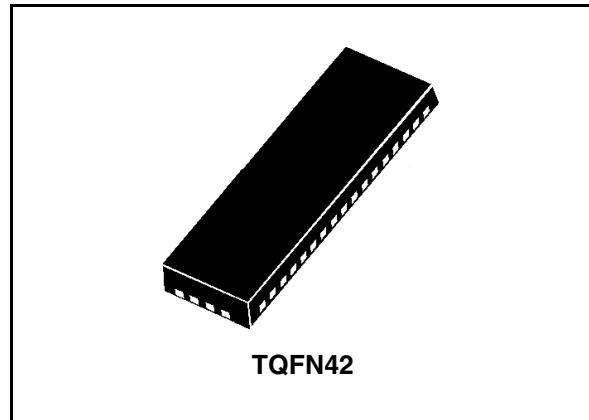


NEATSwitch™: octal SPDT high bandwidth signal switch

Features

- Supports 3.0 Gbps generic data rate
- Octal SPDT switch to support 2 PCI lanes
- Low R_{ON} : 5.5 Ω typical
- Internal voltage regulator
- V_{CC} operating range:
 - 1.65 – 2.0 V (internal regulator bypassed)
 - 2.7 – 3.6 V (internal regulator active)
- Low current consumption: 150 μ A
- ESD HBM model: 2 kV
- Channel on capacitance: 6 pF typical
- Switching time speed: 9 ns
- Near to zero propagation delay: 250 ps
- Bandwidth: -3 dB at 1200 MHz
- Low crosstalk: -20 dB at 1200 MHz
- Bit-to-bit skew: 50 ps typical
- Data and control inputs provide undershoot clamp diode
- Wide bandwidth minimizes skew and jitter
- Hot insertion capable
- Supports bidirectional operation
- Supports PCI-E gen. 1, display ports, LVDS, TMDS and video signaling
- -40 °C to 85 °C operating temperature range



TQFN42

Description

The STMUX3040 is a differential octal single pole double throw (SPDT) bidirectional signal switch with low R_{ON} . It is designed to support various standards such as PCIe gen 1, LVDS, TMDS and video signaling.

The STMUX3040 features very low cross-talk, low bit-to-bit skew, high channel-to-channel noise isolation and low I/O capacitance.

The STMUX3040 switch offers very little or practically no attenuation of the high speed signals at the outputs, thus preserving the signal integrity to pass stringent requirements.

Applications

- Workstation
- PC and notebooks

Table 1. Device summary

Order code	Package	Packaging
STMUX3040QTTR	TQFN42	Tape and reel

Contents

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1 Functional diagrams

Figure 1. Functional diagram (switches)

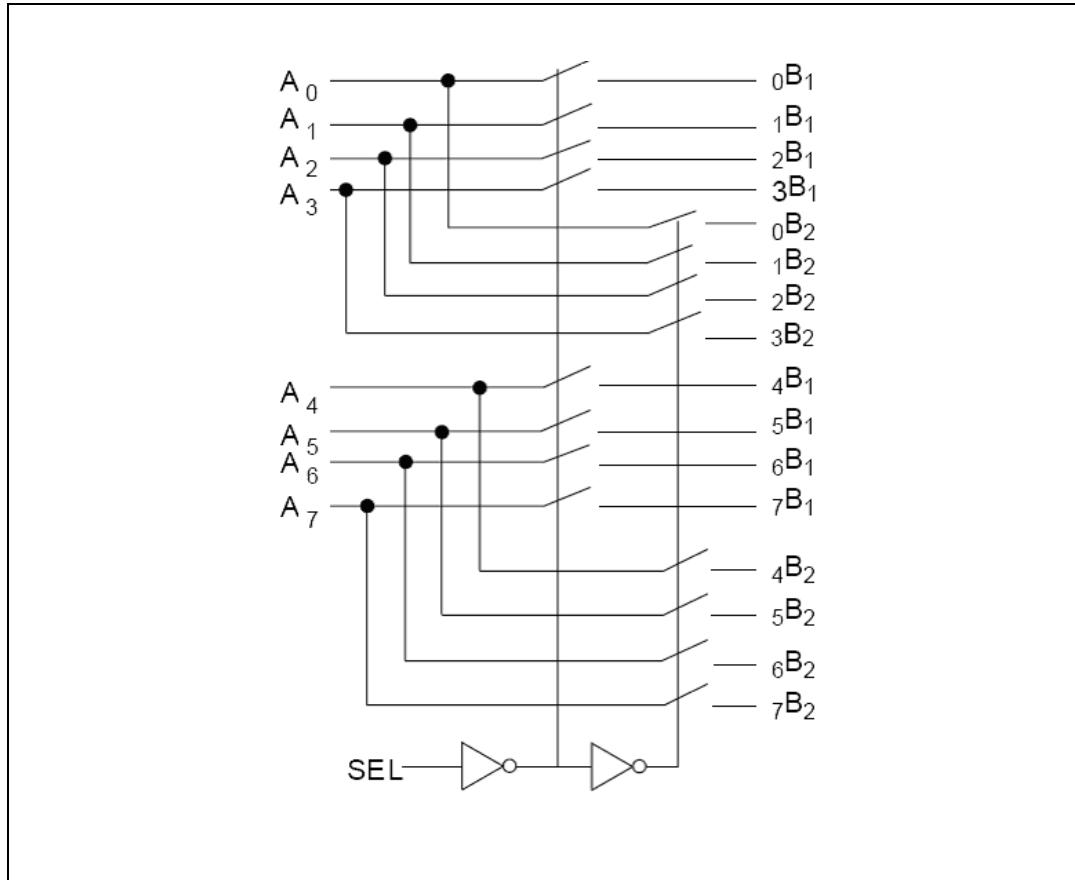
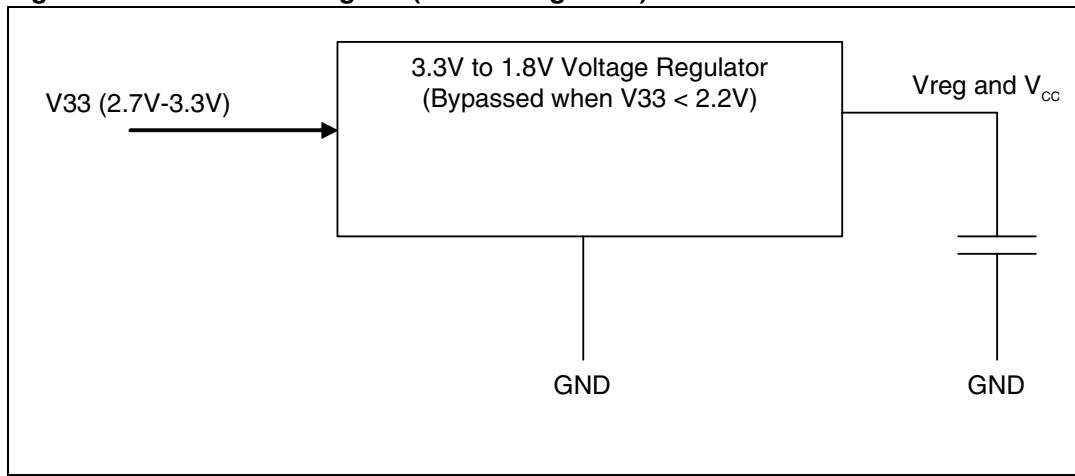


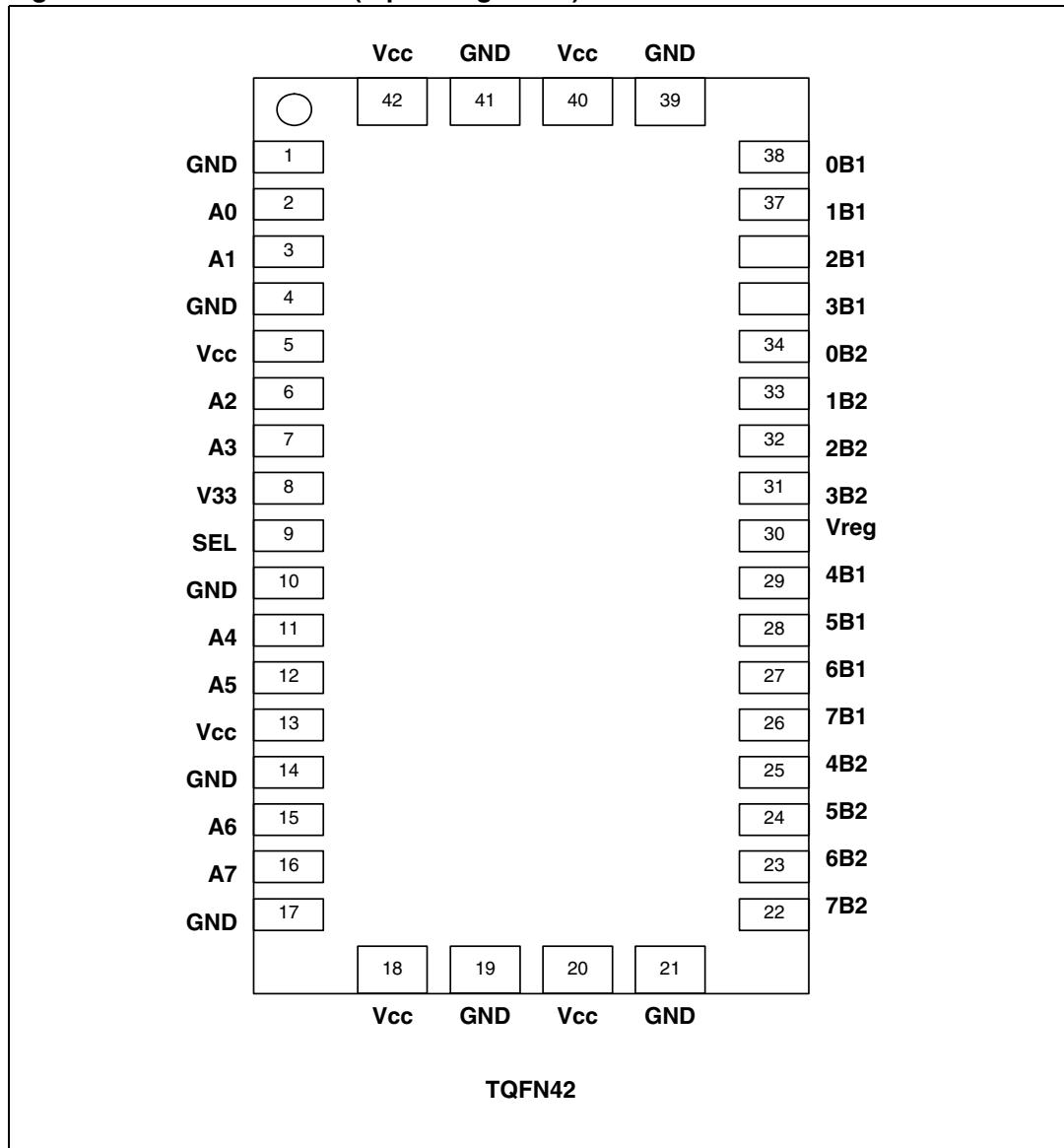
Figure 2. Functional diagram (internal regulator)



2 Pin settings

2.1 Pin connection

Figure 3. Pin connection (top through view)



2.2 Pin description

Table 2. Pin description

Pin number	Pin name	Function
1	GND	Ground
2	A ₀	Switch
3	A ₁	Switch
4	GND	Ground
5	Vcc	1.65 - 2.0 V supply Tied to V _{REG} if V33 > 2.2 V
6	A ₂	Switch
7	A ₃	Switch
8	V33	2.7 V – 3.3 V (internal regulator active) 1.65 – 2.0 V (internal regulator bypassed)
9	SEL	Switch select pin
10	GND	Ground
11	A ₄	Switch
12	A ₅	Switch
13	Vcc	1.65 – 2.0 V supply Tied to V _{REG} if V33 > 2.2 V
14	GND	Ground
15	A ₆	Switch
16	A ₇	Switch
17	GND	Ground
18	Vcc	1.65 – 2.0 V supply Tied to V _{REG} if V33 > 2.2 V
19	GND	Ground
20	Vcc	1.65 – 2.0 V supply Tied to V _{REG} if V33 > 2.2 V
21	GND	Ground
22	7B ₂	Switch
23	6B ₂	Switch
24	5B ₂	Switch
25	4B ₂	Switch
26	7B ₁	Switch
27	6B ₁	Switch
28	5B ₁	Switch

Table 2. Pin description (continued)

Pin number	Pin name	Function
29	₄ B ₁	Switch
30	VREG	Output of internal regulator 22 nF capacitor required here
31	₃ B ₂	Switch
32	₂ B ₂	Switch
33	₁ B ₂	Switch
34	₀ B ₂	Switch
35	₃ B ₁	Switch
36	₂ B ₁	Switch
37	₁ B ₁	Switch
38	₀ B ₁	Switch
39	GND	Ground
40	Vcc	1.65 – 2.0 V supply Tied to V _{REG} if V33 > 2.2 V
41	GND	Ground
42	Vcc	1.65 – 2.0 V supply Tied to V _{REG} if V33 > 2.2 V

2.3 Device operation table

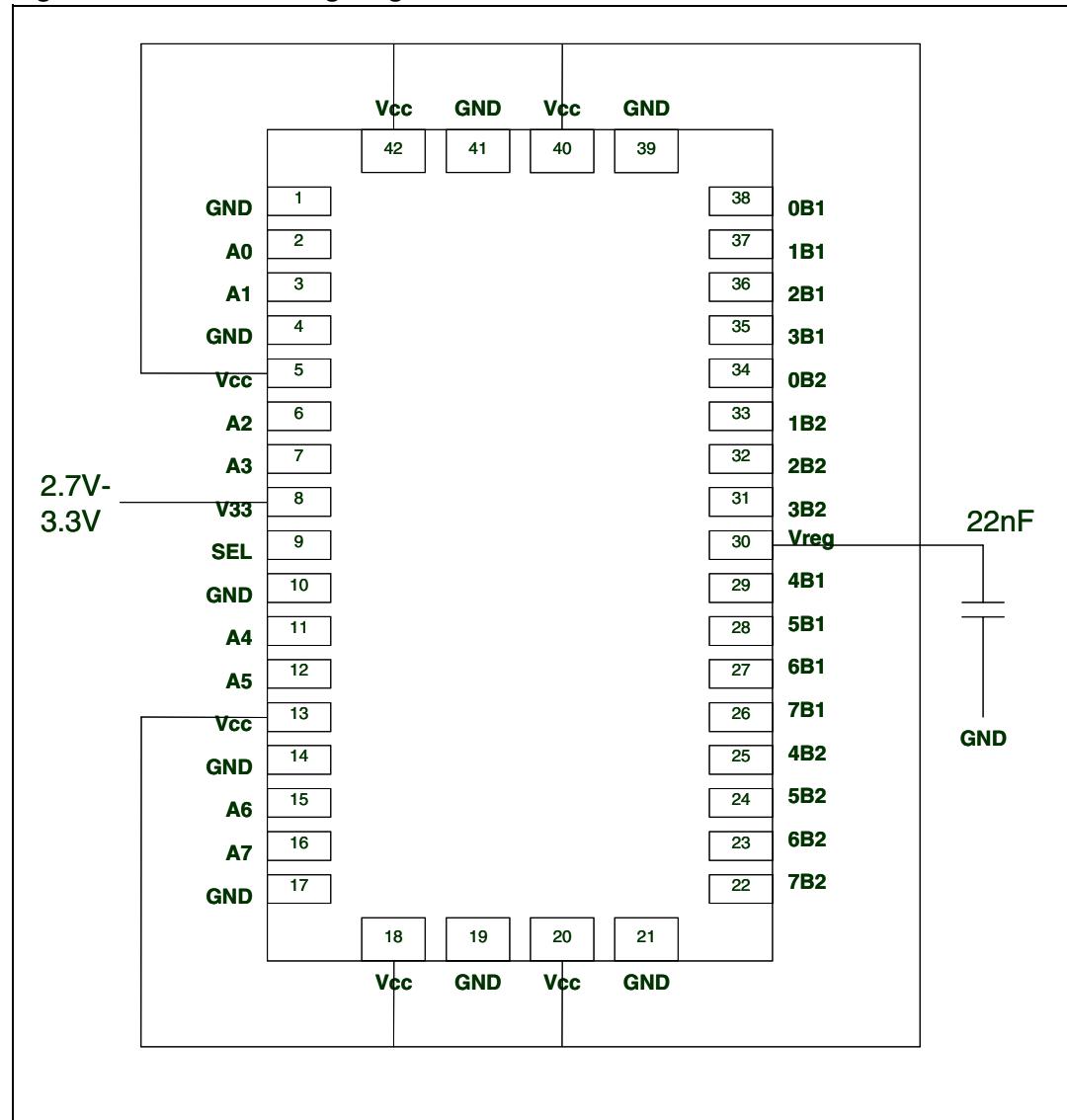
Table 3. Operation table

SEL	Function
L	A _N to _N B ₁
H	A _N to _N B ₂

3 Internal voltage regulator

The STMUX3040 is integrated with an internal voltage regulator. The voltage regulator is activated when the supply voltage to the Vreg pin is more than 2.7 V. If the supply to V_{reg} is less than 2.2 V, the regulator is bypassed.

Figure 4. Internal voltage regulator



When the internal regulator is activated:

- V₃₃ is used as supply input
- V_{reg} is used as output of the internal regulator, a 22 nF capacitor should be connected from this pin to ground

When internal regulator is not used:

- V_{CC}, V₃₃ and V_{reg} are all connected to 1.8 V supply

4 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

4.1 Absolute maximum rating

Table 4. Absolute maximum rating

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage to ground	-0.5 to +2.5	V
V_{33}	Supply voltage to internal regulator	-0.5 to +4.5	V
V_I	DC input voltage	-0.5 to V_{CC} ⁽¹⁾	V
V_{IC}	DC control input voltage	-0.5 to V_{CC} ⁽¹⁾	V
I_O	DC output current	120	mA
T_{STG}	Storage temperature	-65 to +150	°C
T_L	Lead temperature (10 sec)	300	°C

1. $V_{CC} = 1.8 \text{ V} \pm 10\%$ in regulator mode.

4.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	40.8	°C/W

5 Electrical specification

5.1 DC electrical characteristics

$T_A = -40$ to $+85^\circ\text{C}$, $V_{CC} = 1.8 \text{ V} \pm 10\%$
 Table 6. SEL pin

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{IH}	High level input voltage	High level guaranteed	0.65 V_{CC}			V
V_{IL}	Low level input voltage	Low level guaranteed	-0.5		0.35 V_{CC}	V
V_{IK}	Clamp diode voltage	$V_{CC} = 1.8 \text{ V}$, $I_{IN} = -18 \text{ mA}$		-0.8	-1.2	V
I_{IH}	Input high current	$V_{CC} = 1.8 \text{ V}$ $V_{IN} = V_{CC}$			± 5	μA
I_{IL}	Input low current	$V_{CC} = 1.8 \text{ V}$, $V_{IN} = \text{GND}$			± 5	μA

Table 7. All signal switch pins

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{IN}	Input leakage	$V_{CC} = 1.8 \text{ V}$ $V_{IN} = V_{CC}$ All non-tested switches floating			1	μA
V_{IK}	Clamp diode voltage	$V_{CC} = 1.8 \text{ V}$, $I_{IN} = -18 \text{ mA}$		-0.8	-1.2	V
R_{ON}	Switch ON resistance ⁽¹⁾	$V_{CC} = 1.8 \text{ V}$ $V_{IN} = 0.9$ to V_{CC} $I_{IN} = -30 \text{ mA}$		5.5	8.0	Ω
R_{FLAT}	ON resistance flatness ^{(1) (2)}	$V_{CC} = 1.8 \text{ V}$ $V_{IN} = 0.9$ to V_{CC} $I_{IN} = -30 \text{ mA}$		1	1.3	Ω
ΔR_{ON}	ON resistance match between channels $\Delta R_{ON} = R_{ONMAX} - R_{ONMIN}$ ^{(2) (3)}	$V_{CC} = 1.8 \text{ V}$ $V_{IN} = 0.9$ to V_{CC} $I_{IN} = -30 \text{ mA}$		0.5	1	Ω

1. Measured by voltage drop between channels at the indicated current through the switch.
2. Flatness is defined as the difference between the R_{ONMAX} and the R_{ONMIN} of the ON resistance over the specified range on the same channel.
3. ΔR_{ON} measured at the same V_{CC} , temperature and voltage level.

5.2 Capacitance

Table 8. Capacitance ($T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
C_{OFF}	Port x0 to port x1, switch off	$V_{\text{IN}} = 0 \text{ V}$		4		pF
C_{ON}	Capacitance switch on	$V_{\text{IN}} = 0 \text{ V}$		6		pF

5.3 Power supply characteristics

Table 9. Power supply characteristics ($T_A = -40 \text{ to } +85^\circ\text{C}$)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{CC}	Supply voltage (internal regulator inactive)		1.65	1.8	2.0	V
V_{33}	Supply voltage (internal regulator active)		2.7	3.3	3.6	V
I_{CC}	Quiescent power supply current (internal regulator inactive)	$V_{\text{CC}} = 2.0 \text{ V}$, $V_{\text{IN}} = V_{\text{CC}}$ or GND		150	500	μA
I_{CC}	Quiescent power supply current (internal regulator active)	$V_{33} = 3.3\text{V}$, $V_{\text{IN}} = 1.8\text{V}$ or GND		250	700	μA

5.4 Dynamic electrical characteristics

Table 10. Dynamic electrical characteristics ($T_A = -40 \text{ to } +85^\circ\text{C}$, $V_{\text{CC}} = 1.8 \text{ V} \pm 10\%$)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
X_{TALK}	Non-adjacent channel Cross-talk	$R_L = 100 \Omega$, $f = 300 \text{ MHz}$			-30	dB
		$R_L = 100 \Omega$, $f = 600 \text{ MHz}$			-20	dB
		$R_L = 100 \Omega$, $f = 1200 \text{ MHz}$			-20	dB
O_{IRR}	Off isolation	$R_L = 100 \Omega$, $f = 300 \text{ MHz}$			-35	dB
		$R_L = 100 \Omega$, $f = 600 \text{ MHz}$			-28	dB
		$R_L = 100 \Omega$, $f = 1200 \text{ MHz}$			-20	dB
D_R	Data rate per channel			3.0		Gbps
BW	Bandwidth	-3dB bandwidth	1200	1300		MHz

5.5 Dynamic switching characteristics

Table 11. Dynamic switching characteristics ($T_A = -40$ to $+85$ °C, $V_{CC} = 1.8$ V $\pm 10\%$)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_{PD}	Propagation delay	$V_{CC} = 1.65$ V - 2.0 V		0.25		ns
t_{PZH} , t_{PZL}	Line enable time, SEL to x to x0 or x to x1	$V_{CC} = 1.65$ V - 2.0V	0.5	6.5	9	ns
t_{PHZ} , t_{PLZ}	Line disable time, SEL to x to x0 or x to x1	$V_{CC} = 1.65$ V - 2.0 V	0.5	6.5	8.5	ns
$t_{SK(O)}$	Output skew between center port to any other port	$V_{CC} = 1.65$ V - 2.0 V		50	100	ps
$t_{SK(P)}$	Skew between opposite transition of the same output ($t_{PHL} - t_{PLH}$)	$V_{CC} = 1.65$ V - 2.0 V		50	100	ps
t_{ON}	Switching delay	$V_{CC} = 1.65$ V - 2.0 V			50	ns
t_{OFF}	Switching delay	$V_{CC} = 1.65$ V - 2.0 V			30	ns

5.6 ESD performance

Table 12. ESD performance

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ESD	IEC-61000-4-2	Air discharge (10 pulses)		± 2		kV
		Contact discharge (10 pulses)		± 2		kV

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 5. Package dimensions

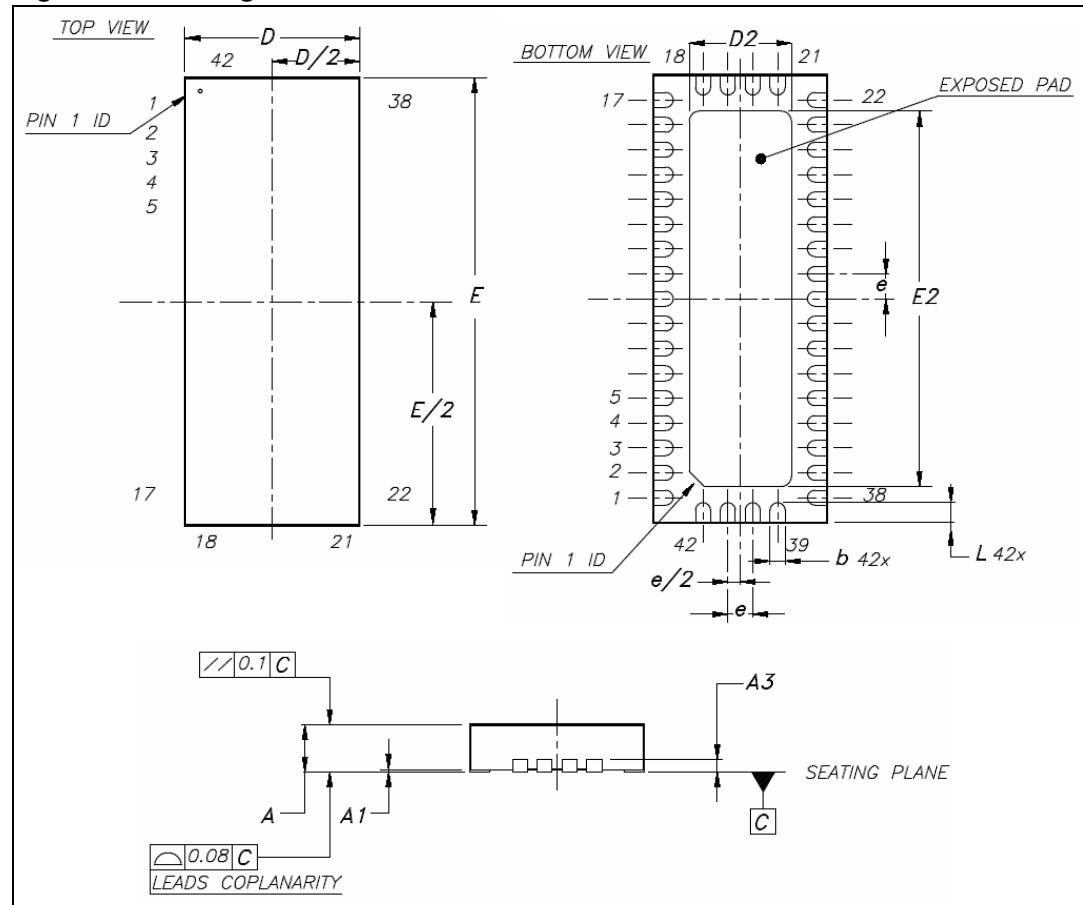


Table 13. TQFN42 mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20	
b	0.20	0.25	0.30
D	3.40	3.50	3.60
D2	2	2.05	2.10
E	8.90	9	9.10
E2	7.50	7.55	7.60
e		0.50	
L	0.30	0.40	0.50

Figure 6. TQFN42 footprint recommendations

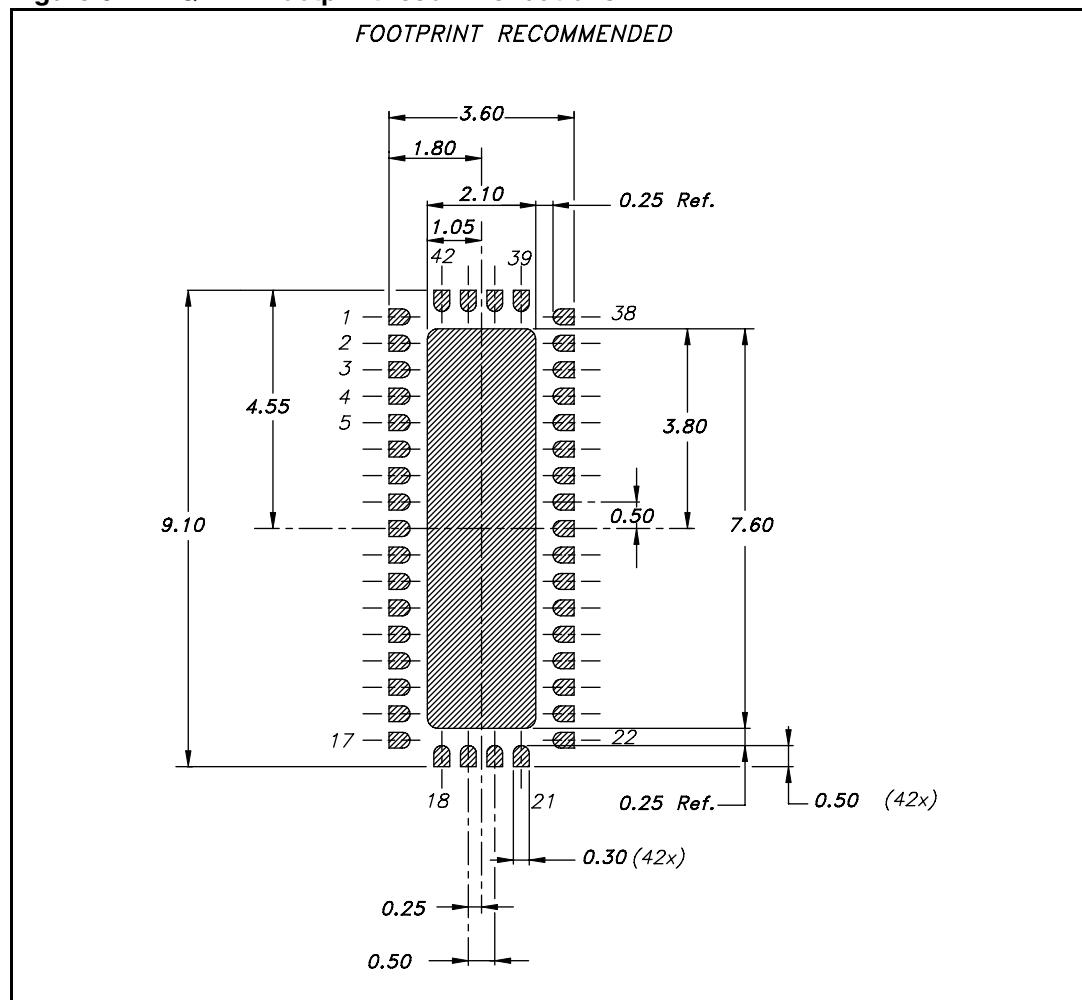


Figure 7. Tape information

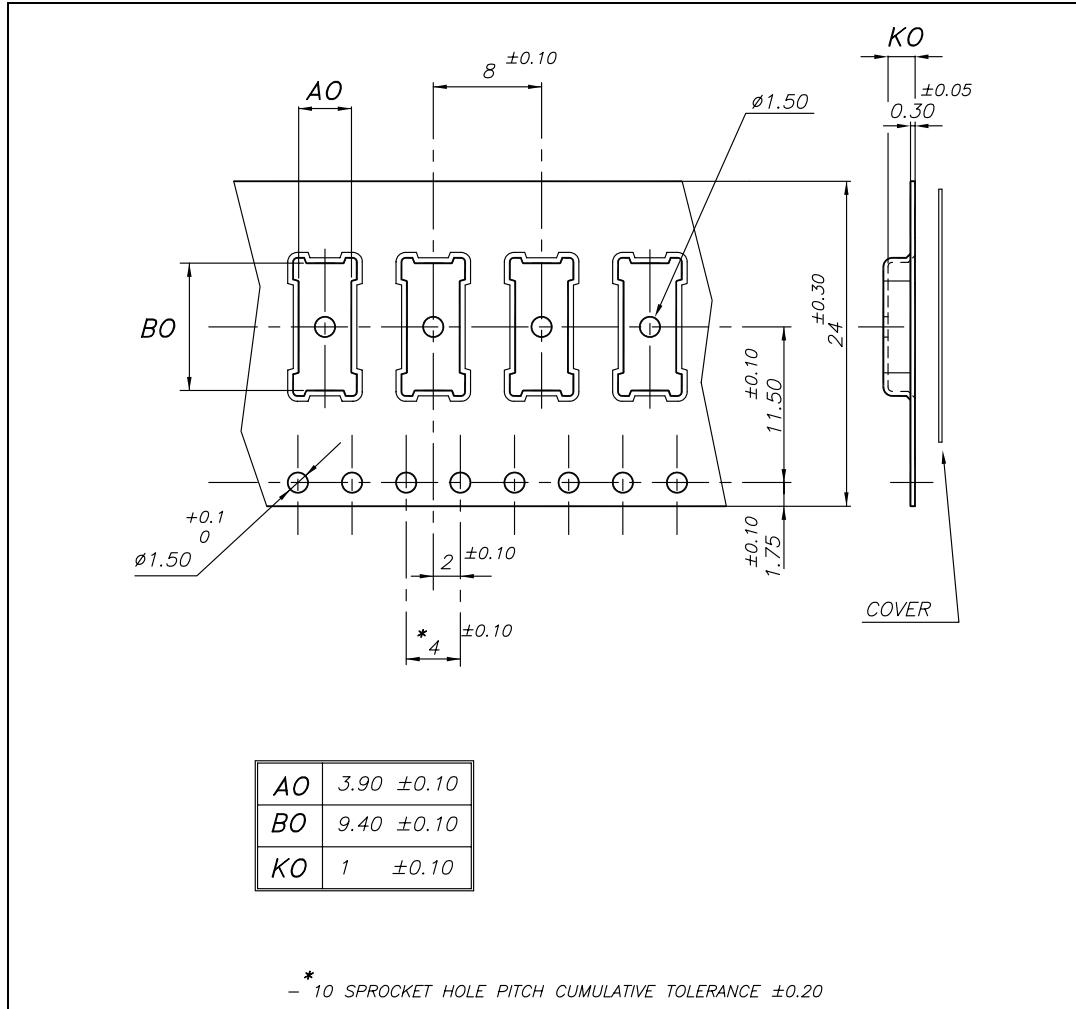
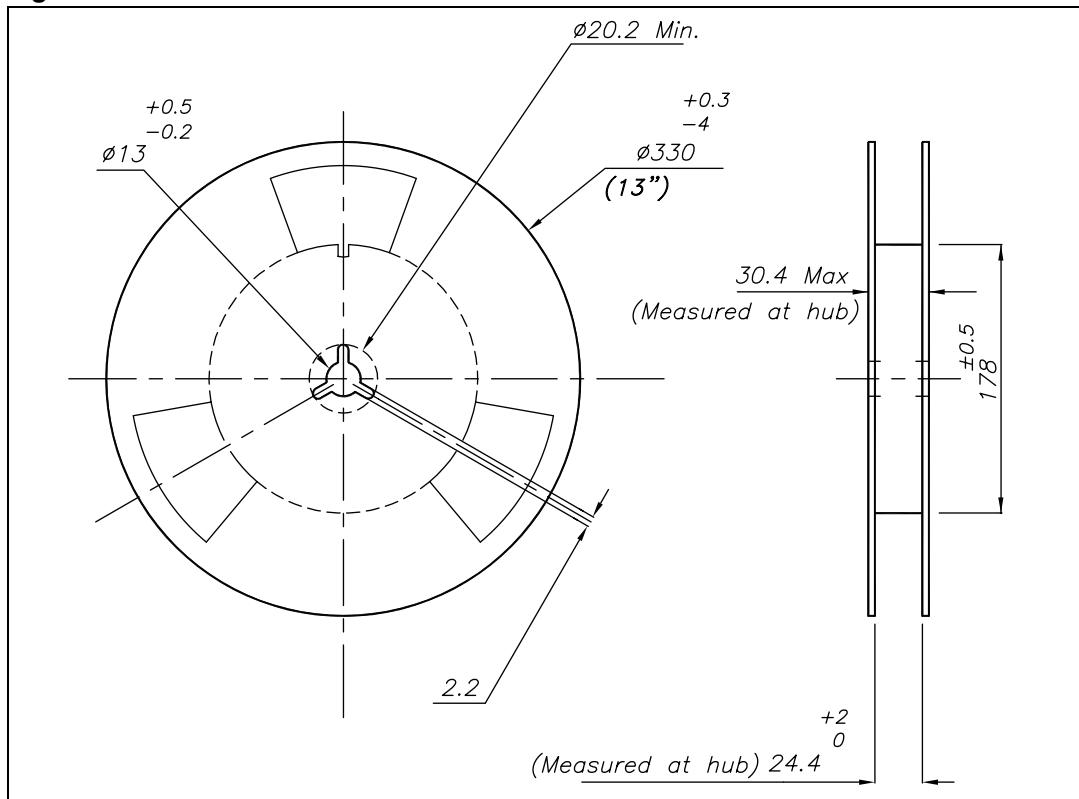


Figure 8. Reel information

7 Revision history

Table 14. Document revision history

Date	Revision	Changes
05-Jul-2007	1	Initial release.
09-Oct-2008	2	Content reworked to improve readability, no technical content change. Modified: title and datasheet cover page. Added: <i>Figure 7: Tape information on page 14</i> , <i>Figure 6: TQFN42 footprint recommendations on page 13</i> and <i>Figure 8: Reel information on page 15</i> .

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