TLE206x,TLE206xA, TLE206xB Excalibur JFET-Input High-Output-Drive µPower Operational Amplifiers

1 Features

- 2× Bandwidth (2MHz) of the TL06x and TL03x Operational Amplifiers
- Low supply current: 290µA/Ch (typical)
- On-chip offset voltage trimming for improved DC performance
- High output drive, specified into 100Ω loads
- Lower noise floor than earlier generations of low-power BiFETs

2 Applications

- Full authority digital engine control
- Flight control unit
- Analog input module

3 Description

The TLE206x series of low-power JFET-input operational amplifiers doubles the bandwidth of the earlier generation TL06x and TL03x BiFET families without significantly increasing power consumption. Texas Instruments Excalibur process also delivers a lower noise floor than the TL06x and TL03x. On-chip Zener trimming of offset voltage yields precision grades for dc-coupled applications. The TL206x devices are pin-compatible with other Texas Instruments BiFETs, in that the devices can be used to double the bandwidth of TL06x and TL03x circuits or to reduce power consumption of TL05x, TL07x, and TL08x circuits by nearly 90%.

BiFET operational amplifiers offer the inherently-higher input impedance of the JFET-input transistors, without sacrificing the output drive associated with bipolar amplifiers. These device features are designed for interfacing with high-impedance sensors or low-level ac signals. The devices also have inherently better ac response than bipolar or CMOS devices having comparable power consumption. The TLE206x family features a high-output-drive circuit capable of driving 100Ω loads at supplies as low as ±5V. This makes them uniquely suited for driving transformer loads in modems and other applications requiring good ac characteristics, low power, and high output drive.

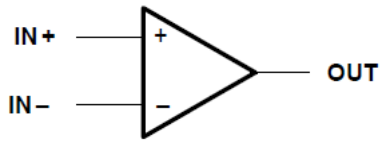
Because BiFET operational amplifiers are designed for use with dual power supplies, care must be taken to observe common-mode input voltage limits and output swing when operating from a single supply. DC biasing of the input signal is required and loads must be terminated to a virtual ground node at mid-supply. Texas Instruments TLE2426 integrated virtual ground generator is useful when operating BiFET amplifiers from single supplies.

The TLE206x are fully specified at ±15V and ±5V. For operation in low-voltage or single-supply systems, Texas Instruments LinCMOS families of operational amplifiers (TLC- and TLV-prefixes) are recommended. When moving from BiFET to CMOS amplifiers, particular attention should be paid to slew rate and bandwidth requirements and output loading. The Texas Instruments TLV2432 and TLV2442 CMOS operational amplifiers are excellent choices to consider.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TLE2061, TLE2061A, TLE2062	P (PDIP, 8)	9.81mm × 9.43mm
	D (SOIC, 8)	4.9mm × 6mm
TLE2062A	D (SOIC, 8)	4.9mm × 6mm
TLE2064, TLE2064A	N (PDIP, 14)	19.3mm × 9.4mm
	D (SOIC, 14)	8.65mm × 6mm
TLE2061M, TLE2061AM, TLE2062M	JG (CDIP, 8)	9.6mm × 6.67mm
	FK (LCCC, 20)	8.89mm × 8.89mm
TLE2064M, TLE2064BM	J (CDIP, 14)	19.56mm × 6.67mm
	FK (LCCC, 20)	8.89mm × 8.89mm
TLE2064AM	J (CDIP, 14)	19.56mm × 6.67mm
	CFP (W, 14)	9.21mm × 6.3mm
	FK (LCCC, 20)	8.89mm × 8.89mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Symbol

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4 Available Options

Table 4-1. TLE2061 Available Options

PACKAGED DEVICES							
T_A	V_{IOmax} at 25°C	SMALL OUTLINE (D)(1)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP(2) (PW)	CERAMIC FLAT PACK (U)
0°C to 70°C	500 µV	—	—	—	—	—	—
	1.5 mV	TLE2061ACD	—	—	TLE2061ACP	—	—
	3 mV	TLE2061CD	—	—	TLE2061CP	TLE2061CPWLE	—
–40°C to 85°C	500 µV	—	—	—	—	—	—
	1.5 mV	TLE2061AID	—	—	TLE2061AIP	—	—
	3 mV	TLE2061D	—	—	TLE2061IP	—	—
– 55°C to 125°C	500 µV	—	—	TLE2061BMJG	—	—	—
	1.5 mV	TLE2061AMD	TLE2061AMFK	TLE2061AMJG	—	—	TLE2061AMU
	3 mV	TLE2061MD	TLE2061MFK	TLE2061MJG	—	—	TLE2061MU

(1) The D packages are available taped and reeled. Add R suffix to device type (that is, TLE2061ACDR). Chips are tested at 25°C.
(2) The PW package is available left-end taped and reeled (indicated by the LE suffix on the device type (that is, TLE2061CPWLE).

Table 4-2. TLE2062 Available Options

PACKAGED DEVICES						
T_A	V_{IOmax} at 25°C	SMALL OUTLINE (D)(1)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	CERAMIC FLAT PACK (U)
0°C to 70°C	1 mV	TLE2062BCD	—	—	TLE2062BCP	—
	2 mV	TLE2062ACD	—	—	TLE2062ACP	—
	4 mV	TLE2062CD	—	—	TLE2062CP	—
– 40°C to 85°C	1 mV	TLE2062BID	—	—	TLE2062BIP	—
	2 mV	TLE2062AID	—	—	TLE2062AIP	—
	4 mV	TLE2062ID	—	—	TLE2062IP	—
– 55°C to 125°C	1 mV	TLE2062BMD	—	TLE2062BMJG	—	—
	2 mV	TLE2062AMD	TLE2062AMFK	TLE2062AMJG	—	TLE2062AMU
	4 mV	TLE2062MD	TLE2062MFK	TLE2062MJG	—	TLE2062MU

(1) The D packages are available taped and reeled. Add R suffix to device type (that is, TLE2082ACDR).

Table 4-3. TLE2064 Available Options

PACKAGED DEVICES						
T_A	V_{IOmax} at 25°C	SMALL OUTLINE (D)(1)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	CERAMIC FLAT PACK (W)
0°C to 70°C	2 mV	—			TLE2064BCN	
	4 mV	TLE2064ACD	—	—	TLE2064ACN	—
	6 mV	TLE2064CD			TLE2064CN	
-40°C to 85°C	2 mV	—			TLE2064BIN	
	4 mV	TLE2064AID	—	—	TLE2064AIN	—
	6 mV	TLE2064ID			TLE2064IN	
-55°C to 125°C	2 mV	—	TLE2064BMFK	TLE2064BMJ		—
	4 mV	TLE2064AMD	TLE2064AMFK	TLE2064AMJ	—	TLE2064AMW
	6 mV	TLE2064MD	TLE2064MFK	TLE2064MJ		TLE2064MW

(1) The D packages are available taped and reeled. Add R suffix to device type, (that is, TLE2064ACDR)

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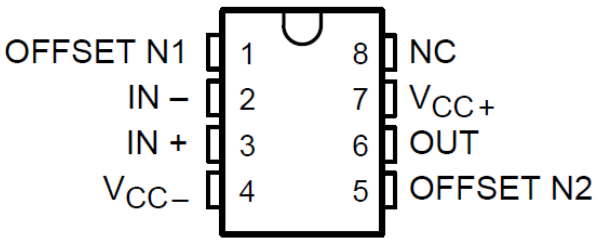

Figure 4-1. TLE2061, TLE2061A, and TLE2061B D, DB, JG, P, or PW Package (Top View)

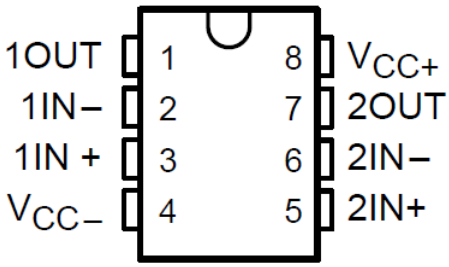

Figure 4-2. TLE2062, TLE2062A, and TLE2062B D, JG, or P Package (Top View)

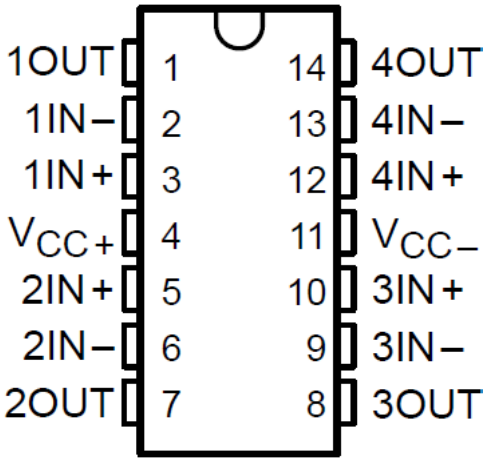

Figure 4-3. TLE2064, TLE2064A, and TLE2064B D, J, N, or W Package (Top View)

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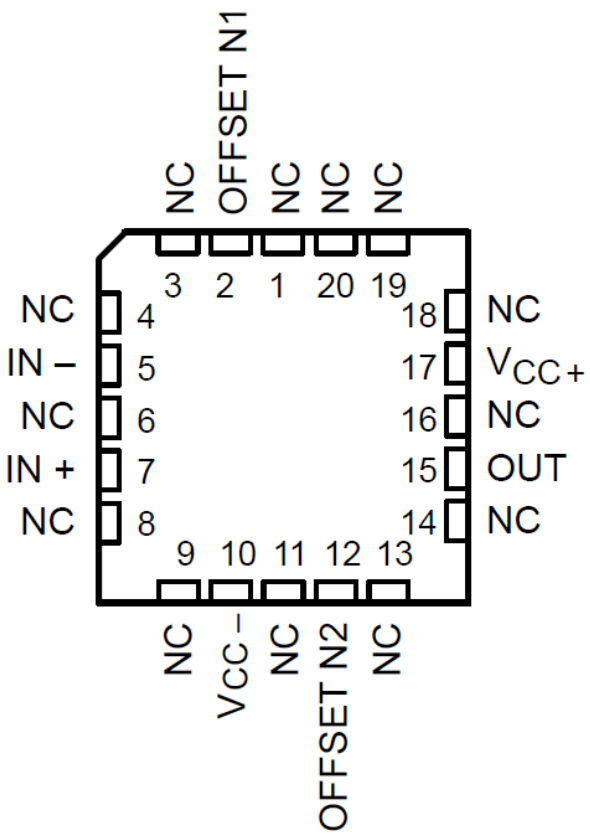

Figure 4-4. TLE2061M, TLE2061AM, and TLE2061BM FK Package (Top View)

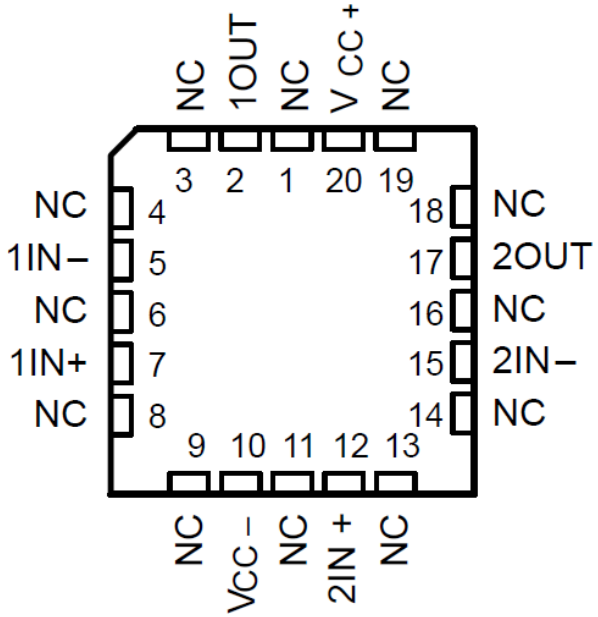

Figure 4-5. TLE2062M, TLE2062AM, and TLE2062BM FK Package (Top View)

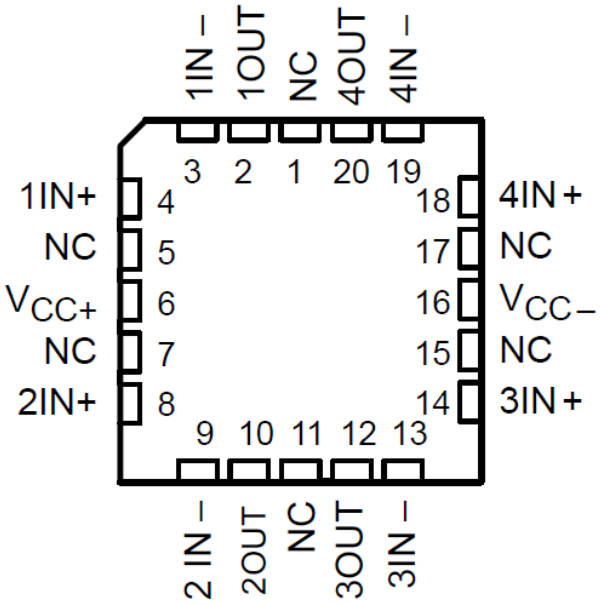

Figure 4-6. TLE2064M, TLE2064AM, and TLE2064BM FK Package (Top View)

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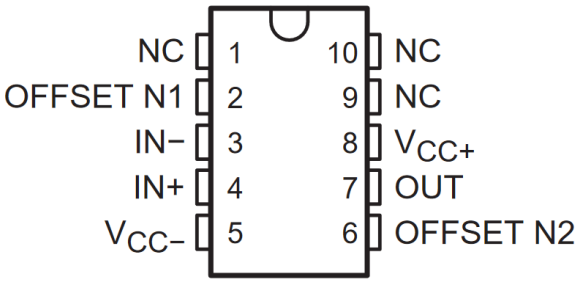


Figure 4-7. TLE2061 and TLE2061A U Package (Top View)

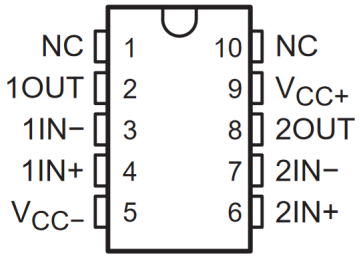
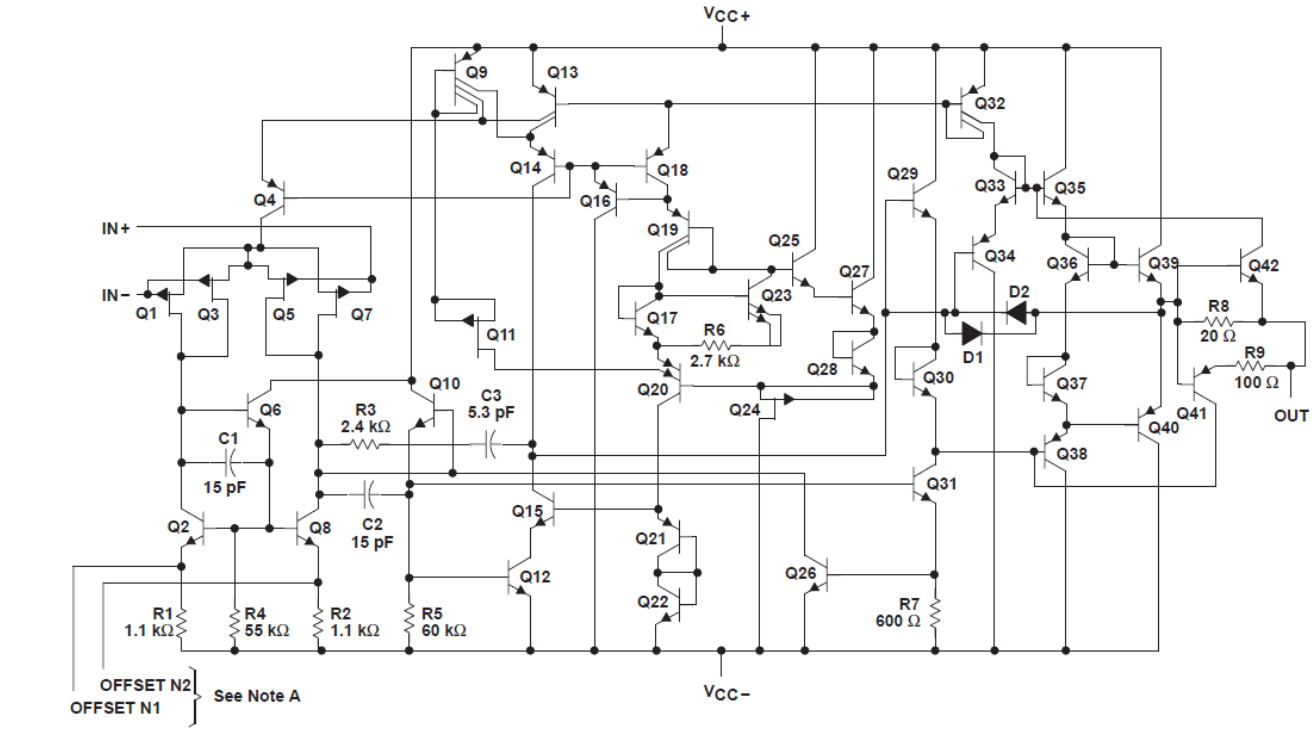


Figure 4-8. TLE2062 and TLE2062A U Package (Top View)



NOTES: A. OFFSET N1 AND OFFSET N2 are only availiable on the TLE2061x devices.
B. Component values are nominal.

ACTUAL DEVICE COMPONENT COUNT			
COMPONENT	TLE2061	TLE2062	TLE2064
Transistors	43	42	42
Resistors	9	9	9
Diodes	1	2	2
Capacitors	3	3	3

Figure 4-9. Equivalent Schematic (Each Channel)

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC+}	Supply voltage(2)			19	V
V_{CC-}	Supply voltage(2)			–19	V
V_{ID}	Differential input voltage range(3)		-38	38	V
V_I	Input voltage range (any input)		V_{CC-}	V_{CC+}	
I_I	Input current		-1	1	mA
I_O	Output current		-80	80	mA
V_{CC+}	Total current into			80	mA
V_{CC-}	Total current out of			-80	mA
	Duration of short-circuit current at (or below) 25°C(4)			Unlimited	
T_A	Operating free-air temperature range	C suffix	0	70	°C
		I suffix	–40	85	
		M suffix	–55	125	
T_{stg}	Storage temperature		-65	150	°C
	Case temperature for 60 seconds	FK package		260	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D package		260	°C
		P package			
		PW package			
	Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package		300	°C
		U			
		W			

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal GND.
(3) Differential voltages are at IN+ with respect to IN –.
(4) The output can be shorted to either supply. Temperatures and/or supply voltages must be limited to ensure that the maximum dissipation rate is not exceeded.

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5.2 Recommended Operating Conditions

			C SUFFIX		I SUFFIX		M SUFFIX		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$V_{CC\pm}$	Supply voltage		±3.5	±18	±3.5	±18	±3.5	±18	V
V_{IC}	Common-mode input voltage,	$V_{CC\pm}$ = ± 5 V	–1.6	4	–1.6	4	–1.6	4	V
		$V_{CC\pm}$ = ±15 V	–11	13	–11	13	–11	13	
T_A	Operating free-air temperature		0	70	–40	85	–55	125	°C

5.3 TLE2061C Electrical Characteristics

at specified free-air temperature, $V_{CC\pm}$ = ± 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A [1]	TLE2061C TLE2061AC TLE2061BC			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2061C	V_{IC} = 0, R_S = 50 Ω	25°C		0.1	3.1	mV
				Full range			4	
		TLE2061AC		25°C		0.1	2.6	
				Full range			3.5	
		TLE2061BC		25°C		0.1	1.9	
				Full range			2.4	
a_{VIO}	Temperature coefficient of input offset voltage			Full range		1		µV/°C
	Input offset voltage long-term drift[2]			25°C		0.04		µV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			0.8	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			2	nA
V_{ICR}	Common-mode input voltage range			25°C	-1.6 to 4	-2 to 6		V
				Full range	-1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	3.5	4.9		V
				Full range	3.3			
			R_L = 100 kΩ	25°C	2.5	4.5		V
				Full range	2			
$V_{OM–}$	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	–3.7	–4.9		V
				Full range	–3.3			
			R_L = 100 kΩ	25°C	–2.5	–4.5		V
				Full range	–2			
A_{VD}	Large-signal differential voltage amplification		V_O = ±2.8 V R_L = 10 Ω	25°C	15	225		V/mV
				Full range	2			
			V_O = 0 to 2 V R_L = 100 Ω	25°C	0.75	225		
				Full range	0.5			
			V_O = 0 to -2 V R_L = 100 Ω	25°C	0.5	225		
				Full range	0.25			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		280		Ω

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5.3 TLE2061C Electrical Characteristics (continued)

at specified free-air temperature, $V_{CC\pm}$ = ± 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	TLE2061C TLE2061AC TLE2061BC			UNIT
					MIN	TYP	MAX	
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICRmin},	R_S = 50 Ω	25°C	65	82		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ± 5 V to ± 15 V,		25°C	75	135		dB
		R_S = 50 Ω		Full range	75			
I_{CC}	Supply current	V_O = 0,	No load	25°C		120	325	µA
				Full range			350	

(1) Full range is 0°C to 70°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV

5.4 TLE2061C Operating Characteristics

at specified free-air temperature, $V_{CC\pm}$ =± 5 V

PARAMETER		TEST CONDITIONS		TA(1)	TLE2061C TLE2061AC TLE2061BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (See Figure 6-1)	RL = 10 kΩ,	CL = 100 pF	25°C	2.2	4		V/µs
				Full range	2.1			
V_n	Equivalent input noise voltage (See Figure 6-2)	f = 10 Hz,	RS = 20 Ω	25°C		59	100	nV/√Hz
		f = 1 kHz,	RS = 20 Ω			43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		µV
In	Equivalent input noise current	f = 1 kHz		25°C		1		fA/√Hz
THD	Total harmonic distortion	AVD = 2, VO(PP) = 2 V,	f = 10 kHz, RL = 10 kΩ	25°C		0.025%		
B1	Unity-gain bandwidth (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	25°C		1.8		MHz
		RL = 100 Ω, 0.1%	CL = 100 pF			1.3		
ts	Settling time	0.1%		25°C		5		µs
		0.01%				10		
BOM	Maximum output-swing bandwidth	AVD = 1,	RL = 10 kΩ	25°C		140		kHz
φm	Phase margin at unity gain (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	25°C		58°		
		RL = 100 Ω,	CL = 100 pF			75°		

(1) Full range is 0°C to 70°C.

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5.5 TLE2061C Electrical Characteristics

at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A [1]	TLE2061C TLE2061AC TLE2061BC			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2061C	V_{IC} = 0, R_S = 50 Ω	25°C		0.1	3	mV
				Full range			3.9	
		TLE2061AC		25°C		0.1	1.5	
				Full range			2.5	
		TLE2061BC		25°C		0.1	0.5	
				Full range			1	
a_{VIO}	Temperature coefficient of input offset voltage			Full range		1		µV/°C
	Input offset voltage long-term drift [2]			25°C		0.04		µV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			1	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			3	nA
V_{ICR}	Common-mode input voltage range			25°C	-11 to 13	-12 to 16		V
				Full range	-11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	13.2	14.9		V
				Full range	13			
			R_L = 600 Ω	25°C	12.5	14.5		V
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	–13.7	–14.9		V
				Full range	–13			
			R_L = 600 kΩ	25°C	–12.5	–14.5		V
				Full range	–12			
A_{VD}	Large-signal differential voltage amplification		V_O = ±10 V, R_L = 10 kΩ	25°C	30	225		V/mV
				Full range	20			
			V_O = 0 to 8 V, R_L = 600 Ω	25°C	25	225		
				Full range	10			
			V_O = 0 to -8 V, R_L = 600 Ω	25°C	3	225		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICRmin}, R_S = 50 Ω	25°C	72	90		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ± 5 V to ± 15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	75			
I_{CC}	Supply current		V_O = 0, No load	25°C		125	350	µA
				Full range			375	

(1) Full range is 0°C to 70°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV

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5.6 TLE2061C Operating Characteristics

at specified free-air temperature, $V_{CC\pm}$ =± 15 V

PARAMETER		TEST CONDITIONS		TA(1)	TLE2061C TLE2061AC TLE2061BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (See Figure 6-1)	RL = 10 kΩ,	CL = 100 pF	25°C	2.6	4		V/µs
				Full range	2.5			
V_n	Equivalent input noise voltage (See Figure 6-2)	f = 10 Hz,	RS = 20 Ω	25°C		70	100	nV/√Hz
		f = 1 kHz,	RS = 20 Ω			40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		µV
In	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	AVD = 2, VO(PP) = 2 V,	f = 10 kHz, RL = 10 kΩ	25°C		0.025%		
B1	Unity-gain bandwidth (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	25°C		2		MHz
		RL = 600 Ω	CL = 100 pF			1.5		
ts	Settling time	0.1%		25°C		5		µs
		0.01%				10		
BOM	Maximum output-swing bandwidth	AVD = 1,	RL = 10 kΩ	25°C		40		kHz
φm	Phase margin at unity gain (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	25°C		60°		
		RL = 600 Ω,	CL = 100 pF			70°		

(1) Full range is 0°C to 70°C.

5.7 TLE2061I Electrical Characteristics

at specified free-air temperature, $V_{CC\pm}$ = ± 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		TA (1)	TLE2061I TLE2061AI TLE2061BI			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2061I	V_{IC} = 0,	R_S = 50 Ω	25°C		0.1	3.1	mV
					Full range			4.4	
		TLE2061AI			25°C		0.1	2.6	
					Full range			3.9	
		TLE2061BI			25°C		0.1	1.9	
					Full range			2.7	
a_{VIO}	Temperature coefficient of input offset voltage				Full range		1		µV/°C
	Input offset voltage long-term drift(2)				25°C		0.04		µV/mo
I_{IO}	Input offset current				25°C		1		pA
					Full range			2	nA
I_{IB}	Input bias current				25°C		3		pA
					Full range			4	nA
V_{ICR}	Common-mode input voltage range				25°C	-1.6 to 4	-2 to 6		V
					Full range	-1.6 to 4			V

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5.7 TLE2061I Electrical Characteristics (continued)

at specified free-air temperature, $V_{CC\pm}$ = ± 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	TLE2061I TLE2061AI TLE2061BI			UNIT
					MIN	TYP	MAX	
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		25°C	3.5	4.9		V
				Full range	3.1			
		R_L = 100 kΩ		25°C	2.5	4.5		V
				Full range	2			
$V_{OM–}$	Maximum negative peak output voltage swing	R_L = 10 kΩ		25°C	–3.7	–4.9		V
				Full range	–3.1			
		R_L = 100 kΩ		25°C	–2.5	–4.5		V
				Full range	–2			
A_{VD}	Large-signal differential voltage amplification	V_O = ±2.8 V	R_L = 10 Ω	25°C	15	225		V/mV
				Full range	2			
		V_O = 0 to 2 V	R_L = 100 Ω	25°C	0.75	225		
				Full range	0.5			
		V_O = 0 to -2 V	R_L = 100 Ω	25°C	0.5	225		
				Full range	0.25			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance	I_O = 0		25°C		280		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICRmin},	R_S = 50 Ω	25°C	65	82		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ± 5 V to ± 15 V,		25°C	75	135		dB
		R_S = 50 Ω		Full range	65			
I_{CC}	Supply current	V_O = 0,	No load	25°C		120	325	μA
				Full range			350	

(1) Full range is -40°C to 85°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV

5.8 TLE2061I Operating Characteristics

at specified free-air temperature, $V_{CC\pm}$ =± 5 V

PARAMETER		TEST CONDITIONS		TA(1)	TLE2061I TLE2061AI TLE2061BI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (See Figure 6-1)	RL = 10 kΩ,	CL = 100 pF	25°C	2.2	4		V/μs
				Full range	1.7			
V_n	Equivalent input noise voltage (See Figure 6-2)	f = 10 Hz,	RS = 20 Ω	25°C		59	100	nV/√Hz
		f = 1 kHz,	RS = 20 Ω			43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
In	Equivalent input noise current	f = 1 kHz		25°C		1		fA/√Hz
THD	Total harmonic distortion	AVD = 2, VO(PP) = 2 V,	f = 10 kHz, RL = 10 kΩ	25°C		0.025%		

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at specified free-air temperature, $V_{CC\pm}$ =± 5 V

PARAMETER		TEST CONDITIONS		TA(1)	TLE2061I TLE2061AI TLE2061BI			UNIT
					MIN	TYP	MAX	
B1	Unity-gain bandwidth (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	25°C		1.8		MHz
		RL = 100 Ω, 0.1%	CL = 100 pF			1.3		
ts	Settling time	0.1%		25°C		5		µs
		0.01%				10		
BOM	Maximum output-swing bandwidth	AVD = 1,	RL = 10 kΩ	25°C		140		kHz
φm	Phase margin at unity gain (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	25°C		58°		
		RL = 100 Ω,	CL = 100 pF			75°		

(1) Full range is -40°C to 85°C.

5.9 TLE2061I Electrical Characteristics

at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		TA (1)	TLE2061I TLE2061AI TLE2061BI			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2061I	V_{IC} = 0,	R_S = 50 Ω	25°C		0.1	3	mV
					Full range			4.3	
		TLE2061AI			25°C		0.1	1.5	
					Full range			2.9	
		TLE2061BI			25°C		0.1	0.5	
					Full range			1.3	
a_{VIO}	Temperature coefficient of input offset voltage				Full range		1		µV/°C
	Input offset voltage long-term drift (2)				25°C		0.04		µV/mo
I_{IO}	Input offset current				25°C		2		pA
					Full range			3	nA
I_{IB}	Input bias current				25°C		4		pA
					Full range			5	nA
V_{ICR}	Common-mode input voltage range				25°C	-11 to 13	-12 to 16		V
					Full range	-11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ		25°C	13.2	14.9		V
					Full range	13			
			R_L = 600 Ω		25°C	12.5	14.5		V
					Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ		25°C	–13.2	–14.9		V
					Full range	–13			
			R_L = 600 kΩ		25°C	–12.5	–14.5		V
					Full range	–12			

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5.9 TLE2061I Electrical Characteristics (continued)

at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	TLE2061I TLE2061AI TLE2061BI			UNIT
					MIN	TYP	MAX	
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V	R_L = 10 kΩ	25°C	30	225		V/mV
				Full range	20			
		V_O = 0 to 8 V	R_L = 600 Ω	25°C	25	225		
				Full range	10			
		V_O = 0 to -8 V	R_L = 600 Ω	25°C	3	225		
				Full range	01			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance	I_O = 0		25°C		280		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICRmin},	R_S = 50 Ω	25°C	72	90		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ± 5 V to ± 15 V,		25°C	75	93		dB
		R_S = 50 Ω		Full range	65			
I_{CC}	Supply current	V_O = 0,	No load	25°C		125	350	μA
				Full range			375	

(1) Full range is -40°C to 85°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV

5.10 TLE2061I Operating Characteristics

at specified free-air temperature, $V_{CC\pm}$ =± 15 V

PARAMETER		TEST CONDITIONS		TA(1)	TLE2061I TLE2061AI TLE2061BI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (See Figure 6-1)	RL = 10 kΩ,	CL = 100 pF	25°C	2.6	4		V/μs
				Full range	2.1			
V_n	Equivalent input noise voltage (See Figure 6-2)	f = 10 Hz,	RS = 20 Ω	25°C		70	100	nV/√Hz
		f = 1 kHz,	RS = 20 Ω			40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
In	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	AVD = 2, VO(PP) = 2 V,	f = 10 kHz, RL = 10 kΩ	25°C		0.025%		
B1	Unity-gain bandwidth (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	25°C		2		MHz
		RL = 600 Ω	CL = 100 pF			1.5		
ts	Settling time	0.1%		25°C		5		μs
		0.01%				10		
BOM	Maximum output-swing bandwidth	AVD = 1,	RL = 10 kΩ	25°C		40		kHz

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at specified free-air temperature, $V_{CC\pm}$ =± 15 V

PARAMETER		TEST CONDITIONS		TA(1)	TLE2061I TLE2061AI TLE2061BI			UNIT
					MIN	TYP	MAX	
φm	Phase margin at unity gain (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	25°C		60°		
		RL = 600 Ω,	CL = 100 pF			70°		

(1) Full range is -40°C to 85°C.

5.11 TLE2061M Electrical Characteristics

at specified free-air temperature, $V_{CC\pm}$ = ± 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A (1)	TLE2061M TLE2061AM TLE2061BM			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2061M	V_{IC} = 0,	R_S = 50 Ω	25°C		0.1	3.1	mV
					Full range			6	
		TLE2061AM			25°C		0.1	2.6	
					Full range			4.6	
		TLE2061BM			25°C		0.1	1.9	
					Full range			3.1	
a_{VIO}	Temperature coefficient of input offset voltage				Full range		1		μV/°C
	Input offset voltage long-term drift(2)				25°C		0.04		μ V/mo
I_{IO}	Input offset current				25°C		1		pA
					Full range			15	nA
I_{IB}	Input bias current				25°C		3		pA
					Full range			30	nA
V_{ICR}	Common-mode input voltage range				25°C	-1.6 to 4	-2 to 6		V
					Full range	-1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ		25°C	3.5	4.9		V
					Full range	3			
			R_L = 600 kΩ		25°C	2.5	4.5		
					Full range	2			
			R_L = 100 kΩ		25°C	2.5	4.5		V
					Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ		25°C	-3.5	-4.9		V
					Full range	-3			
		FK and JG packages	R_L = 600 Ω		25°C	-2.5	-4.5		
					Full range	2			
		D and P packages	R_L = 100 Ω		25°C	–2.5	–4.5		V
					Full range	–2			

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5.11 TLE2061M Electrical Characteristics (continued)

at specified free-air temperature, $V_{CC\pm}$ = ± 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A (1)	TLE2061M TLE2061AM TLE2061BM			UNIT
						MIN	TYP	MAX	
A_{VD}	Large-signal differential voltage amplification		V_O = ±2.8 V	R_L = 10 kΩ	25°C	15	225		V/mV
					Full range	2			
		FK and JG packages	V_O = 0 to 2.5 V	R_L = 600 Ω	25°C	1	225		
					Full range	0.5			
			V_O = 0 to -2.5 V	R_L = 600 Ω	25°C	1	225		
					Full range	0.5			
		D and P packages	V_O = 0 to 2 V	R_L = 100 Ω	25°C	0.75	225		
					Full range	0.5			
			V_O = 0 to -2 V	R_L = 100 Ω	25°C	0.5	225		
					Full range	0.25			
r_i	Input resistance				25°C		10^{12}		Ω
c_i	Input capacitance				25°C		4		pF
z_o	Open-loop output impedance		I_O = 0		25°C		280		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICRmin},	R_S = 50 Ω	25°C	65	82		dB
					Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ± 5 V to ± 15 V,		25°C	75	135		dB
			R_S = 50 Ω		Full range	65			
I_{CC}	Supply current		V_O = 0,	No load	25°C		120	325	μA
					Full range			350	

(1) Full range is -55°C to 125°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV

5.12 TLE2061M Operating Characteristics

at specified free-air temperature, $V_{CC\pm}$ =± 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2061M TLE2061AM TLE2061BM			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain (See Figure 6-1)	RL = 10 kΩ,	CL = 100 pF		4		V/μs
V_n	Equivalent input noise voltage (See Figure 6-2)	f = 10 Hz,	RS = 20 Ω		59		nV/√Hz
		f = 1 kHz,	RS = 20 Ω		43		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			1.1		μV
In	Equivalent input noise current	f = 1 kHz			1		fA/√Hz
THD	Total harmonic distortion	AVD = 2, VO(PP) = 2 V,	f = 10 kHz, RL = 10 kΩ		0.025%		
B1	Unity-gain bandwidth (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF		1.8		MHz
		RL = 100 Ω, 0.1%	CL = 100 pF		1.3		
ts	Settling time	0.1%			5		μs
		0.01%			10		

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at specified free-air temperature, $V_{CC\pm}$ =± 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2061M TLE2061AM TLE2061BM			UNIT
				MIN	TYP	MAX	
BOM	Maximum output-swing bandwidth	AVD = 1,	RL = 10 kΩ		140		kHz
φm	Phase margin at unity gain (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF		58°		
		RL = 100 Ω,	CL = 100 pF		75°		

5.13 TLE2061M Electrical Characteristics

at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A [1]	TLE2061M TLE2061AM TLE2061BM			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2061M	V_{IC} = 0,	R_S = 50 Ω	25°C		0.1	3	mV
					Full range			6	
		TLE2061AM			25°C		0.1	1.5	
					Full range			3.6	
		TLE2061BM			25°C		0.1	0.5	
					Full range			1.7	
a_{VIO}	Temperature coefficient of input offset voltage				Full range		1		µV/°C
	Input offset voltage long-term drift[2]				25°C		0.04		µV/mo
I_{IO}	Input offset current				25°C		2		pA
					Full range			20	nA
I_{IB}	Input bias current				25°C		4		pA
					Full range			40	nA
V_{ICR}	Common-mode input voltage range				25°C	-11 to 13	-12 to 16		V
					Full range	-11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ		25°C	13	14.9		V
					Full range	12.5			
			R_L = 600 Ω		25°C	12.5	14.5		V
					Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ		25°C	–13	–14.9		V
					Full range	–12.5			
			R_L = 600 kΩ		25°C	–12.5	–14.5		V
					Full range	–12			
A_{VD}	Large-signal differential voltage amplification		V_O = ±10 V	R_L = 10 kΩ	25°C	30	225		V/mV
					Full range	20			
			V_O = 0 to 8 V	R_L = 600 Ω	25°C	25	225		
					Full range	7			
			V_O = 0 to -8 V	R_L = 600 Ω	25°C	3	225		
					Full range	1			
r_i	Input resistance				25°C		10^{12}		Ω
c_i	Input capacitance				25°C		4		pF
z_o	Open-loop output impedance		I_O = 0		25°C		280		Ω

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5.13 TLE2061M Electrical Characteristics (continued)

at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	TLE2061M TLE2061AM TLE2061BM			UNIT
					MIN	TYP	MAX	
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICRmin},	R_S = 50 Ω	25°C	72	90		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ± 5 V to ± 15 V,		25°C	75	93		dB
		R_S = 50 Ω		Full range	65			
I_{CC}	Supply current	V_O = 0,	No load	25°C		125	350	µA
				Full range			375	

(1) Full range is -55°C to 125°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV

5.14 TLE2061M Operating Characteristics

at specified free-air temperature, $V_{CC\pm}$ =± 15 V

PARAMETER		TEST CONDITIONS		TA(1)	TLE2061M TLE2061AM TLE2061BM			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (See Figure 6-1)	RL = 10 kΩ,	CL = 100 pF	25°C	2.6	4		V/µs
				Full range	1.8			
V_n	Equivalent input noise voltage (See Figure 6-2)	f = 10 Hz,	RS = 20 Ω	25°C		70		nV/√Hz
		f = 1 kHz,	RS = 20 Ω			40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		µV
In	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	AVD = 2, VO(PP) = 2 V,	f = 10 kHz, RL = 10 kΩ	25°C		0.025%		
B1	Unity-gain bandwidth (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	25°C		2		MHz
		RL = 600 Ω	CL = 100 pF			1.5		
ts	Settling time	0.1%		25°C		5		µs
		0.01%				10		
BOM	Maximum output-swing bandwidth	AVD = 1,	RL = 10 kΩ	25°C		40		kHz
φm	Phase margin at unity gain (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	25°C		60°		
		RL = 600 Ω,	CL = 100 pF			70°		

(1) Full range is -55°C to 125°C.

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5.15 TLE2061Y Electrical Characteristics

at $V_{CC\pm}$ = ± 15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLE2061Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0,	R_S = 50 Ω		0.6	3	mV
	Input offset voltage long-term drift (1)				0.04		μV/mo
I_{IO}	Input offset current				2		pA
I_{IB}	Input bias current				4		pA
V_{ICR}	Common-mode input voltage range			-11 to 13	-12 to 16		V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		13.2	13.7		V
		R_L = 600 Ω		12.5	13.2		V
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		–13.2	–13.7		V
		R_L = 600 kΩ		–12.5	-13		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V	R_L = 10 kΩ	30	230		V/mV
		V_O = 0 to 8 V	R_L = 600 Ω	25	100		
		V_O = 0 to -8 V	R_L = 600 Ω	3	25		
r_i	Input resistance				10^{12}		Ω
c_i	Input capacitance				4		pF
z_o	Open-loop output impedance	I_O = 0			280		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICRmin},	R_S = 50 Ω	72	90		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ± 5 V to ± 15 V,		75	93		dB
I_{CC}	Supply current	V_O = 0,	No load		290	350	μA

(1) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV

5.16 TLE2061Y Operating Characteristics

at $V_{CC\pm}$ =± 15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2061Y			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain (See Figure 6-1)	RL = 10 kΩ,	CL = 100 pF	2.6	3.4		V/μs
V_n	Equivalent input noise voltage (See Figure 6-2)	f = 10 Hz,	RS = 20 Ω		70		nV/√Hz
		f = 1 kHz,	RS = 20 Ω		40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			1.1		μV
In	Equivalent input noise current	f = 1 Hz			1.1		fA/√Hz
THD	Total harmonic distortion	AVD = 2, VO(PP) = 2 V,	f = 10 kHz, RL = 10 kΩ		0.025%		
B1	Unity-gain bandwidth (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF		2		MHz
		RL = 600 Ω	CL = 100 pF		1.5		
ts	Settling time	0.1%			5		μs
		0.01%			10		
BOM	Maximum output-swing bandwidth	AVD = 1,	RL = 10 kΩ		40		kHz

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at $V_{CC\pm}$ =± 15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2061Y			UNIT
				MIN	TYP	MAX	
φm	Phase margin at unity gain (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF		60°		
		RL = 600 Ω,	CL = 100 pF		70°		

5.17 TLE2062C Electrical Characteristics

at specified free-air temperature, $V_{CC\pm}$ = ± 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A [1]	TLE2062C TLE2062AC TLE2062BC			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2062C	V_{IC} = 0,	R_S = 50 Ω	25°C		0.1	5	mV
					Full range			5.9	
		TLE2062AC			25°C		0.1	4	
					Full range			4.9	
		TLE2062BC			25°C		0.1	3	
					Full range			3.9	
a_{VIO}	Temperature coefficient of input offset voltage				Full range		1		μV/°C
	Input offset voltage long-term drift[2]				25°C		0.04		μV/mo
I_{IO}	Input offset current				25°C		1		pA
					Full range			0.8	nA
I_{IB}	Input bias current				25°C		3		pA
					Full range			2	nA
V_{ICR}	Common-mode input voltage range				25°C	-1.6 to 4	-2 to 6		V
					Full range	-1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ		25°C	3.5	4.9		V
					Full range	3.3			
			R_L = 100 kΩ		25°C	2.5	4.5		V
					Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ		25°C	–3.7	–4.9		V
					Full range	–3.3			
			R_L = 100 kΩ		25°C	–2.5	–4.5		V
					Full range	–2			
A_{VD}	Large-signal differential voltage amplification		V_O = ±2.8 V	R_L = 10 Ω	25°C	15	225		V/mV
					Full range	2			
			V_O = 0 to 2 V	R_L = 100 Ω	25°C	0.75	225		
					Full range	0.5			
			V_O = 0 to -2 V	R_L = 100 Ω	25°C	0.5	225		
					Full range	0.25			
r_i	Input resistance				25°C		10^{12}		Ω
c_i	Input capacitance				25°C		4		pF
z_o	Open-loop output impedance		I_O = 0		25°C		280		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICRmin},	R_S = 50 Ω	25°C	65	82		dB
					Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ± 5 V to ± 15 V,		25°C	75	135		dB
			R_S = 50 Ω		Full range	75			

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5.17 TLE2062C Electrical Characteristics (continued)

at specified free-air temperature, $V_{CC\pm}$ = ± 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	TLE2062C TLE2062AC TLE2062BC			UNIT
					MIN	TYP	MAX	
I_{CC}	Supply current	V_O = 0,	No load	25°C		120	620	µA
				Full range			635	

(1) Full range is 0°C to 70°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV

5.18 TLE2062C Operating Characteristics

at specified free-air temperature, $V_{CC\pm}$ =± 5 V

PARAMETER		TEST CONDITIONS		TA(1)	TLE2062C TLE20612C TLE20612C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (See Figure 6-1)	RL = 10 kΩ,	CL = 100 pF	25°C	2.2	4		V/µs
				Full range	2.1			
V_n	Equivalent input noise voltage (See Figure 6-2)	f = 10 Hz,	RS = 20 Ω	25°C		59	100	nV/√Hz
		f = 1 kHz,	RS = 20 Ω			43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		µV
In	Equivalent input noise current	f = 1 kHz		25°C		1		fA/√Hz
THD	Total harmonic distortion	AVD = 2, VO(PP) = 2 V,	f = 10 kHz, RL = 10 kΩ	25°C		0.025%		
B1	Unity-gain bandwidth (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	25°C		1.8		MHz
		RL = 100 Ω, 0.1%	CL = 100 pF			1.3		
ts	Settling time	0.1%		25°C		5		µs
		0.01%				10		
BOM	Maximum output-swing bandwidth	AVD = 1,	RL = 10 kΩ	25°C		140		kHz
φm	Phase margin at unity gain (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	25°C		58°		
		RL = 100 Ω,	CL = 100 pF			75°		

(1) Full range is 0°C to 70°C.

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5.19 TLE2062C Electrical Characteristics

at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A [1]	TLE2062C TLE2062AC TLE2062BC			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2062C	V_{IC} = 0, R_S = 50 Ω	25°C		0.1	4	mV
				Full range			4.9	
		TLE2062AC		25°C		0.1	2	
				Full range			2.9	
		TLE2062BC		25°C		0.1	1	
				Full range			1.9	
a_{VIO}	Temperature coefficient of input offset voltage			Full range		1		µV/°C
	Input offset voltage long-term drift [2]			25°C		0.04		µV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			1	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			3	nA
V_{ICR}	Common-mode input voltage range			25°C	-11 to 13	-12 to 16		V
				Full range	-11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	13.2	14.9		V
				Full range	13			
			R_L = 600 Ω	25°C	12.5	14.5		V
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	–13.7	–14.9		V
				Full range	–13			
			R_L = 600 kΩ	25°C	–12.5	–14.5		V
				Full range	–12			
A_{VD}	Large-signal differential voltage amplification		V_O = ±10 V, R_L = 10 kΩ	25°C	30	225		V/mV
				Full range	20			
			V_O = 0 to 8 V, R_L = 600 Ω	25°C	25	225		
				Full range	10			
			V_O = 0 to -8 V, R_L = 600 Ω	25°C	3	225		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICRmin}, R_S = 50 Ω	25°C	72	90		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ± 5 V to ± 15 V,	25°C	75	93		dB
			R_S = 50 Ω	Full range	75			
I_{CC}	Supply current		V_O = 0, No load	25°C		275	690	µA
				Full range			715	

(1) Full range is 0°C to 70°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV

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5.20 TLE2062C Operating Characteristics

at specified free-air temperature, $V_{CC\pm}$ =± 15 V

PARAMETER		TEST CONDITIONS		TA[1]	TLE2062C TLE2062AC TLE2062BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (See Figure 6-1)	RL = 10 kΩ,	CL = 100 pF	25°C	2.6	4		V/µs
				Full range	2.5			
V_n	Equivalent input noise voltage (See Figure 6-2)	f = 10 Hz,	RS = 20 Ω	25°C		70	100	nV/√Hz
		f = 1 kHz,	RS = 20 Ω			40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		µV
In	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	AVD = 2, VO(PP) = 2 V,	f = 10 kHz, RL = 10 kΩ	25°C		0.025%		
B1	Unity-gain bandwidth (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	25°C		2		MHz
		RL = 600 Ω	CL = 100 pF			1.5		
ts	Settling time	0.1%		25°C		5		µs
		0.01%				10		
BOM	Maximum output-swing bandwidth	AVD = 1,	RL = 10 kΩ	25°C		40		kHz
φm	Phase margin at unity gain (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	25°C		60°		
		RL = 600 Ω,	CL = 100 pF			70°		

(1) Full range is 0°C to 70°C.

5.21 TLE2062I Electrical Characteristics

at specified free-air temperature, $V_{CC\pm}$ = ± 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A [1]	TLE2062I TLE2062AI TLE2062BI			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2062I	V_{IC} = 0,	R_S = 50 Ω	25°C		0.1	5	mV
					Full range			6.3	
		TLE2062AI			25°C		0.1	4	
					Full range			5.3	
		TLE2062BI			25°C		0.1	3	
					Full range			4.3	
a_{VIO}	Temperature coefficient of input offset voltage				Full range		1		µV/°C
	Input offset voltage long-term drift[2]				25°C		0.04		µV/mo
I_{IO}	Input offset current				25°C		1		pA
					Full range			2	nA
I_{IB}	Input bias current				25°C		3		pA
					Full range			4	nA
V_{ICR}	Common-mode input voltage range				25°C	-1.6 to 4	-2 to 6		V
					Full range	-1.6 to 4			V

5.21 TLE2062I Electrical Characteristics (continued)

at specified free-air temperature, $V_{CC\pm}$ = ± 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	TLE2062I TLE2062AI TLE2062BI			UNIT
					MIN	TYP	MAX	
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		25°C	3.5	4.9		V
				Full range	3.1			
		R_L = 100 kΩ		25°C	2.5	4.5		V
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		25°C	–3.7	–4.9		V
				Full range	–3.1			
		R_L = 100 kΩ		25°C	–2.5	–4.5		V
				Full range	–2			
A_{VD}	Large-signal differential voltage amplification	V_O = ±2.8 V	R_L = 10 Ω	25°C	15	225		V/mV
				Full range	2			
		V_O = 0 to 2 V	R_L = 100 Ω	25°C	0.75	225		
				Full range	0.5			
		V_O = 0 to -2 V	R_L = 100 Ω	25°C	0.5	225		
				Full range	0.25			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance	I_O = 0		25°C		280		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICRmin},	R_S = 50 Ω	25°C	65	82		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ± 5 V to ± 15 V,		25°C	75	135		dB
		R_S = 50 Ω		Full range	65			
I_{CC}	Supply current	V_O = 0,	No load	25°C		120	620	μA
				Full range			640	

(1) Full range is -40°C to 85°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV

5.22 TLE2062I Operating Characteristics

at specified free-air temperature, $V_{CC\pm}$ =± 5 V

PARAMETER		TEST CONDITIONS		TA(1)	TLE2062I TLE2062AI TLE2062BI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (See Figure 6-1)	RL = 10 kΩ,	CL = 100 pF	25°C	2.2	4		V/μs
				Full range	1.7			
V_n	Equivalent input noise voltage (See Figure 6-2)	f = 10 Hz,	RS = 20 Ω	25°C		59	100	nV/√Hz
		f = 1 kHz,	RS = 20 Ω			43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
In	Equivalent input noise current	f = 1 kHz		25°C		1		fA/√Hz
THD	Total harmonic distortion	AVD = 2, VO(PP) = 2 V,	f = 10 kHz, RL = 10 kΩ	25°C		0.025%		

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at specified free-air temperature, $V_{CC\pm}$ =± 5 V

PARAMETER		TEST CONDITIONS		TA(1)	TLE2062I TLE2062AI TLE2062BI			UNIT
					MIN	TYP	MAX	
B1	Unity-gain bandwidth (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	25°C		1.8		MHz
		RL = 100 Ω, 0.1%	CL = 100 pF			1.3		
ts	Settling time	0.1%		25°C		5		µs
		0.01%				10		
BOM	Maximum output-swing bandwidth	AVD = 1,	RL = 10 kΩ	25°C		140		kHz
φm	Phase margin at unity gain (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	25°C		58°		
		RL = 100 Ω,	CL = 100 pF			75°		

(1) Full range is -40°C to 85°C.

5.23 TLE2062I Electrical Characteristics

at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		TA (1)	TLE2062I TLE2062AI TLE2062BI			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2062I	V_{IC} = 0,	R_S = 50 Ω	25°C		0.1	4	mV
					Full range			5.3	
		TLE2062AI			25°C		0.1	2	
					Full range			3.3	
		TLE2062BI			25°C		0.1	1	
					Full range			2.3	
a_{VIO}	Temperature coefficient of input offset voltage				Full range		1		µV/°C
	Input offset voltage long-term drift(2)				25°C		0.04		µV/mo
I_{IO}	Input offset current				25°C		2		pA
					Full range			3	nA
I_{IB}	Input bias current				25°C		4		pA
					Full range			5	nA
V_{ICR}	Common-mode input voltage range				25°C	-11 to 13	-12 to 16		V
					Full range	-11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ		25°C	13.2	14.9		V
					Full range	13			
			R_L = 600 Ω		25°C	12.5	14.5		V
					Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ		25°C	–13.2	–14.9		V
					Full range	–13			
			R_L = 600 kΩ		25°C	–12.5	–14.5		V
					Full range	–12			

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5.23 TLE2062I Electrical Characteristics (continued)

at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	TLE2062I TLE2062AI TLE2062BI			UNIT
					MIN	TYP	MAX	
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V	R_L = 10 kΩ	25°C	30	225		V/mV
				Full range	20			
		V_O = 0 to 8 V	R_L = 600 Ω	25°C	25	225		
				Full range	10			
		V_O = 0 to -8 V	R_L = 600 Ω	25°C	3	225		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance	I_O = 0		25°C		280		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICRmin},	R_S = 50 Ω	25°C	72	90		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ± 5 V to ± 15 V,		25°C	75	93		dB
		R_S = 50 Ω		Full range	65			
I_{CC}	Supply current	V_O = 0,	No load	25°C		275	690	μA
				Full range			720	

(1) Full range is -40°C to 85°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV

5.24 TLE2062I Operating Characteristics

at specified free-air temperature, $V_{CC\pm}$ =± 15 V

PARAMETER		TEST CONDITIONS		TA(1)	TLE2062I TLE2062AI TLE2062BI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (See Figure 6-1)	RL = 10 kΩ,	CL = 100 pF	25°C	2.6	4		V/μs
				Full range	2.1			
V_n	Equivalent input noise voltage (See Figure 6-2)	f = 10 Hz,	RS = 20 Ω	25°C		70	100	nV/√Hz
		f = 1 kHz,	RS = 20 Ω			40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
In	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	AVD = 2, VO(PP) = 2 V,	f = 10 kHz, RL = 10 kΩ	25°C		0.025%		
B1	Unity-gain bandwidth (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	25°C		2		MHz
		RL = 600 Ω	CL = 100 pF			1.5		
ts	Settling time	0.1%		25°C		5		μs
		0.01%				10		
BOM	Maximum output-swing bandwidth	AVD = 1,	RL = 10 kΩ	25°C		40		kHz

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at specified free-air temperature, $V_{CC\pm}$ =± 15 V

PARAMETER		TEST CONDITIONS		TA(1)	TLE2062I TLE2062AI TLE2062BI			UNIT
					MIN	TYP	MAX	
φm	Phase margin at unity gain (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	25°C		60°		
		RL = 600 Ω,	CL = 100 pF			70°		

(1) Full range is -40°C to 85°C.

5.25 TLE2062M Electrical Characteristics

at specified free-air temperature, $V_{CC\pm}$ = ± 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A (1)	TLE2062M TLE2062AM TLE2062BM			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2062M	V_{IC} = 0,	R_S = 50 Ω	25°C		1	5	mV
					Full range			7	
		TLE2062AM			25°C		0.9	4	
					Full range			6	
		TLE2062BM			25°C		0.7	3	
					Full range			5	
a_{VIO}	Temperature coefficient of input offset voltage				Full range		6		µV/°C
	Input offset voltage long-term drift(2)				25°C		0.04		µV/mo
I_{IO}	Input offset current				25°C		1		pA
					Full range			15	nA
I_{IB}	Input bias current				25°C		3		pA
					Full range			30	nA
V_{ICR}	Common-mode input voltage range				25°C	-1.6 to 4	-2 to 6		V
					Full range	-1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ		25°C	3.5	3.7		V
					Full range	3			
			R_L = 600 kΩ		25°C	2.5	3.6		
					Full range	2			
			R_L = 100 kΩ		25°C	2.5	3.1		V
					Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ		25°C	–3.5	–3.9		V
					Full range	–3			
		FK and JG packages	R_L = 600 Ω		25°C	–2.5	–3.5		
					Full range	–2			
		D and P packages	R_L = 100 Ω		25°C	–2.5	–2.7		V
					Full range	–2			

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5.25 TLE2062M Electrical Characteristics (continued)

at specified free-air temperature, $V_{CC\pm}$ = ± 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A (1)	TLE2062M TLE2062AM TLE2062BM			UNIT
						MIN	TYP	MAX	
A_{VD}	Large-signal differential voltage amplification		V_O = ±2.8 V	R_L = 10 kΩ	25°C	15	80		V/mV
					Full range	2			
		FK and JG packages	V_O = 0 to 2.5 V	R_L = 600 Ω	25°C	1	65		
					Full range	0.5			
			V_O = 0 to -2.5 V	R_L = 600 Ω	25°C	1	16		
					Full range	0.5			
		D and P packages	V_O = 0 to 2 V	R_L = 100 Ω	25°C	0.75	45		
					Full range	0.5			
			V_O = 0 to -2 V	R_L = 100 Ω	25°C	0.5	3		
					Full range	0.25			
r_i	Input resistance				25°C		10^{12}		Ω
c_i	Input capacitance				25°C		4		pF
z_o	Open-loop output impedance		I_O = 0		25°C		560		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICRmin},	R_S = 50 Ω	25°C	65	82		dB
					Full range	60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ± 5 V to ± 15 V,		25°C	75	93		dB
			R_S = 50 Ω		Full range	65			
I_{CC}	Supply current		V_O = 0,	No load	25°C		560	620	μA
					Full range			650	

(1) Full range is -55°C to 125°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV

5.26 TLE2062M Operating Characteristics

at specified free-air temperature, T_A = 25°C, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		TLE2062M TLE2062AM TLE2062BM			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain (See Figure 6-1)	RL = 10 kΩ,	CL = 100 pF		4		V/μs
V_n	Equivalent input noise voltage (See Figure 6-2)	f = 10 Hz,	RS = 20 Ω		59		nV/√Hz
		f = 1 kHz,	RS = 20 Ω		43		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			1.1		μV
In	Equivalent input noise current	f = 1 kHz			1		fA/√Hz
THD	Total harmonic distortion	AVD = 2, VO(PP) = 2 V,	f = 10 kHz, RL = 10 kΩ		0.025%		
B1	Unity-gain bandwidth (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF		1.8		MHz
		RL = 100 Ω, 0.1%	CL = 100 pF		1.3		
ts	Settling time	0.1%			5		μs
		0.01%			10		
BOM	Maximum output-swing bandwidth	AVD = 1,	RL = 10 kΩ		140		kHz

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at specified free-air temperature, T_A = 25°C, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		TLE2062M TLE2062AM TLE2062BM			UNIT
				MIN	TYP	MAX	
φm	Phase margin at unity gain (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF		58°		
		RL = 100 Ω,	CL = 100 pF		75°		

5.27 TLE2062M Electrical Characteristics

at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A [1]	TLE2062M TLE2062AM TLE2062BM			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2062M	V_{IC} = 0, R_S = 50 Ω	25°C		0.1	4	mV
				Full range			6	
		TLE2062AM		25°C		0.1	2	
				Full range			4	
		TLE2062BM		25°C		0.1	1	
				Full range			3	
a_{VIO}	Temperature coefficient of input offset voltage			Full range		1		µV/°C
	Input offset voltage long-term drift [2]			25°C		0.04		µV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			20	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			40	nA
V_{ICR}	Common-mode input voltage range			25°C	-11 to 13	-12 to 16		V
				Full range	-11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	13	14.9		V
				Full range	12.5			
			R_L = 600 Ω	25°C	12.5	14.5		V
				Full range	11			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	–13	–14.9		V
				Full range	–12.5			
			R_L = 600 kΩ	25°C	–12.5	–14.5		V
				Full range	–11			
A_{VD}	Large-signal differential voltage amplification		V_O = ±10 V R_L = 10 kΩ	25°C	30	225		V/mV
				Full range	20			
			V_O = 0 to 8 V R_L = 600 Ω	25°C	25	225		
				Full range	7			
			V_O = 0 to -8 V R_L = 600 Ω	25°C	3	225		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICRmin}, R_S = 50 Ω	25°C	72	90		dB
				Full range	65			

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5.27 TLE2062M Electrical Characteristics (continued)

at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A (1)	TLE2062M TLE2062AM TLE2062BM			UNIT
				MIN	TYP	MAX	
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ± 5 V to ± 15 V, R_S = 50 Ω	25°C	75	93		dB
			Full range	65			
I_{CC}	Supply current	V_O = 0, No load	25°C		275	690	µA
			Full range			730	

(1) Full range is -55°C to 125°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV

5.28 TLE2062M Operating Characteristics

at specified free-air temperature, $V_{CC\pm}$ =± 15 V

PARAMETER		TEST CONDITIONS		TA(1)	TLE2062M TLE2062AM TLE2062BM			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (See Figure 6-1)	RL = 10 kΩ,	CL = 100 pF	25°C	2.6	4		V/µs
				Full range	1.8			
V_n	Equivalent input noise voltage (See Figure 6-2)	f = 10 Hz,	RS = 20 Ω	25°C		70		nV/√Hz
		f = 1 kHz,	RS = 20 Ω			40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		µV
In	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	AVD = 2, VO(PP) = 2 V,	f = 10 kHz, RL = 10 kΩ	25°C		0.025%		
B1	Unity-gain bandwidth (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	25°C		2		MHz
		RL = 600 Ω	CL = 100 pF			1.5		
ts	Settling time	0.1%		25°C		5		µs
		0.01%				10		
BOM	Maximum output-swing bandwidth	AVD = 1,	RL = 10 kΩ	25°C		40		kHz
φm	Phase margin at unity gain (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	25°C		60°		
		RL = 600 Ω,	CL = 100 pF			70°		

(1) Full range is -55°C to 125°C.

5.29 TLE2062Y Electrical Characteristics

at $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLE2062Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0,	R_S = 50 Ω		0.9	4	mV
	Input offset voltage long-term drift(1)				0.04		µV/mo
I_{IO}	Input offset current				2		pA
I_{IB}	Input bias current				4		pA

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5.29 TLE2062Y Electrical Characteristics (continued)

at $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLE2062Y			UNIT
				MIN	TYP	MAX	
V_{ICR}	Common-mode input voltage range			-11 to 13	-12 to 16		V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		13.2	13.7		V
		R_L = 600 Ω		12.5	13.2		V
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		–13.2	–13.7		V
		R_L = 600 kΩ		–12.5	-13		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V	R_L = 10 kΩ	30	230		V/mV
		V_O = 0 to 8 V	R_L = 600 Ω	25	100		
		V_O = 0 to -8 V	R_L = 600 Ω	3	25		
r_i	Input resistance				10^{12}		Ω
c_i	Input capacitance				4		pF
z_o	Open-loop output impedance	I_O = 0			560		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICRmin},	R_S = 50 Ω	72	90		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ± 5 V to ± 15 V,		75	93		dB
I_{CC}	Supply current	V_O = 0,	No load		625	690	μA

(1) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV

5.30 TLE2062Y Operating Characteristics

at $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2062Y			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain (See Figure 6-1)	RL = 10 kΩ,	CL = 100 pF	2.6	3.4	4	V/μs
V_n	Equivalent input noise voltage (See Figure 6-2)	f = 10 Hz,	RS = 20 Ω		70		nV/√Hz
		f = 1 kHz,	RS = 20 Ω		40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			1.1		μV
In	Equivalent input noise current	f = 1 Hz			1.1		fA/√Hz
THD	Total harmonic distortion	AVD = 2, VO(PP) = 2 V,	f = 10 kHz, RL = 10 kΩ		0.025%		
B1	Unity-gain bandwidth (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF		2		MHz
		RL = 600 Ω	CL = 100 pF		1.5		
ts	Settling time	0.1%			5		μs
		0.01%			10		
BOM	Maximum output-swing bandwidth	AVD = 1,	RL = 10 kΩ		40		kHz
φm	Phase margin at unity gain (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF		60°		
		RL = 600 Ω,	CL = 100 pF		70°		

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5.31 TLE2064C Electrical Characteristics

at specified free-air temperature, $V_{CC\pm}$ = ± 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A [1]	TLE2064C TLE2064AC TLE2064BC			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2064C	V_{IC} = 0, R_S = 50 Ω	25°C		0.1	7	mV
				Full range			7.9	
		TLE2064AC		25°C		0.1	6	
				Full range			6.9	
		TLE2064BC		25°C		0.1	3.5	
				Full range			4.4	
a_{VIO}	Temperature coefficient of input offset voltage			Full range		1		μV/°C
	Input offset voltage long-term drift [2]			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			0.8	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			2	nA
V_{ICR}	Common-mode input voltage range			25°C	-1.6 to 4	-2 to 6		V
				Full range	-1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	3.5	4.9		V
				Full range	3.3			
			R_L = 100 kΩ	25°C	2.5	4.5		V
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	–3.7	–4.9		V
				Full range	–3.3			
			R_L = 100 kΩ	25°C	–2.5	–4.5		V
				Full range	–2			
A_{VD}	Large-signal differential voltage amplification		V_O = ±2.8 V, R_L = 10 Ω	25°C	15	225		V/mV
				Full range	2			
			V_O = 0 to 2 V, R_L = 100 Ω	25°C	0.75	225		
				Full range	0.5			
			V_O = 0 to -2 V, R_L = 100 Ω	25°C	0.5	225		
				Full range	0.15			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICRmin}, R_S = 50 Ω	25°C	65	82		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ± 5 V to ± 15 V, R_S = 50 Ω	25°C	75	135		dB
				Full range	75			
I_{CC}	Supply current (four amplifiers)		V_O = 0, No load	25°C		0.6	1.3	mA
				Full range			1.3	

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5.31 TLE2064C Electrical Characteristics (continued)

at specified free-air temperature, $V_{CC\pm}$ = ± 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	TLE2064C TLE2064AC TLE2064BC			UNIT
					MIN	TYP	MAX	
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 1000,	f = 1 kHz	25°C		120		dB

(1) Full range is 0°C to 70°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV

5.32 TLE2064C Operating Characteristics

at specified free-air temperature, $V_{CC\pm}$ =± 5 V

PARAMETER		TEST CONDITIONS		TA(1)	TLE2064C TLE2064AC TLE2064BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (See Figure 6-1)	RL = 10 kΩ,	CL = 100 pF	25°C	2.2	4		V/µs
				Full range	2.1			
V_n	Equivalent input noise voltage (See Figure 6-2)	f = 10 Hz,	RS = 20 Ω	25°C		59	100	nV/√Hz
		f = 1 kHz,	RS = 20 Ω			43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		µV
In	Equivalent input noise current	f = 1 kHz		25°C		1		fA/√Hz
THD	Total harmonic distortion	AVD = 2, VO(PP) = 2 V,	f = 10 kHz, RL = 10 kΩ	25°C		0.025%		
B1	Unity-gain bandwidth (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	25°C		1.8		MHz
		RL = 100 Ω, 0.1%	CL = 100 pF			1.3		
ts	Settling time	0.1%		25°C		5		µs
		0.01%				10		
BOM	Maximum output-swing bandwidth	AVD = 1,	RL = 10 kΩ	25°C		140		kHz
φm	Phase margin at unity gain (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	25°C		58°		
		RL = 100 Ω,	CL = 100 pF			75°		

(1) Full range is 0°C to 70°C.

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5.33 TLE2064C Electrical Characteristics

at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A [1]	TLE2064C TLE2064AC TLE2064BC			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2064C	V_{IC} = 0, R_S = 50 Ω	25°C		0.1	6	mV
				Full range			6.9	
		TLE2064AC		25°C		0.1	4	
				Full range			4.9	
		TLE2064BC		25°C		0.1	2	
				Full range			4	
a_{VIO}	Temperature coefficient of input offset voltage			Full range		1		µV/°C
	Input offset voltage long-term drift [2]			25°C		0.04		µV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			1	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			3	nA
V_{ICR}	Common-mode input voltage range			25°C	-11 to 13	-12 to 16		V
				Full range	-11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	13.2	14.9		V
				Full range	13			
			R_L = 600 Ω	25°C	12.5	14.5		V
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	–13.2	–14.9		V
				Full range	–13			
			R_L = 600 kΩ	25°C	–12.5	–14.5		V
				Full range	–12			
A_{VD}	Large-signal differential voltage amplification		V_O = ±10 V, R_L = 10 kΩ	25°C	30	225		V/mV
				Full range	20			
			V_O = 0 to 8 V, R_L = 600 Ω	25°C	25	225		
				Full range	10			
			V_O = 0 to -8 V, R_L = 600 Ω	25°C	3	225		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICRmin}, R_S = 50 Ω	25°C	72	90		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ± 5 V to ± 15 V,	25°C	75	93		dB
			R_S = 50 Ω	Full range	75			
I_{CC}	Supply current (four amplifiers)		V_O = 0, No load	25°C		0.6	1.4	µA
				Full range			1.5	

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5.33 TLE2064C Electrical Characteristics (continued)

at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	TLE2064C TLE2064AC TLE2064BC			UNIT
					MIN	TYP	MAX	
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 1000,	f = 1 kHz	25°C		120		dB

(1) Full range is 0°C to 70°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV

5.34 TLE2064C Operating Characteristics

at specified free-air temperature, $V_{CC\pm}$ =± 15 V

PARAMETER		TEST CONDITIONS		TA(1)	TLE2064C TLE2064AC TLE2064BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (See Figure 6-1)	RL = 10 kΩ,	CL = 100 pF	25°C	2.6	4		V/µs
				Full range	2.5			
V_n	Equivalent input noise voltage (See Figure 6-2)	f = 10 Hz,	RS = 20 Ω	25°C		70	100	nV/√Hz
		f = 1 kHz,	RS = 20 Ω			40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		µV
In	Equivalent input noise current	f = 1 kHz		25°C		1		fA/√Hz
THD	Total harmonic distortion	AVD = 2, VO(PP) = 2 V,	f = 10 kHz, RL = 10 kΩ	25°C		0.025%		
B1	Unity-gain bandwidth (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	25°C		2		MHz
		RL = 600 Ω	CL = 100 pF			1.5		
ts	Settling time	0.1%		25°C		5		µs
		0.01%				10		
BOM	Maximum output-swing bandwidth	AVD = 1,	RL = 10 kΩ	25°C		40		kHz
φm	Phase margin at unity gain (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	25°C		50°		
		RL = 600 Ω,	CL = 100 pF			70°		

(1) Full range is 0°C to 70°C.

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5.35 TLE2064I Electrical Characteristics

at specified free-air temperature, $V_{CC\pm}$ = ± 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A [1]	TLE2064I TLE2064AI TLE2064BI			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2064I	V_{IC} = 0, R_S = 50 Ω	25°C		0.1	7	mV
				Full range			8.3	
		TLE2064AI		25°C		0.1	6	
				Full range			7.3	
		TLE2064BI		25°C		0.1	3.5	
				Full range			4.8	
a_{VIO}	Temperature coefficient of input offset voltage			Full range		1		µV/°C
	Input offset voltage long-term drift[2]			25°C		0.04		µ V/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			2	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			4	nA
V_{ICR}	Common-mode input voltage range			25°C	-1.6 to 4	-2 to 6		V
				Full range	-1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	3.5	4.9		V
				Full range	3.1			
			R_L = 100 kΩ	25°C	2.5	4.5		V
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	–3.7	–4.9		V
				Full range	–3.1			
			R_L = 100 kΩ	25°C	–2.5	–4.5		V
				Full range	–2			
A_{VD}	Large-signal differential voltage amplification		V_O = ±2.8 V, R_L = 10 Ω	25°C	15	225		V/mV
				Full range	2			
			V_O = 0 to 2 V, R_L = 100 Ω	25°C	0.75	225		
				Full range	0.5			
			V_O = 0 to -2 V, R_L = 100 Ω	25°C	0.5	225		
				Full range	0.15			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICRmin}, R_S = 50 Ω	25°C	65	82		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ± 5 V to ± 15 V, R_S = 50 Ω	25°C	75	135		dB
				Full range	65			
I_{CC}	Supply current (four amplifiers)		V_O = 0, No load	25°C		0.6	1.3	mA
				Full range			1.3	

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5.35 TLE2064I Electrical Characteristics (continued)

at specified free-air temperature, $V_{CC\pm}$ = ± 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	TLE2064I TLE2064AI TLE2064BI			UNIT
					MIN	TYP	MAX	
V_{O1}/ V_{O2}	Crosstalk attenuation	A_{VD} = 1000,	f = 1 kHz	25°C		120		dB

(1) Full range is -40°C to 85°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV

5.36 TLE2064I Operating Characteristics

at specified free-air temperature, $V_{CC\pm}$ =± 5 V

PARAMETER		TEST CONDITIONS		TA(1)	TLE2064I TLE2064AI TLE2064BI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (See Figure 6-1)	RL = 10 kΩ,	CL = 100 pF	25°C	2.2	4		V/µs
				Full range	1.7			
V_n	Equivalent input noise voltage (See Figure 6-2)	f = 10 Hz,	RS = 20 Ω	25°C		59	100	nV/√Hz
		f = 1 kHz,	RS = 20 Ω			43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		µV
In	Equivalent input noise current	f = 1 kHz		25°C		1		fA/√Hz
THD	Total harmonic distortion	AVD = 2, VO(PP) = 2 V,	f = 10 kHz, RL = 10 kΩ	25°C		0.025%		
B1	Unity-gain bandwidth (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	25°C		1.8		MHz
		RL = 100 Ω, 0.1%	CL = 100 pF			1.3		
ts	Settling time	0.1%		25°C		5		µs
		0.01%				10		
BOM	Maximum output-swing bandwidth	AVD = 1,	RL = 10 kΩ	25°C		140		kHz
φm	Phase margin at unity gain (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	25°C		58°		
		RL = 100 Ω,	CL = 100 pF			75°		

(1) Full range is -40°C to 85°C.

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5.37 TLE2064I Electrical Characteristics

at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A (1)	TLE2064I TLE2064AI TLE2064BI			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2064I	V_{IC} = 0, R_S = 50 Ω	25°C		0.1	6	mV
				Full range			7.3	
		TLE2064AI		25°C		0.1	4	
				Full range			5.3	
		TLE2064BI		25°C		0.1	2	
				Full range			3.3	
a_{VIO}	Temperature coefficient of input offset voltage			Full range		1		µV/°C
	Input offset voltage long-term drift (2)			25°C		0.04		µV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			3	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			5	nA
V_{ICR}	Common-mode input voltage range			25°C	-11 to 13	-12 to 16		V
				Full range	-11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	13.2	14.9		V
				Full range	13			
			R_L = 600 Ω	25°C	12.5	14.5		V
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	–13.2	–14.9		V
				Full range	–13			
			R_L = 600 kΩ	25°C	–12.5	–14.5		V
				Full range	–12			
A_{VD}	Large-signal differential voltage amplification		V_O = ±10 V, R_L = 10 kΩ	25°C	30	225		V/mV
				Full range	20			
			V_O = 0 to 8 V, R_L = 600 Ω	25°C	25	225		
				Full range	10			
			V_O = 0 to -8 V, R_L = 600 Ω	25°C	3	225		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICRmin}, R_S = 50 Ω	25°C	72	90		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ± 5 V to ± 15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	65			
I_{CC}	Supply current (four amplifiers)		V_O = 0, No load	25°C		0.6	1.4	mA
				Full range			1.5	
V_{O1}/V_{O2}	Crosstalk attenuation		A_{VD} = 1000, f = 1 kHz	25°C		120		dB

(1) Full range is -40°C to 85°C.

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(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV

5.38 TLE2064I Operating Characteristics

at specified free-air temperature, $V_{CC\pm}$ =± 15 V

PARAMETER		TEST CONDITIONS		TA(1)	TLE2064I TLE2064AI TLE2064BI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (See Figure 6-1)	RL = 10 kΩ,	CL = 100 pF	25°C	2.6	4		V/µs
				Full range	2.1			
V_n	Equivalent input noise voltage (See Figure 6-2)	f = 10 Hz,	RS = 20 Ω	25°C		70	100	nV/√Hz
		f = 1 kHz,	RS = 20 Ω			40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		µV
In	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	AVD = 2, VO(PP) = 2 V,	f = 10 kHz, RL = 10 kΩ	25°C		0.025%		
B1	Unity-gain bandwidth (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	25°C		2		MHz
		RL = 600 Ω	CL = 100 pF			1.5		
ts	Settling time	0.1%		25°C		5		µs
		0.01%				10		
BOM	Maximum output-swing bandwidth	AVD = 1,	RL = 10 kΩ	25°C		40		kHz
φm	Phase margin at unity gain (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	25°C		60°		
		RL = 600 Ω,	CL = 100 pF			70°		

(1) Full range is -40°C to 85°C.

5.39 TLE2064M Electrical Characteristics

at specified free-air temperature, $V_{CC\pm}$ = ± 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A (1)	TLE2064M TLE2064AM TLE2064BM			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2064M	V_{IC} = 0,	R_S = 50 Ω	25°C		1.2	7	mV
					Full range			9	
		TLE2064AM			25°C		1.2	6	
					Full range			8	
		TLE2064BM			25°C		0.8	3.5	
					Full range			5.5	
a_{VIO}	Temperature coefficient of input offset voltage				Full range		6		µV/°C
	Input offset voltage long-term drift(2)				25°C		0.04		µ V/mo
I_{IO}	Input offset current				25°C		1		pA
					Full range			15	nA
I_{IB}	Input bias current				25°C		3		pA
					Full range			30	nA
V_{ICR}	Common-mode input voltage range				25°C	-1.6 to 4	-2 to 6		V
					Full range	-1.6 to 4			V

5.39 TLE2064M Electrical Characteristics (continued)

at specified free-air temperature, $V_{CC\pm}$ = ± 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A (1)	TLE2064M TLE2064AM TLE2064BM			UNIT
					MIN	TYP	MAX	
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	3.5	3.7		V
				Full range	3			
			R_L = 600 kΩ	25°C	2.5	3.6		
				Full range	2			
			R_L = 100 kΩ	25°C	2.5	3.1		V
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	-3.5	-3.9		V
				Full range	-3			
		FK and JG packages	R_L = 600 Ω	25°C	-2.5	-3.5		
				Full range	-2			
		D and P packages	R_L = 100 Ω	25°C	–2.5	–2.7		V
				Full range	–2			
A_{VD}	Large-signal differential voltage amplification		V_O = ±2.8 V R_L = 10 kΩ	25°C	15	80		V/mV
				Full range	2			
		FK and JG packages	V_O = 0 to 2.5 V R_L = 600 Ω	25°C	1	65		
				Full range	0.5			
			V_O = 0 to -2.5 V R_L = 600 Ω	25°C	1	16		
				Full range	0.5			
		D and P packages	V_O = 0 to 2 V R_L = 100 Ω	25°C	0.75	45		
				Full range	0.25			
			V_O = 0 to -2 V R_L = 100 Ω	25°C	0.4	3		
				Full range	0.15			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		560		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICRmin}, R_S = 50 Ω	25°C	65	82		dB
				Full range	60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ± 5 V to ± 15 V,	25°C	75	93		dB
			R_S = 50 Ω	Full range	65			
I_{CC}	Supply current (four amplifiers)		V_O = 0, No load	25°C		1.12	1.3	mA
				Full range			1.3	
ΔI_{CC}	Supply-current change over operating temperature range (four amplifiers)			Full range		144		µA
V_{O1}/V_{O2}	Crosstalk attenuation		A_{VD} = 1000, f = 1 kHz	25°C		120		dB

(1) Full range is -55°C to 125°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV

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5.40 TLE2064M Operating Characteristics

, $V_{CC\pm}$ = ±5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TA	TLE2064M TLE2064AM TLE2064BM			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (See Figure 6-1)	RL = 10 kΩ,	CL = 100 pF	25°C		4		V/µs
V_n	Equivalent input noise voltage (See Figure 6-2)	f = 10 Hz,	RS = 20 Ω	Full range		59		nV/√Hz
		f = 1 kHz,	RS = 20 Ω	25°C		43		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		µV
In	Equivalent input noise current	f = 1 kHz		25°C		1		fA/√Hz
THD	Total harmonic distortion	AVD = 2, VO(PP) = 2 V,	f = 10 kHz, RL = 10 kΩ	25°C		0.025%		
B1	Unity-gain bandwidth (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	25°C		1.8		MHz
		RL = 100 Ω, 0.1%	CL = 100 pF	25°C		1.3		
ts	Settling time	0.1%		25°C		5		µs
		0.01%		25°C		10		
BOM	Maximum output-swing bandwidth	AVD = 1,	RL = 10 kΩ	25°C		140		kHz
φm	Phase margin at unity gain (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	Full range		58°		
		RL = 100 Ω,	CL = 100 pF	25°C		75°		

5.41 TLE2064M Electrical Characteristics

at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A (1)	TLE2064M TLE2064AM TLE2064BM			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2064M	V_{IC} = 0,	R_S = 50 Ω	25°C		0.1	6	mV
					Full range			8	
		TLE2064AM			25°C		0.1	4	
					Full range			6	
		TLE2064BM			25°C		0.1	2	
					Full range			4	
a_{VIO}	Temperature coefficient of input offset voltage				Full range		1		µV/°C
	Input offset voltage long-term drift (2)				25°C		0.04		µ V/mo
I_{IO}	Input offset current				25°C		2		pA
					Full range			20	nA
I_{IB}	Input bias current				25°C		4		pA
					Full range			40	nA
V_{ICR}	Common-mode input voltage range				25°C	-11 to 13	-12 to 16		V
					Full range	-11 to 13			V

5.41 TLE2064M Electrical Characteristics (continued)

at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A (1)	TLE2064M TLE2064AM TLE2064BM			UNIT
				MIN	TYP	MAX	
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	13	14.9		V
			Full range	12.5			
		R_L = 600 Ω	25°C	12.5	14.5		V
			Full range	12			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ	25°C	–13	–14.9		V
			Full range	–12.5			
		R_L = 600 kΩ	25°C	–13	–14.5		V
			Full range	–12.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V R_L = 10 kΩ	25°C	30	225		V/mV
			Full range	20			
		V_O = 0 to 8 V R_L = 600 Ω	25°C	25	225		
			Full range	7			
		V_O = 0 to -8 V R_L = 600 Ω	25°C	3	225		
			Full range	1			
r_i	Input resistance		25°C		10^{12}		Ω
c_i	Input capacitance		25°C		4		pF
z_o	Open-loop output impedance	I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICRmin}, R_S = 50 Ω	25°C	72	90		dB
			Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ± 5 V to ± 15 V,	25°C	75	93		dB
		R_S = 50 Ω	Full range	65			
I_{CC}	Supply current (four amplifiers)	V_O = 0, No load	25°C		0.6	1.4	mA
			Full range			1.5	
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 1000, f = 1 kHz	25°C		120		dB

(1) Full range is -55°C to 125°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV

5.42 TLE2064M Operating Characteristics

at specified free-air temperature, $V_{CC\pm}$ =± 15 V

PARAMETER		TEST CONDITIONS		TA(1)	TLE2064M TLE2064AM TLE2064BM			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (See Figure 6-1)	RL = 10 kΩ,	CL = 100 pF	25°C	2.6	4		V/µs
				Full range	1.8			
V_n	Equivalent input noise voltage (See Figure 6-2)	f = 10 Hz,	RS = 20 Ω	25°C		70		nV/√Hz
		f = 1 kHz,	RS = 20 Ω			40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		µV
In	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz

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at specified free-air temperature, $V_{CC\pm}$ =± 15 V

PARAMETER		TEST CONDITIONS		TA[1]	TLE2064M TLE2064AM TLE2064BM			UNIT
					MIN	TYP	MAX	
THD	Total harmonic distortion	AVD = 2, VO(PP) = 2 V,	f = 10 kHz, RL = 10 kΩ	25°C		0.025%		
B1	Unity-gain bandwidth (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	25°C		2		MHz
		RL = 600 Ω	CL = 100 pF			1.5		
ts	Settling time	0.1%		25°C		5		µs
		0.01%				10		
BOM	Maximum output-swing bandwidth	AVD = 1,	RL = 10 kΩ	25°C		40		kHz
φm	Phase margin at unity gain (See Figure 6-3)	RL = 10 kΩ,	CL = 100 pF	25°C		60°		
		RL = 600 Ω,	CL = 100 pF			70°		

(1) Full range is -55°C to 125°C.

5.43 TLE2064Y Electrical Characteristics

at $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLE2064Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0,	R_S = 50 Ω		0.9	6	mV
	Input offset voltage long-term drift (1)				0.04		µ V/mo
I_{IO}	Input offset current				2		pA
I_{IB}	Input bias current				4		pA
V_{ICR}	Common-mode input voltage range			-11 to 13	-12 to 16		V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		13.2	13.7		V
		R_L = 600 Ω		12.5	13.2		
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		–13.2	–13.7		V
		R_L = 600 kΩ		12.5	13		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V	R_L = 10 kΩ	30	230		V/mV
		V_O = 0 to 8 V	R_L = 600 Ω	25	100		
		V_O = 0 to -8 V	R_L = 600 Ω	3	25		
r_i	Input resistance				10^{12}		Ω
c_i	Input capacitance				4		pF
z_o	Open-loop output impedance	I_O = 0			560		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICRmin},	R_S = 50 Ω	72	90		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ± 5 V to ± 15 V,		75	93		dB
I_{CC}	Supply current	V_O = 0,	No load		1.25	1.4	mA
V_{O1}/ V_{O2}	Crosstalk attenuation	A_{VD} = 1000,	f = 1 kHz		120		dB

(1) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV

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5.44 TLE2064Y Operating Characteristics

at $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2064Y			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	RL = 10 kΩ,	CL = 100 pF	2.6	3.4		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	RS = 20 Ω		70		nV/√Hz
		f = 1 kHz,	RS = 20 Ω		40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			1.1		μV
In	Equivalent input noise current	f = 1 Hz			1.1		fA/√Hz
THD	Total harmonic distortion	AVD = 2, VO(PP) = 2 V,	f = 10 kHz, RL = 10 kΩ		0.025%		
B1	Unity-gain bandwidth (see Figure 3)	RL = 10 kΩ,	CL = 100 pF		2		MHz
		RL = 600 Ω	CL = 100 pF		1.5		
ts	Settling time	0.1%			5		μs
		0.01%			10		
BOM	Maximum output-swing bandwidth	AVD = 1,	RL = 10 kΩ		40		kHz
φm	Phase margin at unity gain (see Figure 3)	RL = 10 kΩ,	CL = 100 pF		60°		
		RL = 600 Ω,	CL = 100 pF		70°		

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5.45 Typical Characteristics

Table 5-1. Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	4, 5, 6
I_{IB}	Input bias current	vs Common-mode input voltage vs Free-air temperature	7, 8
I_{IO}	Input offset current	vs Free-air temperature	8
V_{ICR}	Common-mode input voltage	vs Free-air temperature	9
V_{OM}	Maximum peak output voltage	vs Output current vs Supply voltage	10, 11, 12, 13, 14
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency vs Load resistance	15, 16, 17
A_{VD}	Large-signal differential voltage amplification	vs Frequency vs Free-air temperature	18, 19
I_{OS}	Short-circuit output current	vs Elasped time vs Free-air temperature	20, 21
z_o	Output impedance	vs Frequency	22, 23
CMRR	Common-mode rejection ratio	vs Frequency	24
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	25, 26, 27, 28, 29, 30
	Voltage-follower small-signal pulse response	vs Time	31, 32
	Voltage-follower large-signal pulse response	vs Time	33, 34
	Noise voltage (referred to input)	0.1 to 10 Hz	35
V_n	Equivalent input noise voltage	vs Frequency	36
THD	Total harmonic distortion	vs Frequency	37, 38
B_1	Unity-gain bandwidth	vs Supply voltage vs Free-air temperature	39, 40
φ_m	Phase margin	vs Supply voltage vs Load capacitance vs Free-air temperature	41, 42, 43
	Phase shift	vs Frequency	18

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5.46 Typical Characteristics

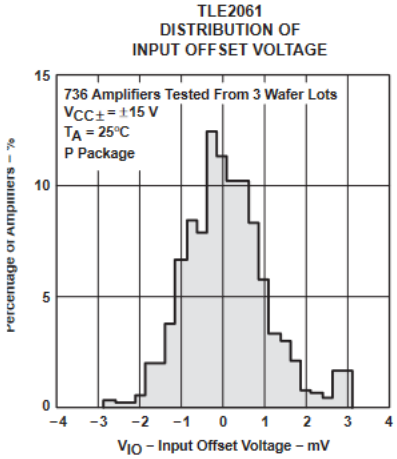

Figure 5-1.

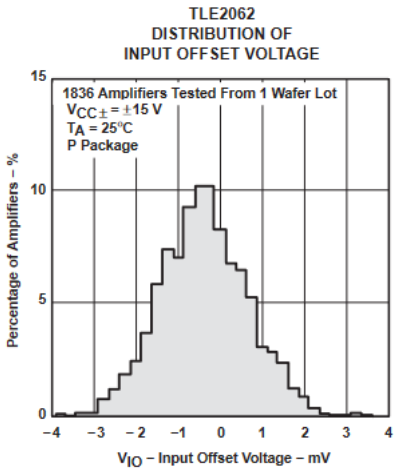

Figure 5-2.

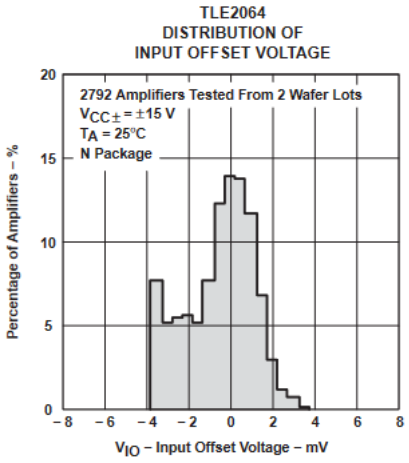

Figure 5-3.

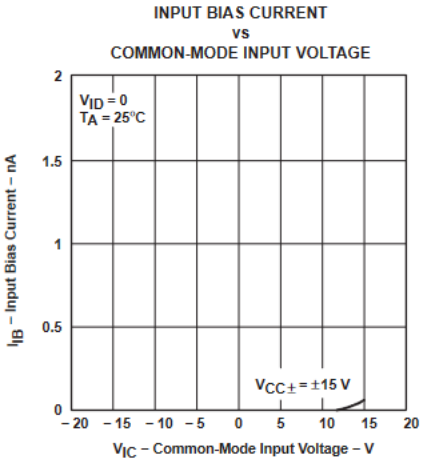

Figure 5-4.

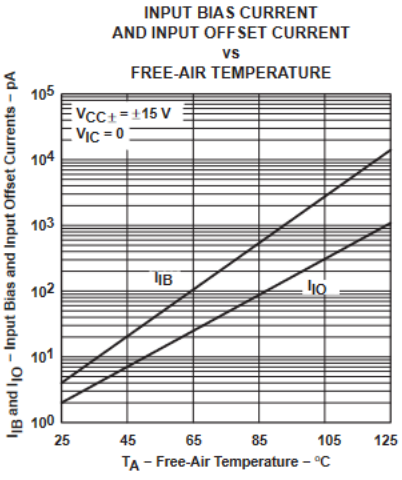

Figure 5-5.

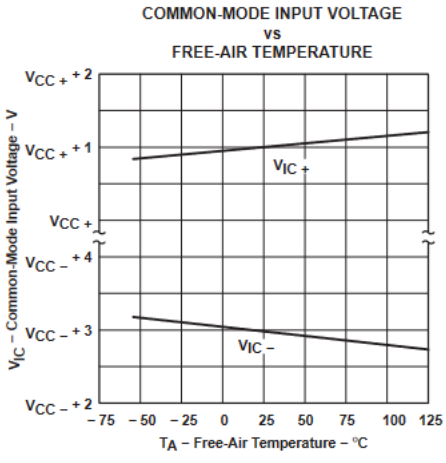

Figure 5-6.

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5.46 Typical Characteristics (continued)

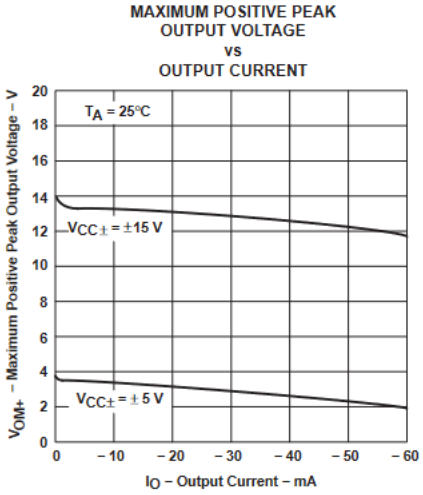

Figure 5-7.

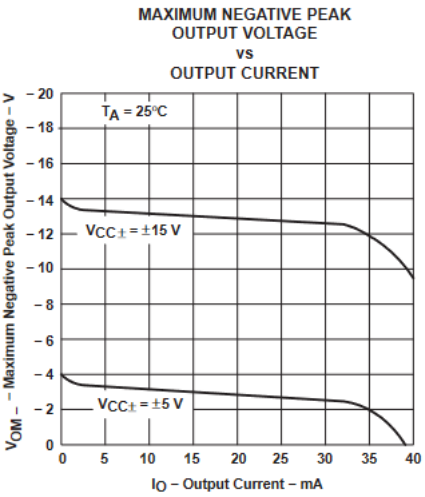

Figure 5-8.

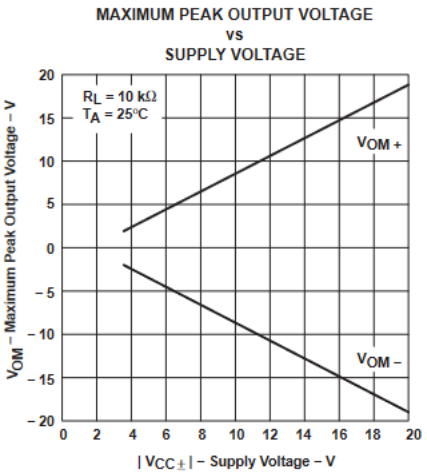

Figure 5-9.

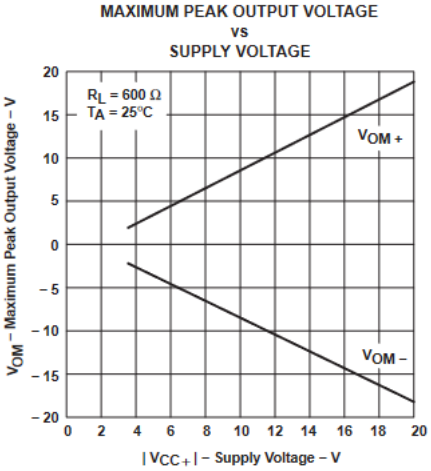

Figure 5-10.

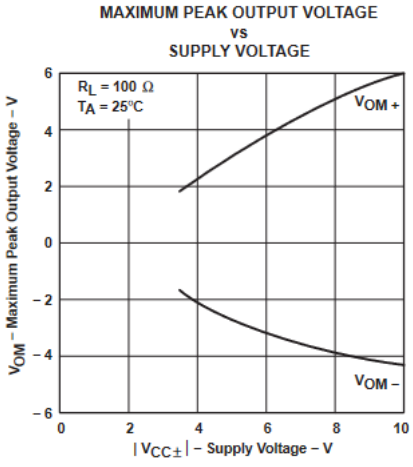

Figure 5-11.

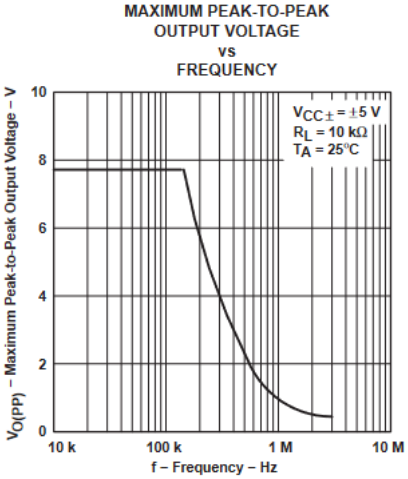

Figure 5-12.

5.46 Typical Characteristics (continued)

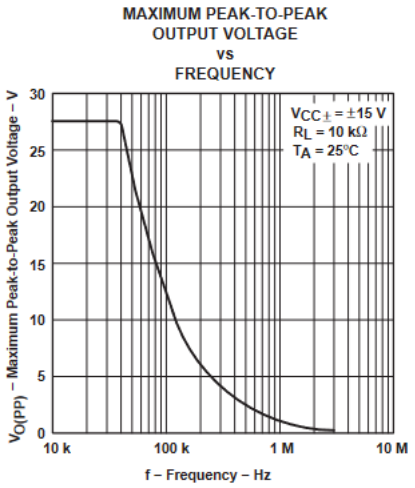

Figure 5-13.

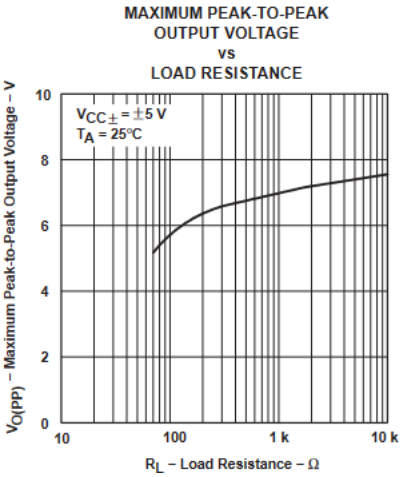

Figure 5-14.

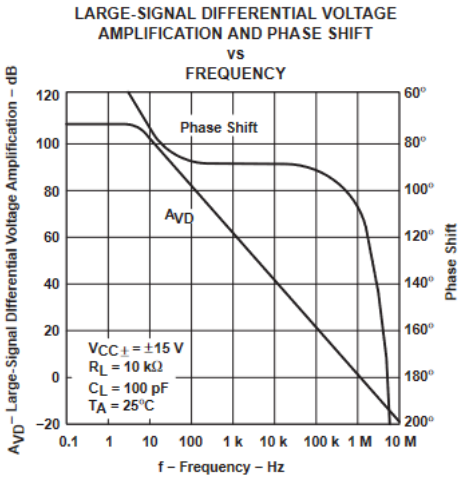

Figure 5-15.

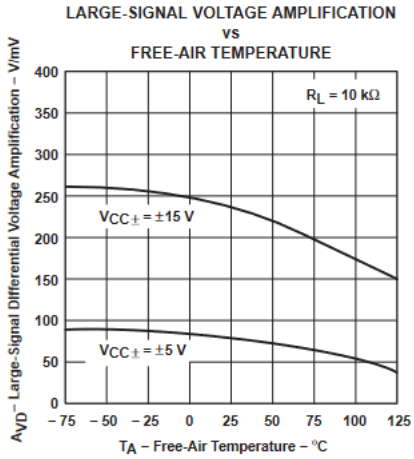

Figure 5-16.

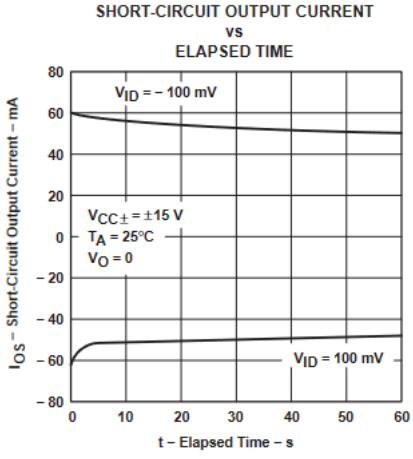

Figure 5-17.

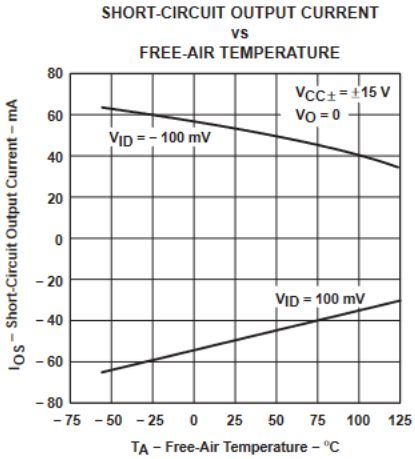

Figure 5-18.

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5.46 Typical Characteristics (continued)

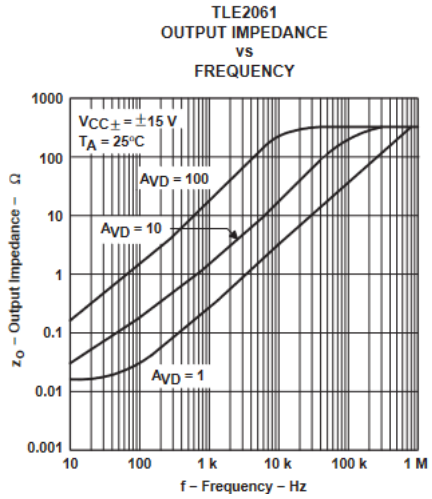


Figure 5-19.

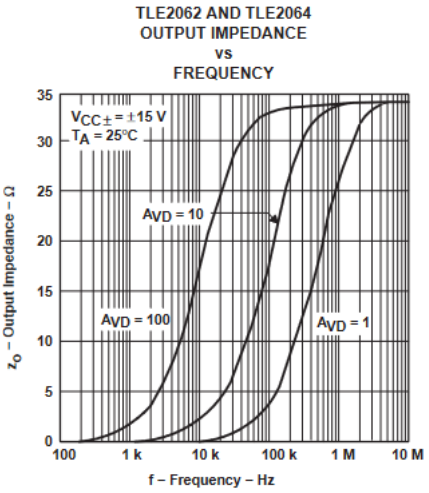


Figure 5-20.

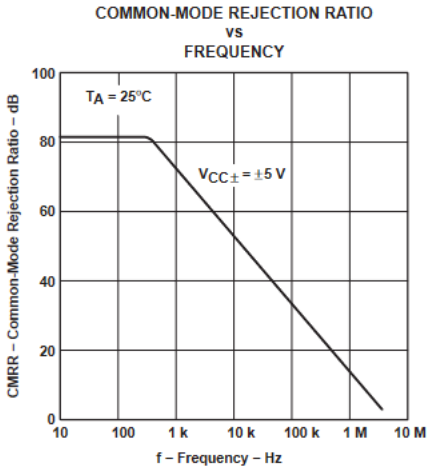


Figure 5-21.

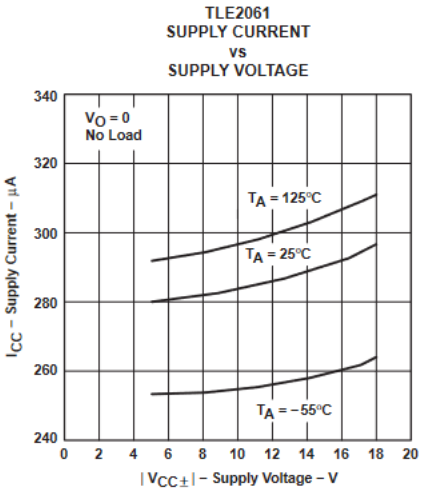
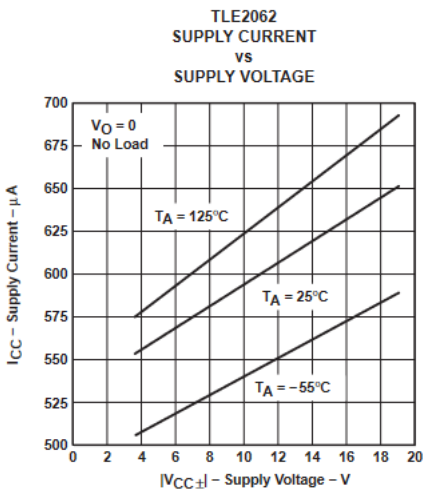


Figure 5-22.



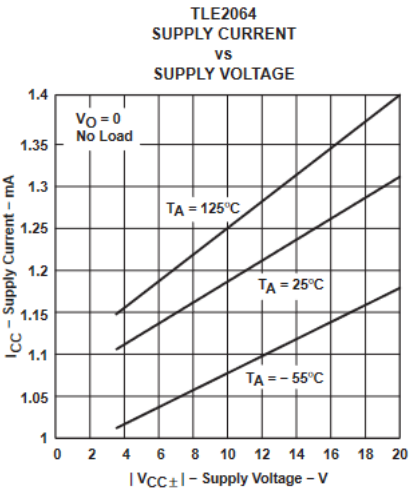


Figure 5-23.

5.46 Typical Characteristics (continued)

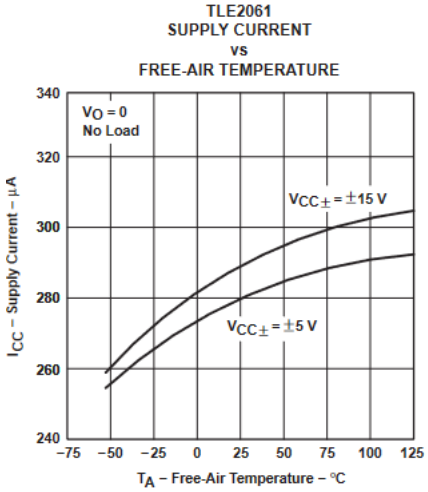


Figure 5-24.

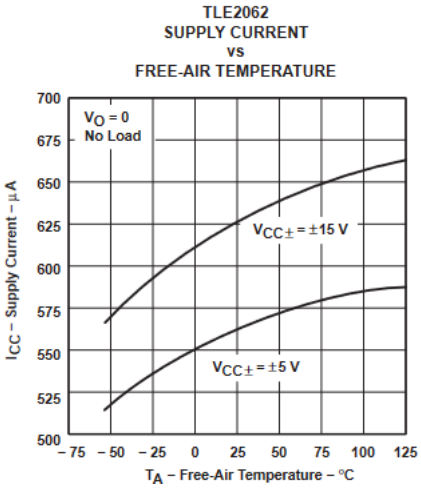


Figure 5-25.

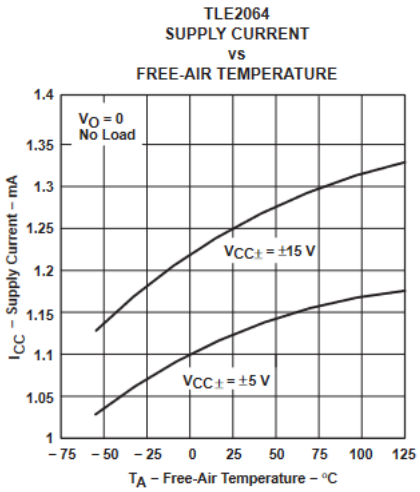


Figure 5-26.

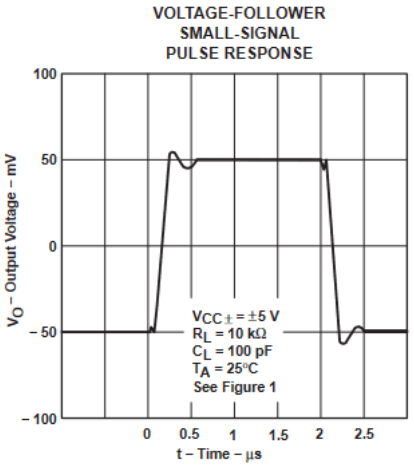


Figure 5-27.

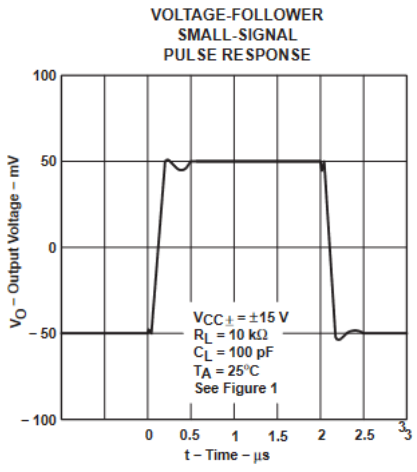


Figure 5-28.

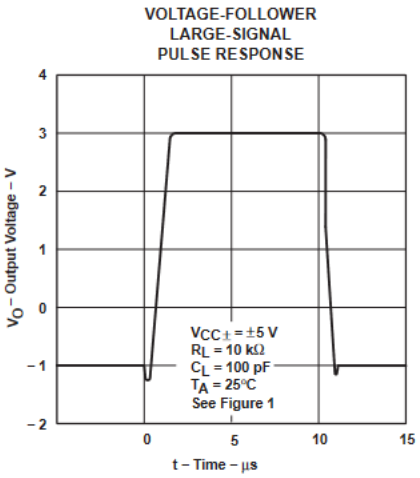


Figure 5-29.

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5.46 Typical Characteristics (continued)

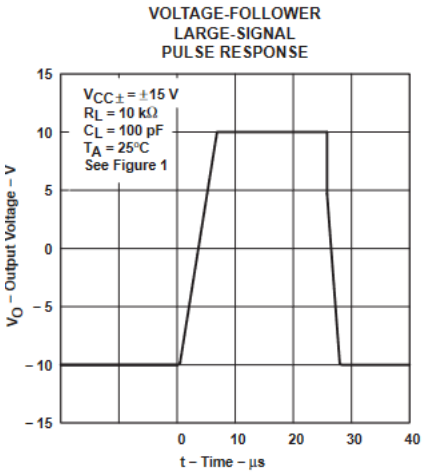

Figure 5-30.

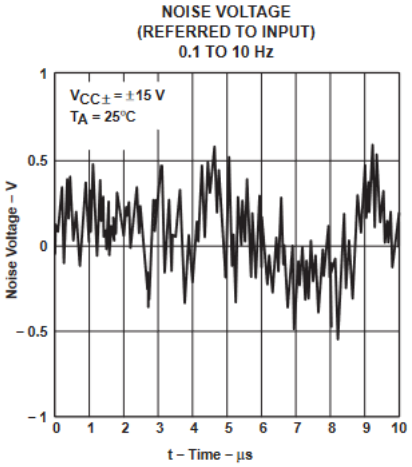

Figure 5-31.

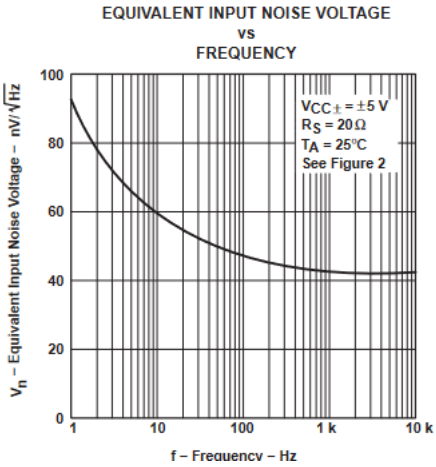

Figure 5-32.

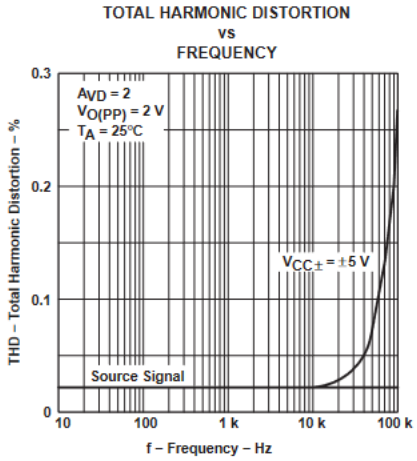

Figure 5-33.

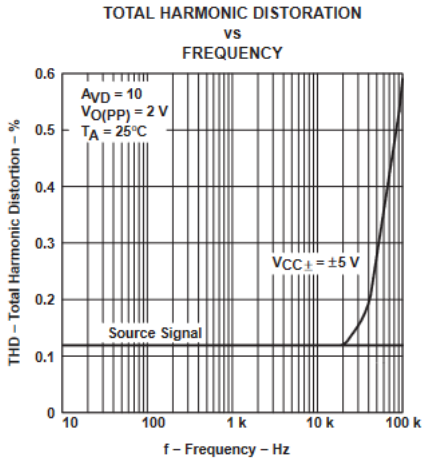

Figure 5-34.

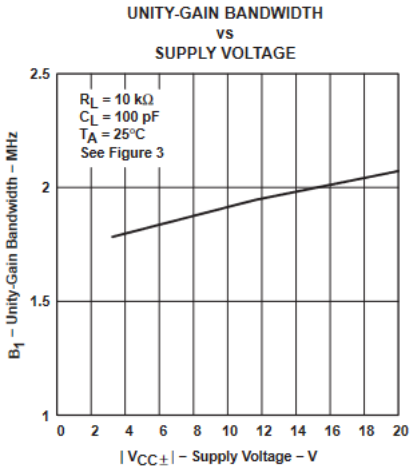

Figure 5-35.

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5.46 Typical Characteristics (continued)

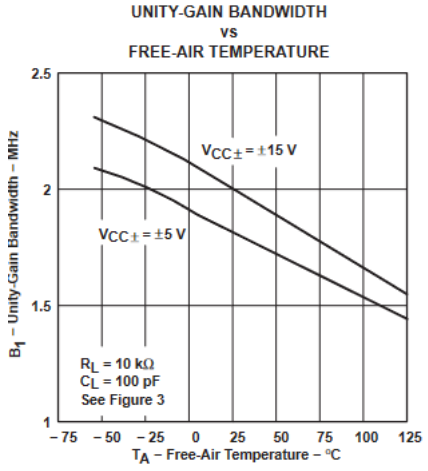

Figure 5-36.

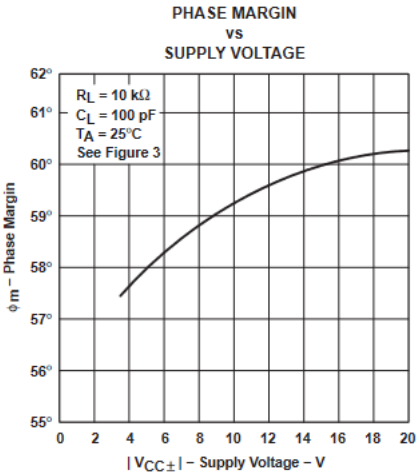

Figure 5-37.

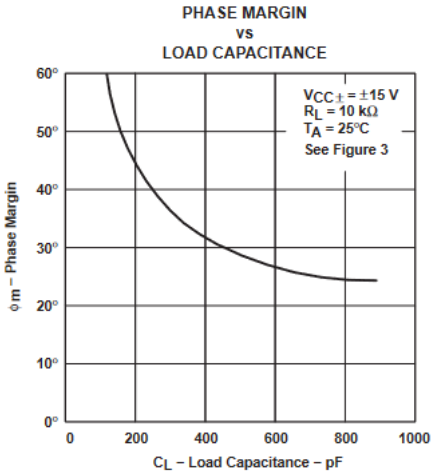

Figure 5-38.

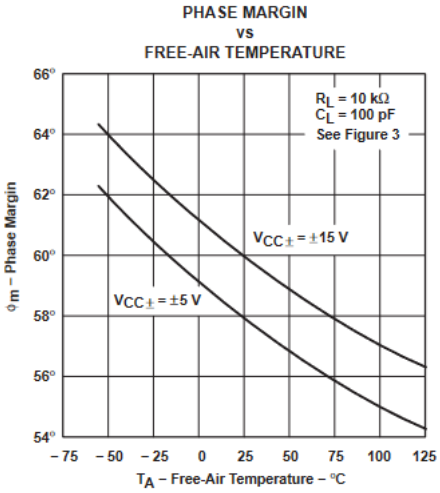

Figure 5-39.

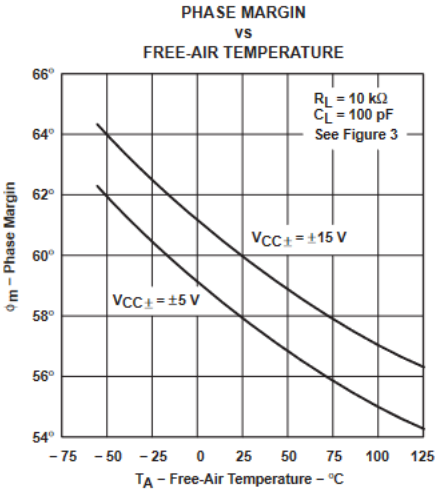

Figure 5-40.

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6 Parameter Measurement Information

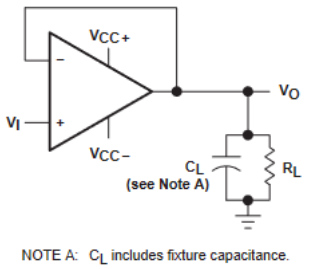

Figure 6-1. Slew-Rate Test Circuit

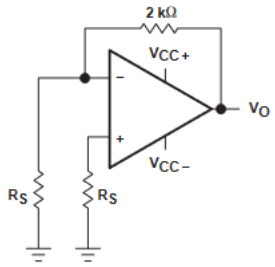

Figure 6-2. Noise-Voltage Test Circuit

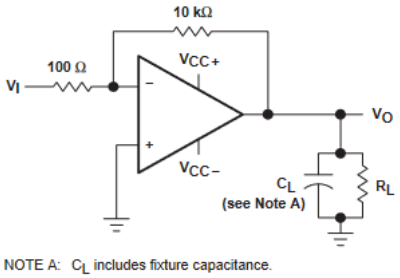

Figure 6-3. Unity-Gain Bandwidth and Phase-Margin Test Circuit

6.1 Typical Values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

6.2 Input Bias and Offset Current

At the picoampere bias current level typical of the TLE206x, TLE2064xA, and TLE206xB, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted into the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Input Characteristics

The TLE206x, TLE206xA, and TLE206xB are specified with a minimum and a maximum input voltage that, if exceeded at either input, can cause the device to malfunction. Due to the extremely high input impedance and resulting low bias current requirements, the TLE206x, TLE206xA, and TLE206xB are designed for low-level signal processing. However, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is good practice to include guard rings around inputs (see Figure 7-1). Drive these guards from a low-impedance source at the same voltage level as the common-mode input

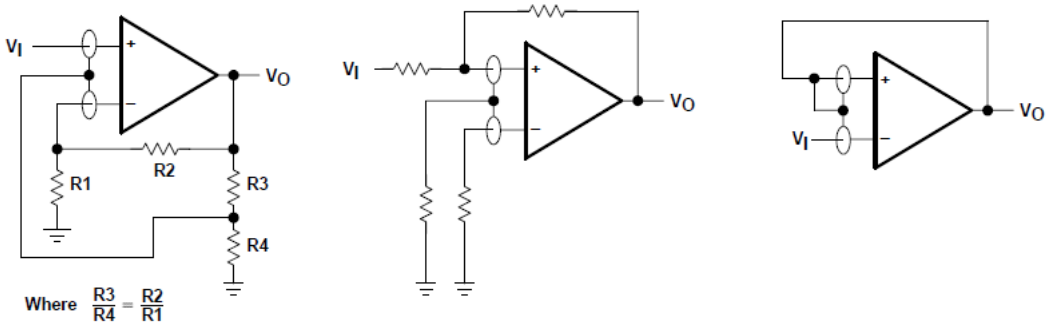

Figure 7-1. Use of Guard Rings

7.1.2 TLE2061 Input Offset Voltage Nulling

The TLE2061 series offers external null pins that can be used to further reduce the input offset voltage. The circuit can be connected if the feature is desired (see Figure 7-2). When external nulling is not needed, the null pins may be left unconnected.

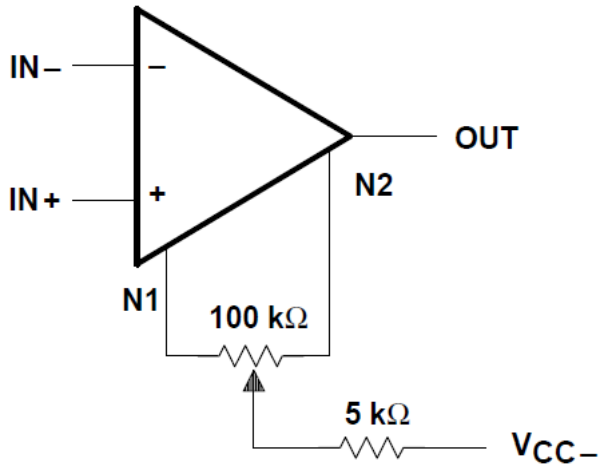

Figure 7-2. Input Offset Voltage Nulling

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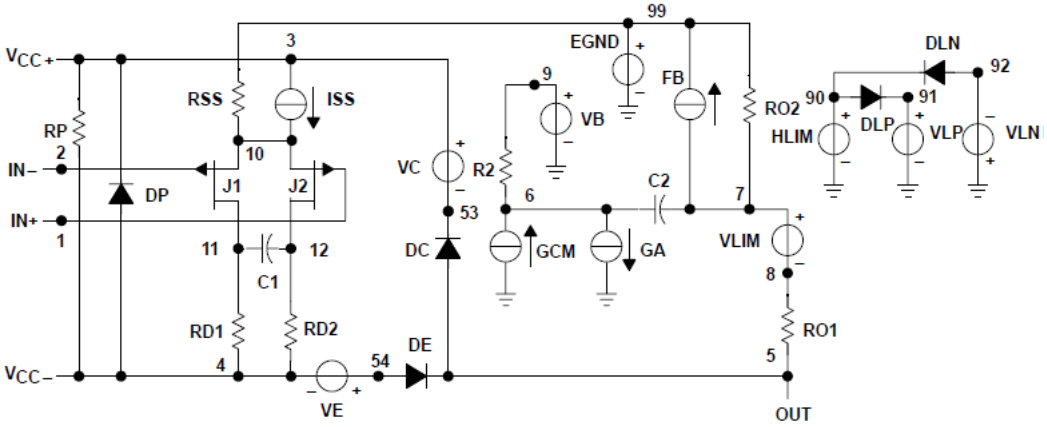
7.1.3 Macromodel Information

Macromodel information provided was derived using *PSpice*ä *Parts*ä model generation software. The Boyle macromodel and subcircuit in Figure 7-3 were generated using the TLE206x typical electrical and operating characteristics at T_A = 25°C. With this information, users can generate output simulations of the following key parameters to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit




```
.SUBCKT TLE208x 1 2 3 4 5
  C1   11  12   2.2E–12
  C2   6   7    10.00E–12
  DC   5   53   DX
  DE   54  5    DX
  DLP  90  91   DX
  DLN  92  90   DX
  DP   4   3    DX
  EGND 99  0 POLY (2) (3,0) (4,0) 0 .5 .5
  FB   7   99   POLY (5) VB VC VE VLP VLN 0
+ .... 5.607E6 –6E6 6E6 6E6 –6E6
  GA   6   0    11 12 333.0E–6
  GCM  0   6    10 99 7.43E–9
  ISS  3   10   DC 400.0E–6
  HLIM 90  0    VLIM 1K
  J1   11  2    10 JX
  J2   12  1    10 JX
  R2   6   9    100.0E3
  RD1  4   11   3.003E3
  RD2  4   12   3.003E3
  R01  8   5    80
  R02  7   99   80
  RP   3   4    27.30E3
  RSS  10  99   500.0E3
  VB   9   0    DC 0
  VC   3   53   DC 2.20
  VE   54  4    DC 2.20
  VLIM 7   8    DC 0
  VLP  91  0    DC 45
  VLN  0   92   DC 45
.MODEL DX D (IS=800.0E–18)
.MODEL JX PJF (IS=15.00E–12 BETA=554.5E–6
+ VTO=–.6)
.ENDS
```

1. G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Integrated Circuit Operational Amplifiers”, IEEE Journal of Solid-State Circuits, SC-9, 353 (1974).

Figure 7-3. Boyle Macromodel and Subcircuit

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2004) to Revision C (July 2025)	Page
• Updated the numbering, formatting, tables, figures and cross-references throughout the document to reflect modern datasheet standards	1
• Added *Applications* section	1
• Updated typical offset to 0.1mV all test conditions and supply voltages	8
• Updated typical offset drift to 1µV/°C across all test conditions and supply voltages	8
• Updated typical open-loop gain to 225V/mV across all test conditions and supply voltages	8
• Updated typical quiescent current across all test conditions and supply voltages	8
• Updated typical output swing across all test conditions and supply voltages	8
• Updated typical slew rate to 4V/µs across all test conditions and supply voltages	8

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9080701M2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9080701M2A TLE2061MFKB
5962-9080701MPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9080701MPA TLE2061M
5962-9080702Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9080702Q2A TLE2061 AMFKB
5962-9080702QPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9080702QPA TLE2061AM
5962-9080703QPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9080703QPA TLE2061BM
5962-9080801MPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9080801MPA TLE2062M
5962-9080803QPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9080803QPA TLE2062BM
5962-9080901M2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9080901M2A TLE2064 MFKB
5962-9080901MCA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9080901MCA TLE2064MJB
5962-9080902M2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9080902M2A TLE2064A MFKB
5962-9080902MDA	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9080902MDA TLE2064AMWB
5962-9080903Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9080903Q2A TLE2064 BMFKB

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9080903QCA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9080903QCA TLE2064BMJB
TLE2061ACD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	2061AC
TLE2061ACP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLE2061AC
TLE2061ACP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLE2061AC
TLE2061ACPE4	Active	Production	PDIP (P) | 8	50 | TUBE	-	Call TI	Call TI	0 to 70	
TLE2061AID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	2061AI
TLE2061AIP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLE2061AI
TLE2061AIP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLE2061AI
TLE2061AMFKB	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9080702Q2A TLE2061AMFKB
TLE2061AMFKB.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9080702Q2A TLE2061AMFKB
TLE2061AMJGB	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9080702QPA TLE2061AM
TLE2061AMJGB.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9080702QPA TLE2061AM
TLE2061BMJGB	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9080703QPA TLE2061BM
TLE2061BMJGB.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9080703QPA TLE2061BM
TLE2061CD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	2061C
TLE2061CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2061C
TLE2061CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2061C
TLE2061CDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	0 to 70	
TLE2061CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLE2061CP
TLE2061CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLE2061CP
TLE2061ID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	2061I
TLE2061IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2061I

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLE2061IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2061I
TLE2061IP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLE2061IP
TLE2061IP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLE2061IP
TLE2061MD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-55 to 125	2061M
TLE2061MDG4	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-55 to 125	2061M
TLE2061MFKB	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9080701M2A TLE2061MFKB
TLE2061MFKB.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9080701M2A TLE2061MFKB
TLE2061MJGB	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9080701MPA TLE2061M
TLE2061MJGB.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9080701MPA TLE2061M
TLE2062ACD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	2062AC
TLE2062ACDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2062AC
TLE2062ACDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2062AC
TLE2062ACDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2062AC
TLE2062ACDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2062AC
TLE2062AID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	2062AI
TLE2062AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2062AI
TLE2062AIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2062AI
TLE2062AMD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-55 to 125	2062AM
TLE2062AMDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2062AM
TLE2062AMDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2062AM
TLE2062AMJG	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TLE2062 AMJG
TLE2062AMJG.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TLE2062 AMJG
TLE2062BMJG	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TLE2062 BMJG

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLE2062BMJG.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TLE2062 BMJG
TLE2062BMJGB	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9080803QPA TLE2062BM
TLE2062BMJGB.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9080803QPA TLE2062BM
TLE2062CD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	2062C
TLE2062CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2062C
TLE2062CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2062C
TLE2062CDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	0 to 70	
TLE2062CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLE2062CP
TLE2062CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLE2062CP
TLE2062ID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	2062I
TLE2062IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2062I
TLE2062IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2062I
TLE2062IDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2062I
TLE2062IDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2062I
TLE2062IP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLE2062IP
TLE2062IP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLE2062IP
TLE2062MFKB	Obsolete	Production	LCCC (FK) | 20	-	-	Call TI	Call TI	-	5962-9080801M2A TLE2062MFKB
TLE2062MJG	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TLE2062MJG
TLE2062MJG.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TLE2062MJG
TLE2062MJGB	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9080801MPA TLE2062M
TLE2062MJGB.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9080801MPA TLE2062M
TLE2064ACD	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	2064AC
TLE2064ACDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	2064AC
TLE2064ACDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2064AC
TLE2064ACN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-	TLE2064ACN

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLE2064ACN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLE2064ACN
TLE2064AID	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	2064AI
TLE2064AIDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	2064AI
TLE2064AIDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2064AI
TLE2064AIDRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2064AI
TLE2064AIDRG4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2064AI
TLE2064AMD	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	2064AM
TLE2064AMDG4	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-	2064AM
TLE2064AMDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2064AM
TLE2064AMDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2064AM
TLE2064AMDRG4	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-	2064AM
TLE2064AMFKB	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9080902M2A TLE2064A MFKB
TLE2064AMFKB.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9080902M2A TLE2064A MFKB
TLE2064AMJ	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TLE2064AMJ
TLE2064AMJ.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TLE2064AMJ
TLE2064AMWB	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9080902MDA TLE2064AMWB
TLE2064AMWB.A	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9080902MDA TLE2064AMWB
TLE2064BMFKB	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9080903Q2A TLE2064 BMFKB
TLE2064BMFKB.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9080903Q2A TLE2064 BMFKB

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLE2064BMJ	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TLE2064BMJ
TLE2064BMJ.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TLE2064BMJ
TLE2064BMJB	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9080903QC A TLE2064BMJB
TLE2064BMJB.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9080903QC A TLE2064BMJB
TLE2064CD	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	TLE2064C
TLE2064CDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLE2064C
TLE2064CDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLE2064C
TLE2064CDRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	-	Call TI	Call TI	0 to 70	
TLE2064CN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLE2064CN
TLE2064CN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLE2064CN
TLE2064CNE4	Active	Production	PDIP (N) | 14	25 | TUBE	-	Call TI	Call TI	0 to 70	
TLE2064ID	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	TLE2064I
TLE2064IDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLE2064I
TLE2064IDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLE2064I
TLE2064IN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLE2064IN
TLE2064IN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLE2064IN
TLE2064INE4	Active	Production	PDIP (N) | 14	25 | TUBE	-	Call TI	Call TI	-40 to 85	
TLE2064MD	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	TLE2064M
TLE2064MDG4	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-	T2064M
TLE2064MDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLE2064M
TLE2064MDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLE2064M
TLE2064MFKB	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9080901M2A TLE2064 MFKB
TLE2064MFKB.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9080901M2A TLE2064 MFKB

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLE2064MJ	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TLE2064MJ
TLE2064MJ.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TLE2064MJ
TLE2064MJB	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9080901MC A TLE2064MJB
TLE2064MJB.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9080901MC A TLE2064MJB

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLE2061, TLE2061A, TLE2061AM, TLE2061M, TLE2062, TLE2062A, TLE2062AM, TLE2062M, TLE2064, TLE2064A, TLE2064AM, TLE2064M :

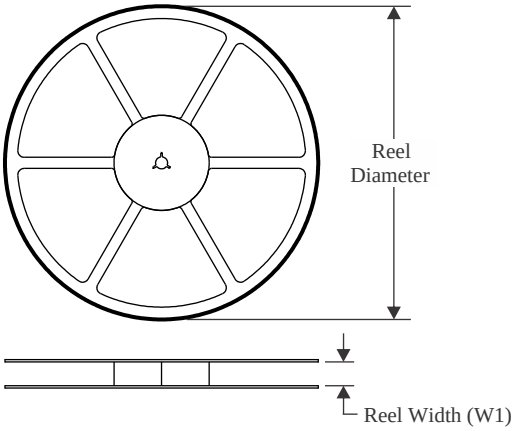
- Catalog : TLE2061A, TLE2061, TLE2062A, TLE2062, TLE2064A, TLE2064
- Military : TLE2061M, TLE2061AM, TLE2062M, TLE2062AM, TLE2064M, TLE2064AM

NOTE: Qualified Version Definitions:

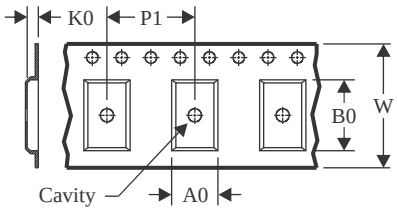
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

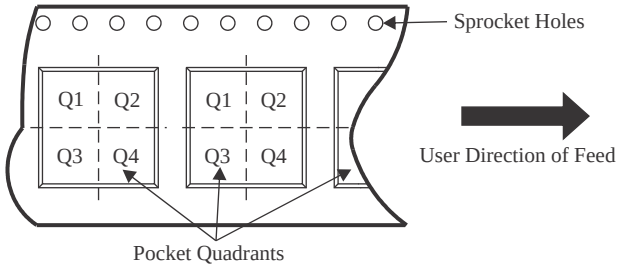


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

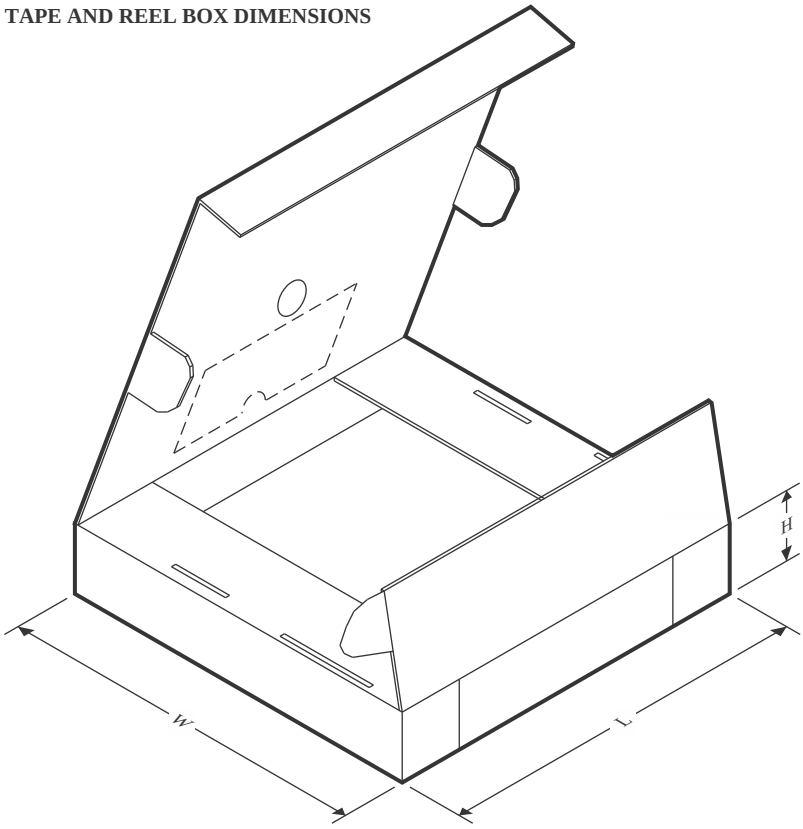
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLE2061CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2061IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2062ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2062ACDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2062AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2062AMDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2062CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2062IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2062IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2064ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLE2064AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLE2064AIDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLE2064AMDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLE2064CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLE2064IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLE2064MDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

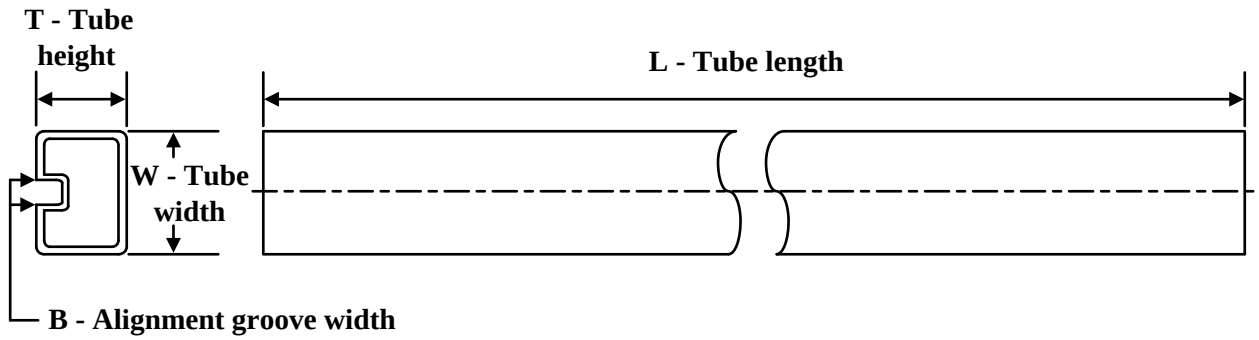
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLE2061CDR	SOIC	D	8	2500	353.0	353.0	32.0
TLE2061IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLE2062ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TLE2062ACDRG4	SOIC	D	8	2500	353.0	353.0	32.0
TLE2062AIDR	SOIC	D	8	2500	353.0	353.0	32.0
TLE2062AMDR	SOIC	D	8	2500	350.0	350.0	43.0
TLE2062CDR	SOIC	D	8	2500	353.0	353.0	32.0
TLE2062IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLE2062IDRG4	SOIC	D	8	2500	353.0	353.0	32.0
TLE2064ACDR	SOIC	D	14	2500	353.0	353.0	32.0
TLE2064AIDR	SOIC	D	14	2500	353.0	353.0	32.0
TLE2064AIDRG4	SOIC	D	14	2500	353.0	353.0	32.0
TLE2064AMDR	SOIC	D	14	2500	350.0	350.0	43.0
TLE2064CDR	SOIC	D	14	2500	353.0	353.0	32.0
TLE2064IDR	SOIC	D	14	2500	353.0	353.0	32.0
TLE2064MDR	SOIC	D	14	2500	350.0	350.0	43.0

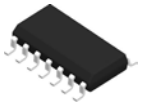
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9080701M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9080702Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9080901M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9080902M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9080902MDA	W	CFP	14	25	506.98	26.16	6220	NA
5962-9080903Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
TLE2061ACP	P	PDIP	8	50	506	13.97	11230	4.32
TLE2061ACP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLE2061AIP	P	PDIP	8	50	506	13.97	11230	4.32
TLE2061AIP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLE2061AMFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
TLE2061AMFKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA
TLE2061CP	P	PDIP	8	50	506	13.97	11230	4.32
TLE2061CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLE2061IP	P	PDIP	8	50	506	13.97	11230	4.32
TLE2061IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLE2061MFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
TLE2061MFKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA
TLE2062CP	P	PDIP	8	50	506	13.97	11230	4.32
TLE2062CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLE2062IP	P	PDIP	8	50	506	13.97	11230	4.32
TLE2062IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLE2064ACN	N	PDIP	14	25	506	13.97	11230	4.32
TLE2064ACN.A	N	PDIP	14	25	506	13.97	11230	4.32
TLE2064AMFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
TLE2064AMFKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA
TLE2064AMWB	W	CFP	14	25	506.98	26.16	6220	NA
TLE2064AMWB.A	W	CFP	14	25	506.98	26.16	6220	NA
TLE2064BMFKB	FK	LCCC	20	55	506.98	12.06	2030	NA

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLE2064BMFKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA
TLE2064CN	N	PDIP	14	25	506	13.97	11230	4.32
TLE2064CN.A	N	PDIP	14	25	506	13.97	11230	4.32
TLE2064IN	N	PDIP	14	25	506	13.97	11230	4.32
TLE2064IN.A	N	PDIP	14	25	506	13.97	11230	4.32
TLE2064MFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
TLE2064MFKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA

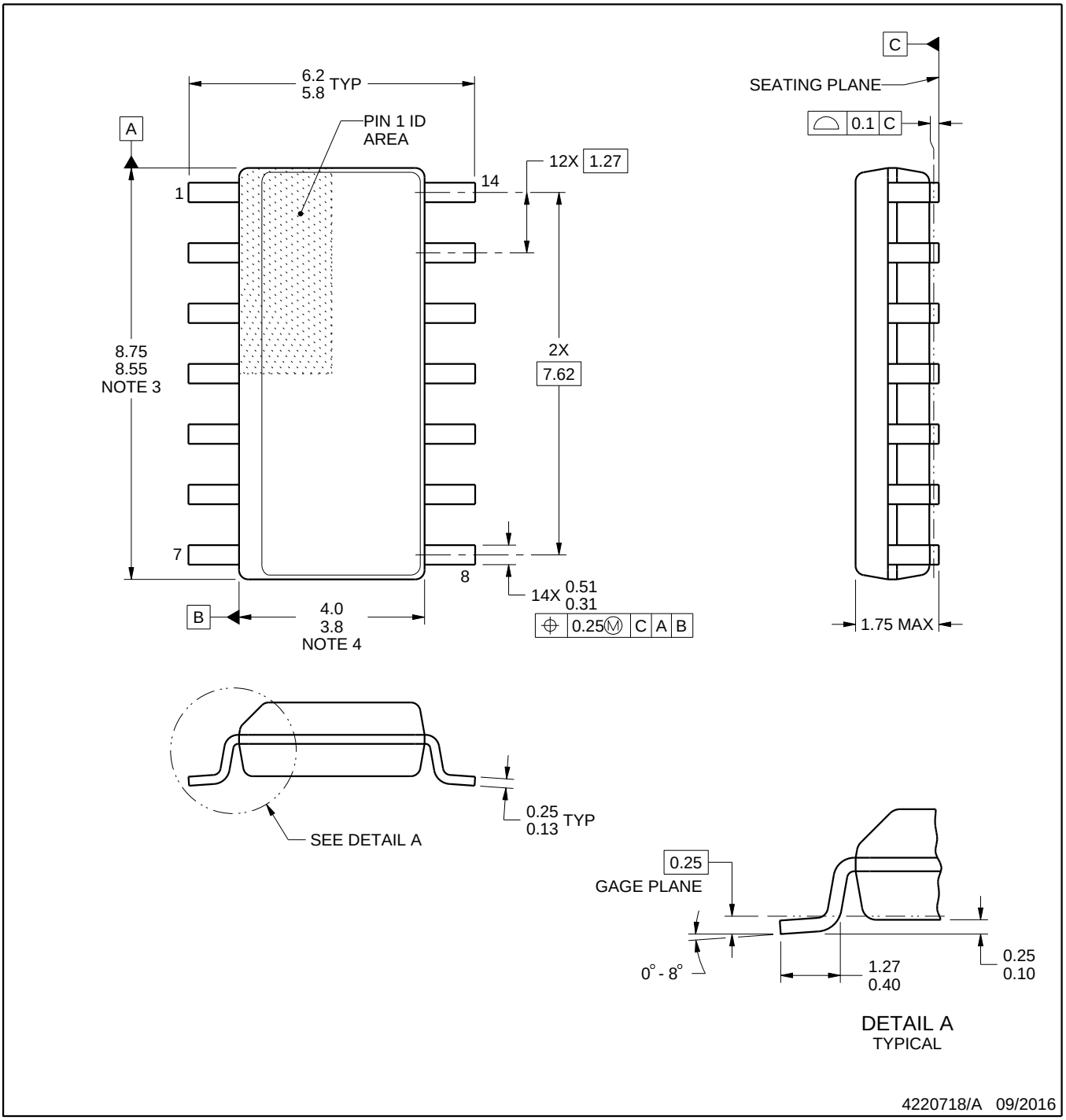


PACKAGE OUTLINE

D0014A

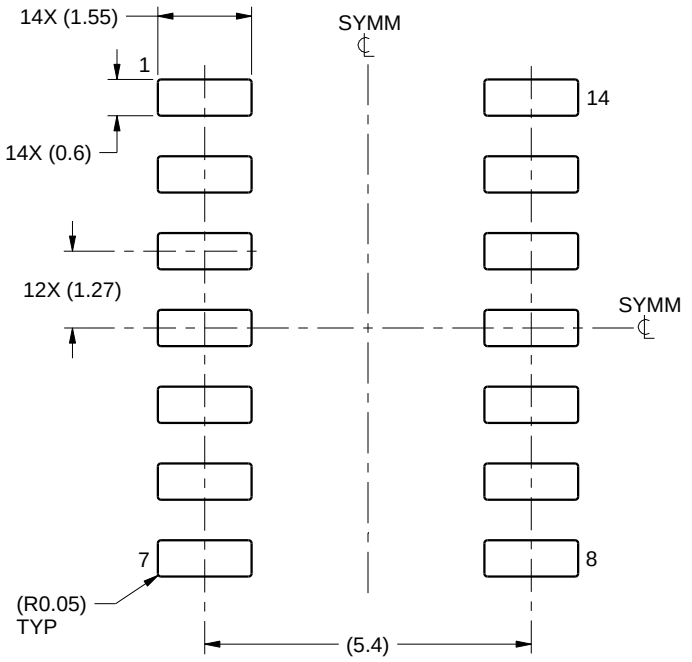
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

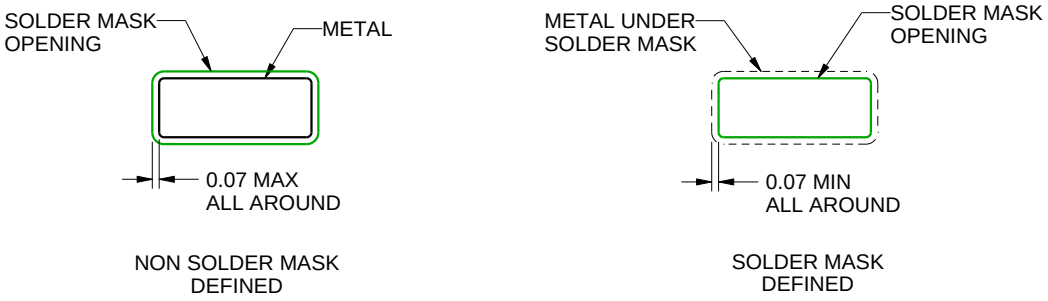


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

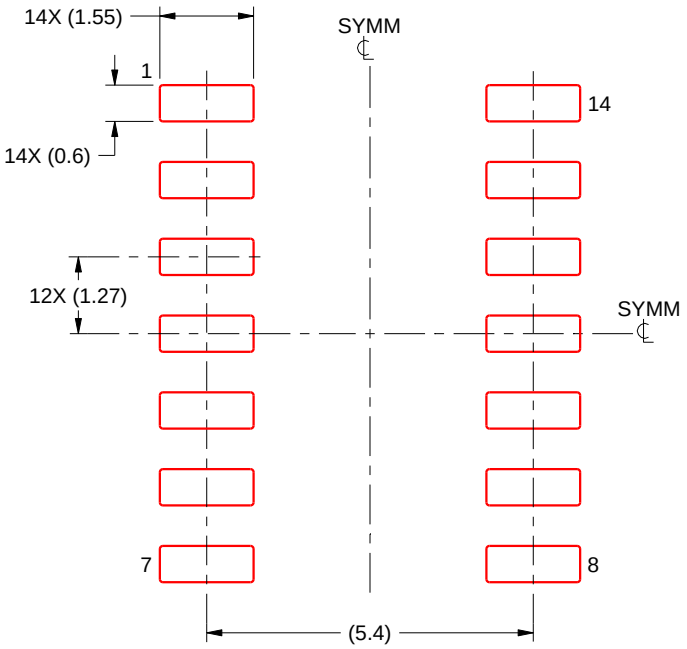
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



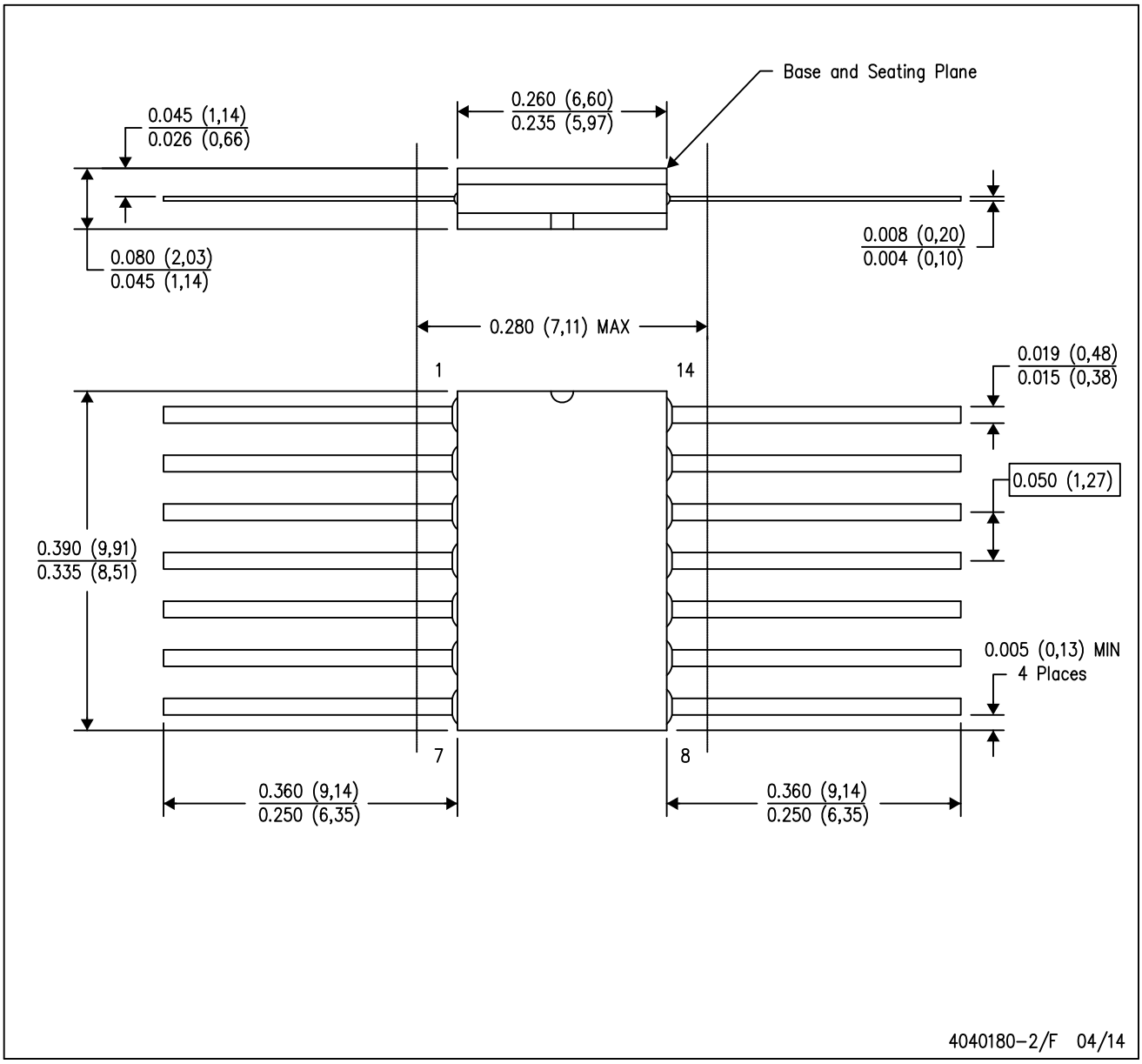
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

GENERIC PACKAGE VIEW

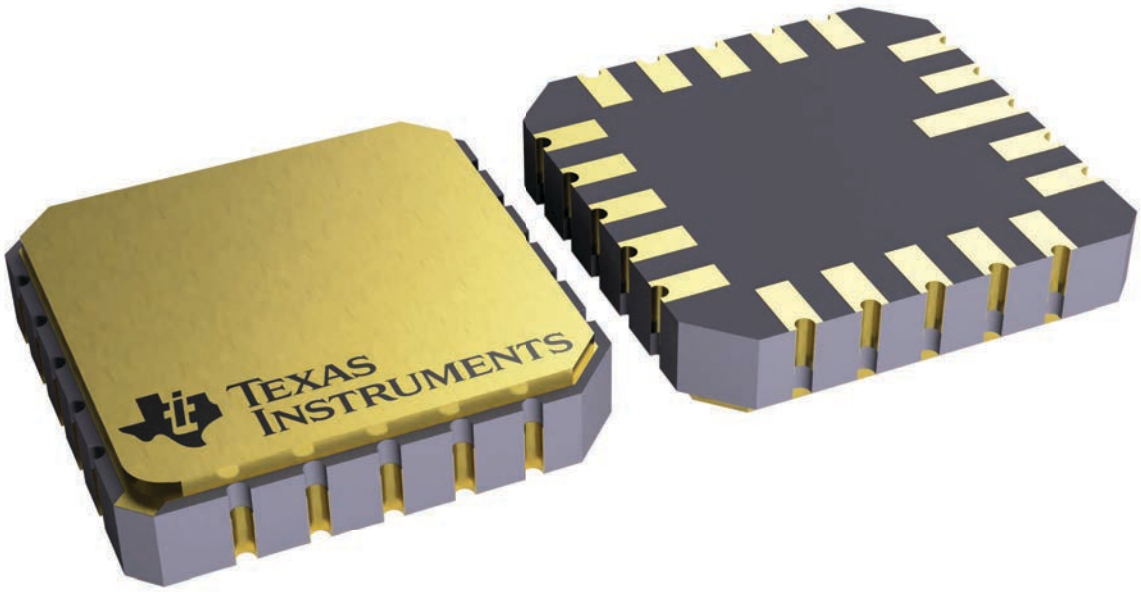
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

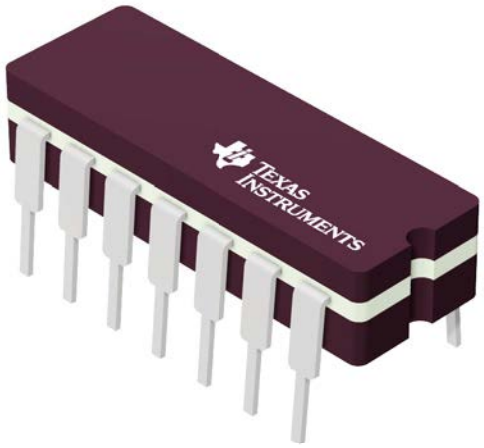


4229370VA\

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

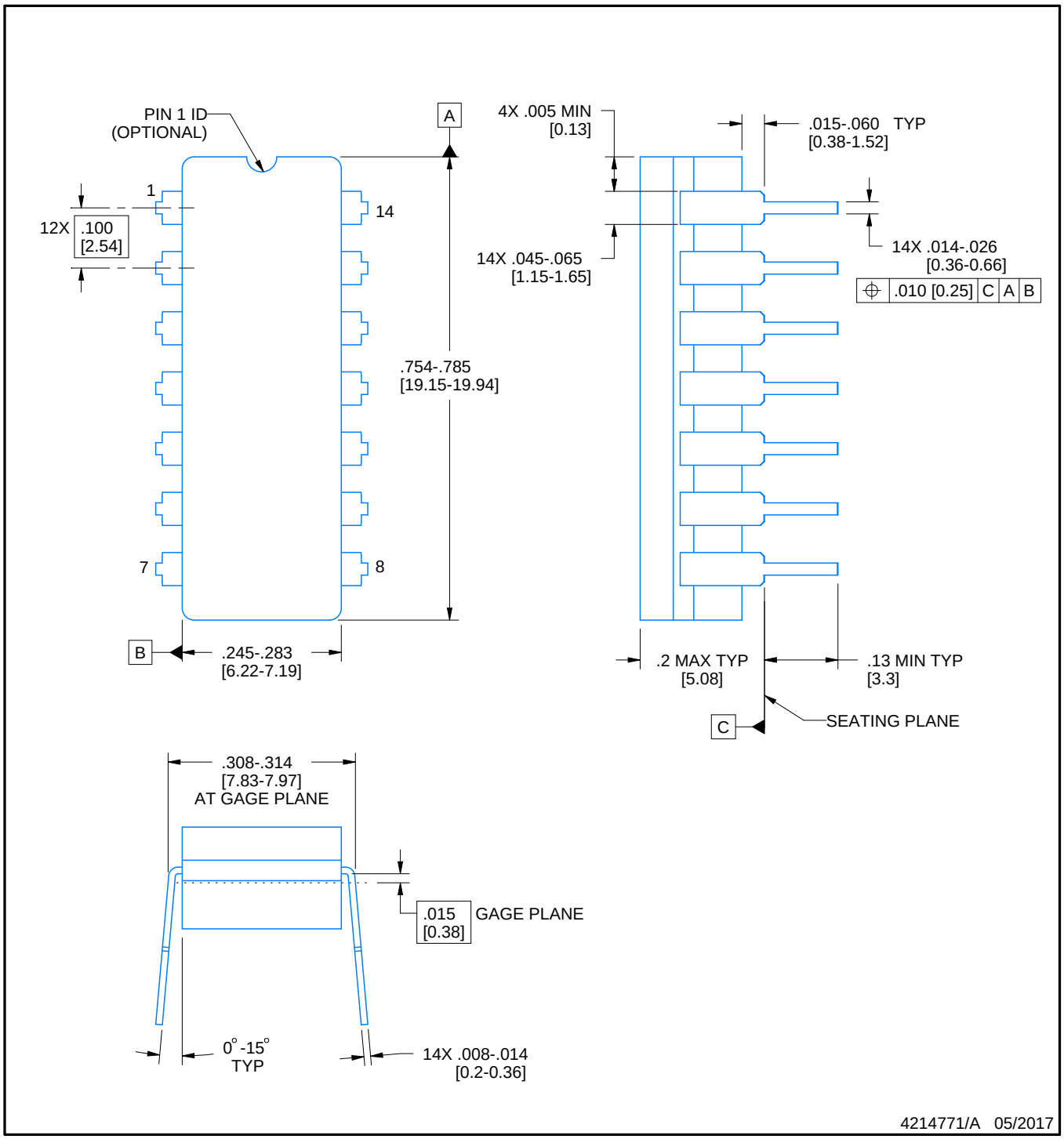
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

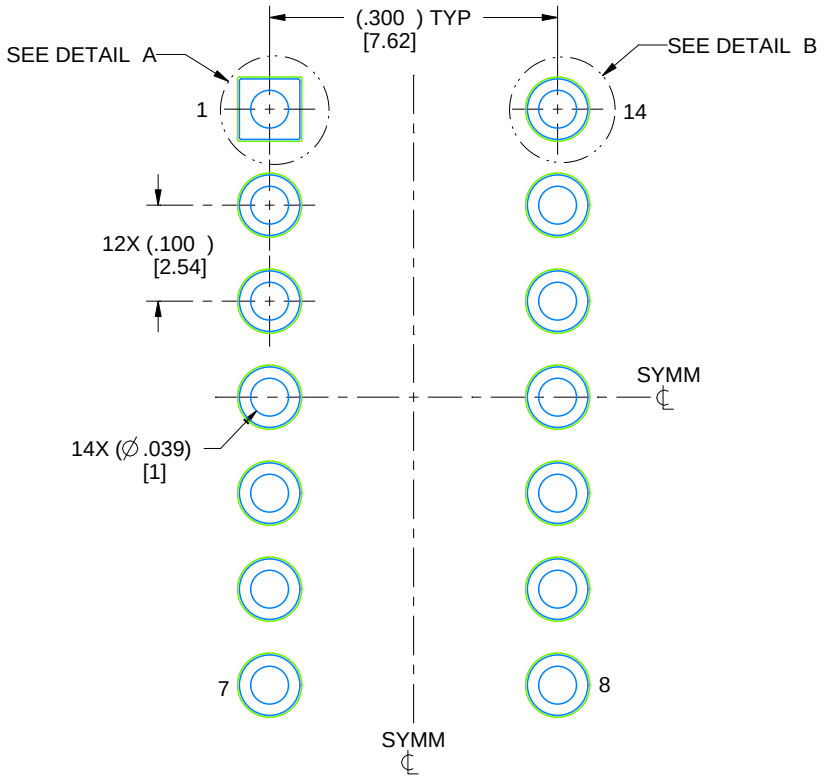
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

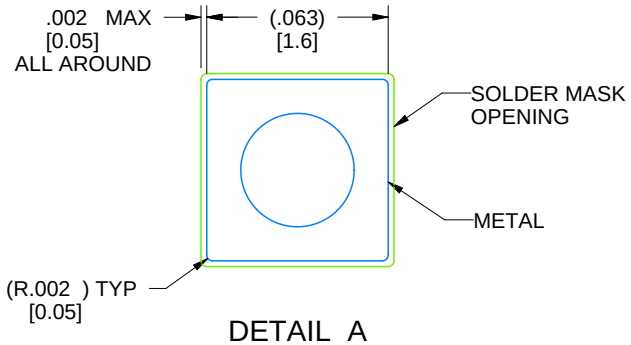
J0014A

CDIP - 5.08 mm max height

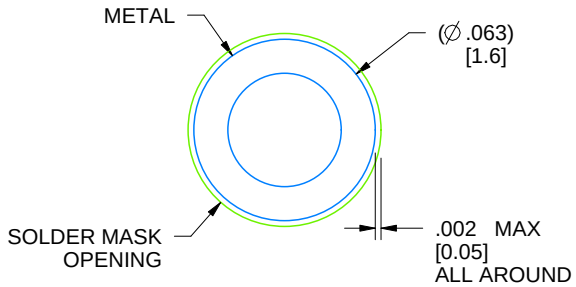
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

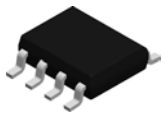


DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

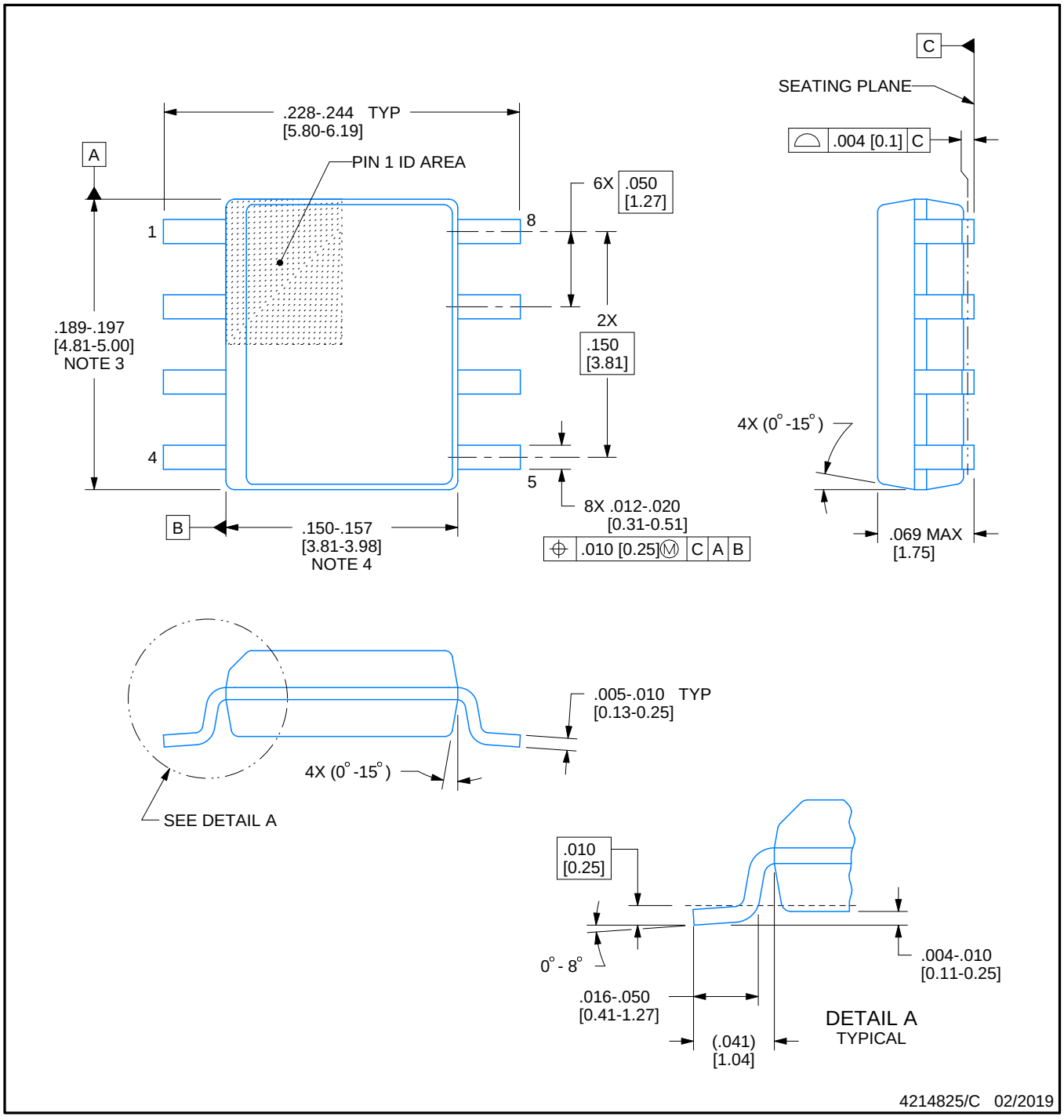


PACKAGE OUTLINE

D0008A

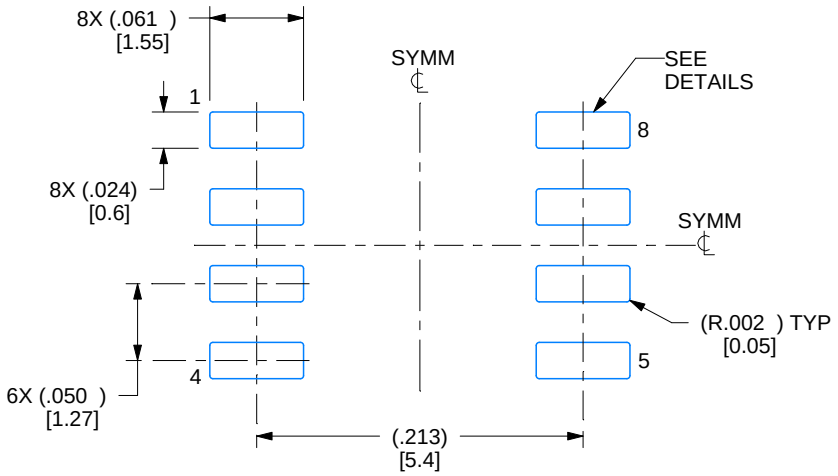
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

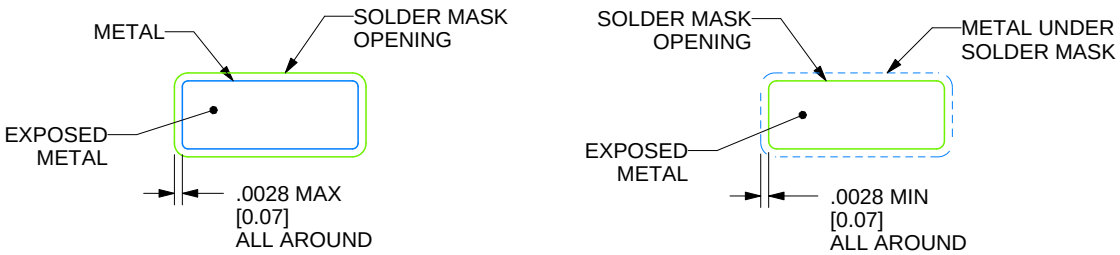


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

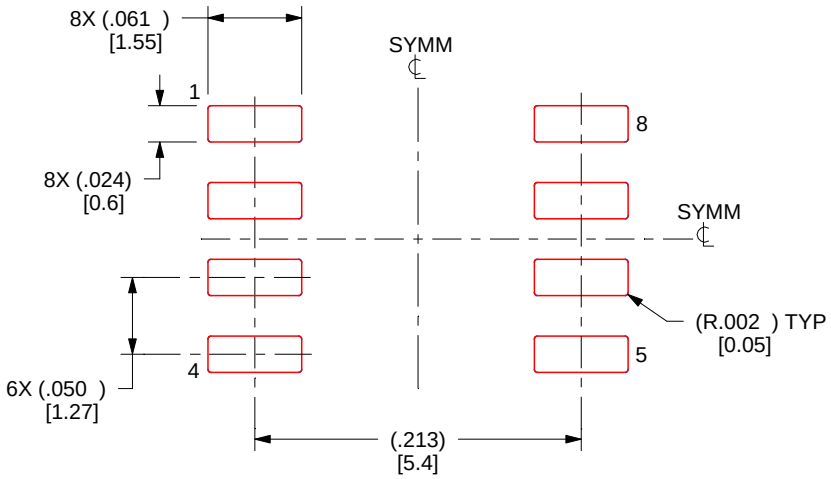
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



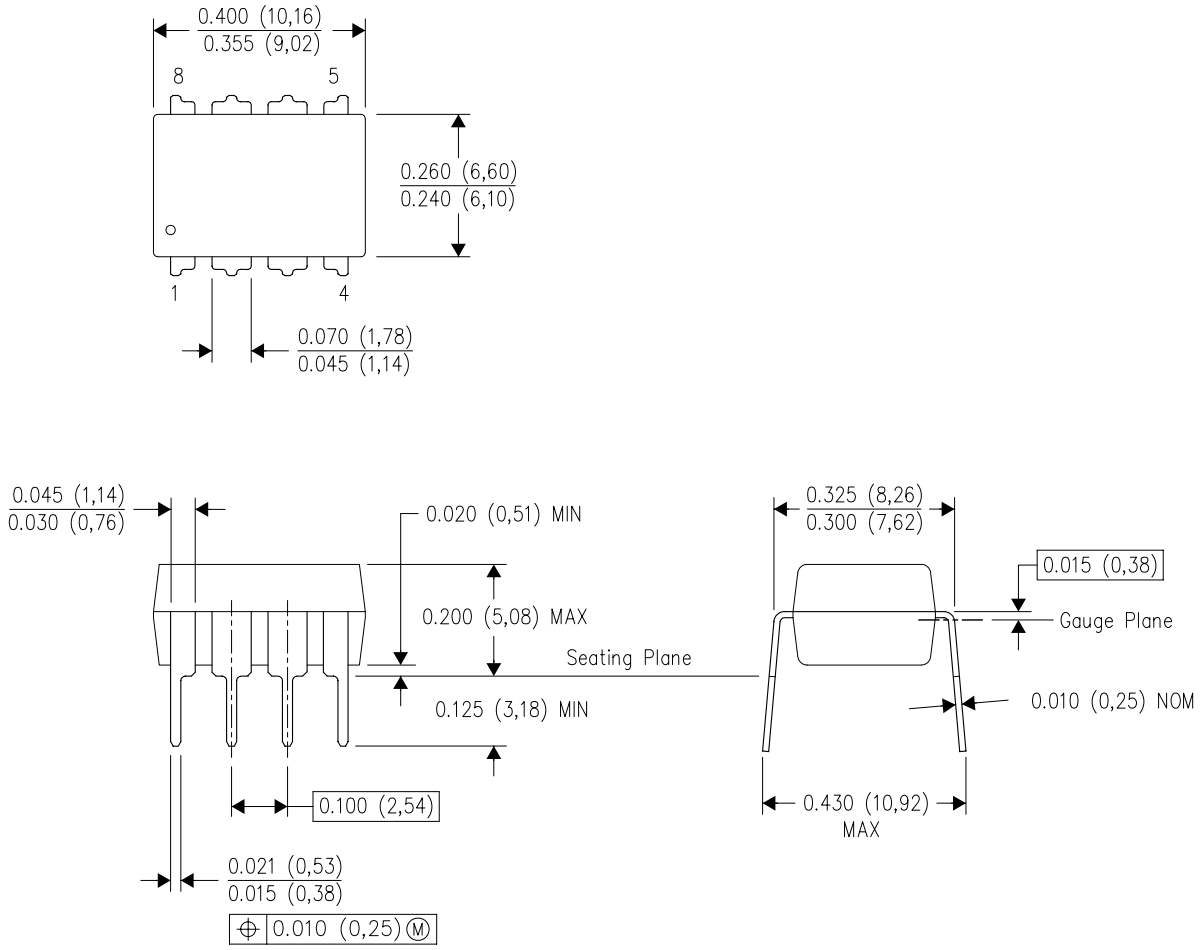
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

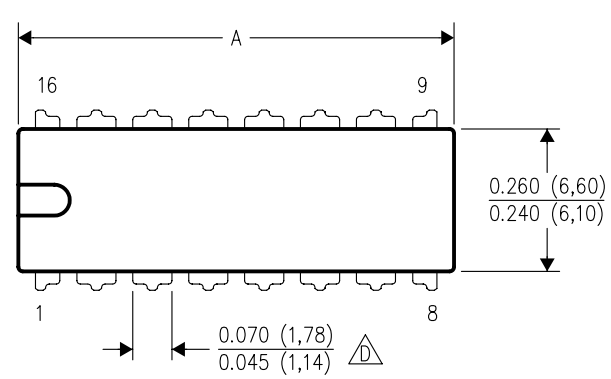


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

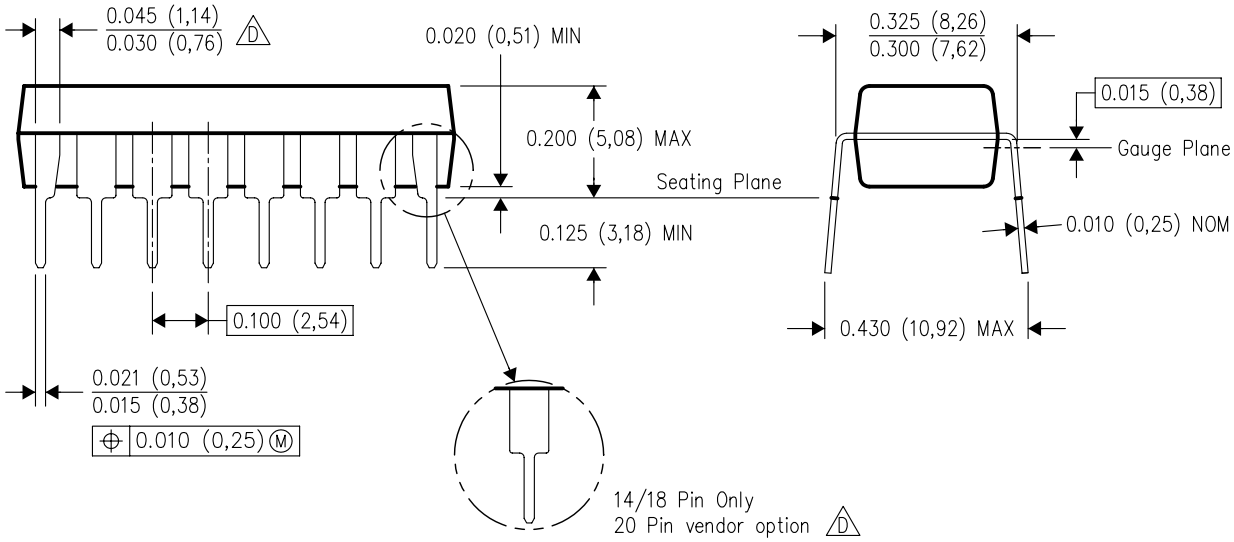
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

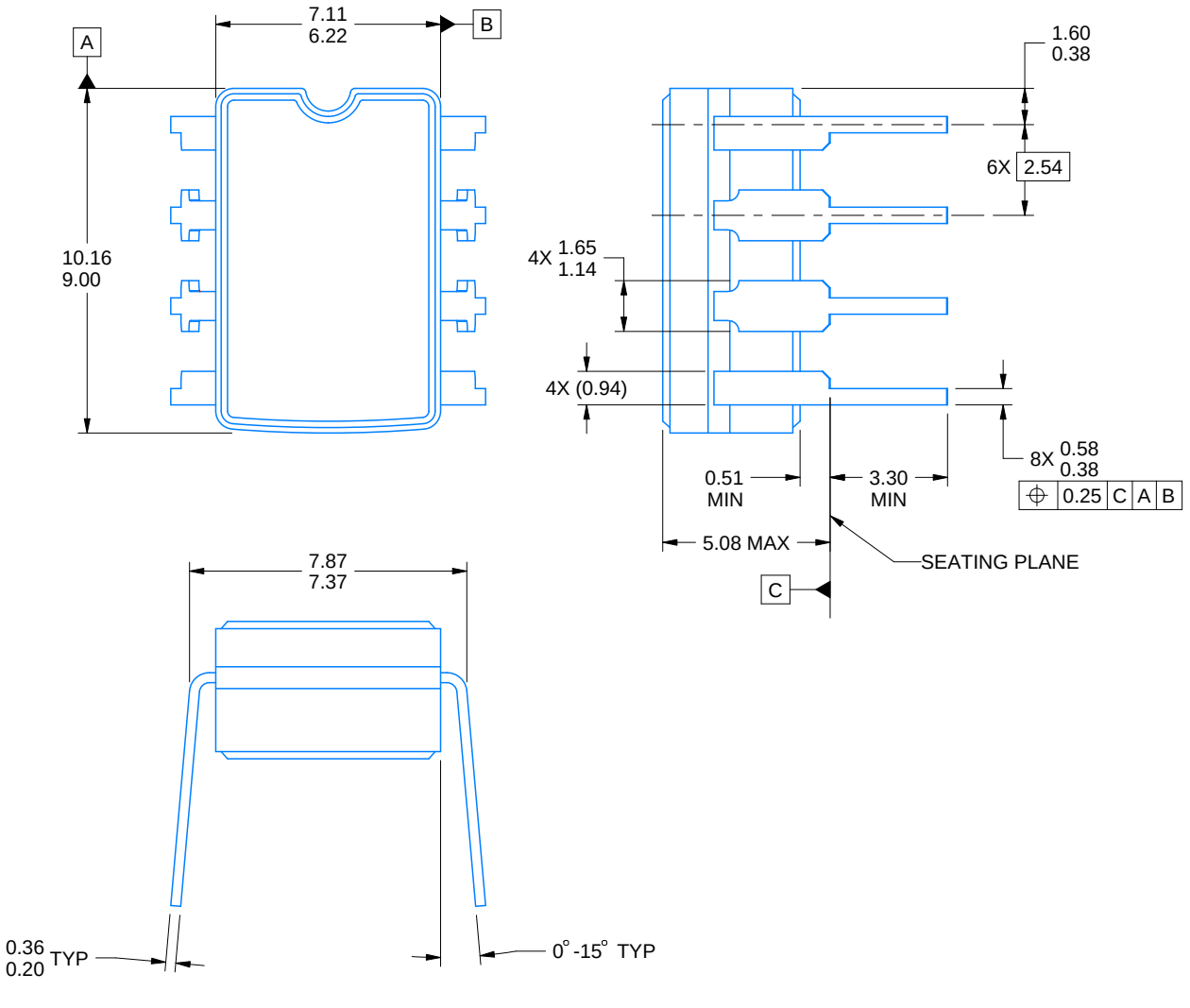
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



4230036/A 09/2023

NOTES:

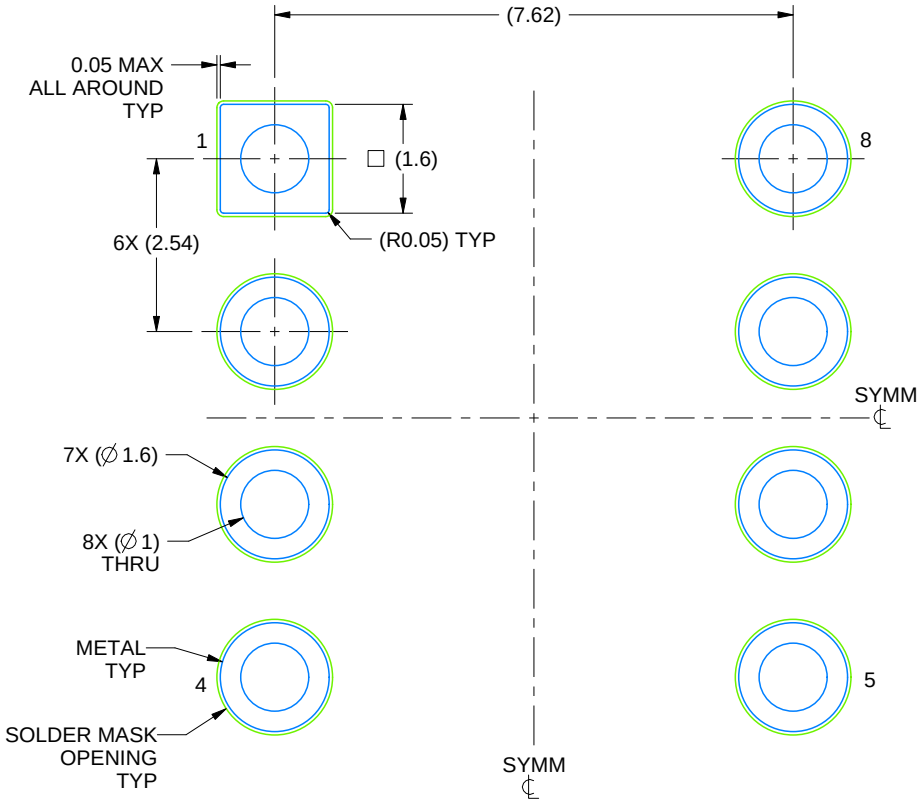
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

4230036/A 09/2023

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