TOSHIBA BIPOLAR DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TD62650FG,TD62651FG,TD62652FG

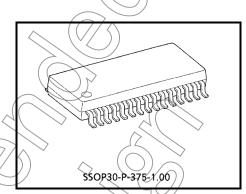
5V POWER SUPPLY & SUPPLY MONITORING + COMMUNICATIONS IC

The TD62650FG series covers products developed for use in microcomputer systems applicable to automatic vending machines. They produce an output voltage of 5 V \pm 0.5 V without need for adjustment, through their accurate reference voltage and amplifier circuit.

The 5V section can reset the system by outputting reset signals at power—on, and also output a reset signal when the 5 V output voltage drops below the specified 92% (TD62650FG / 652FG) or 85% (TD62651FG) because of external disturbances or other problem.

It also incorporates a watchdog timer for self-diagnosing the system. When the system malfunctions, the IC generates reset pulses intermittently to prevent the system from running away. The interface section incorporates three serial ports corresponding to the typical 24–V 4800 bps system in microcomputers.

The suffix (G) appended to the part number represents a Lead (Pb)-Free product



Weight: 0.63 g (typ.)

FEATURES

• Accurate output $5V \pm 0.25 \mathcal{Y}$

• Output PNP Tr incorporated : Current capacity; 300 mA (max)

• Power-on Reset timer incorporated

• Watchdog timer incorporated

Small flat package sealing : SSOP30 pm (1 mm pitch)

Difference 1

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CHARACTERISTIC	TD62650 / 652FG	TD62651FG
Reset Detecting Voltage	5V / 92%	5V / 85%

• Difference 2 Time setting resistance $22~k\Omega$ for power—on reset k watchdog timer, and PULL resistance of $4.7~k\Omega$ for RESET pin.

TD62650FG	TD62651FG	TD62652FG
Built-in	Nøne	None

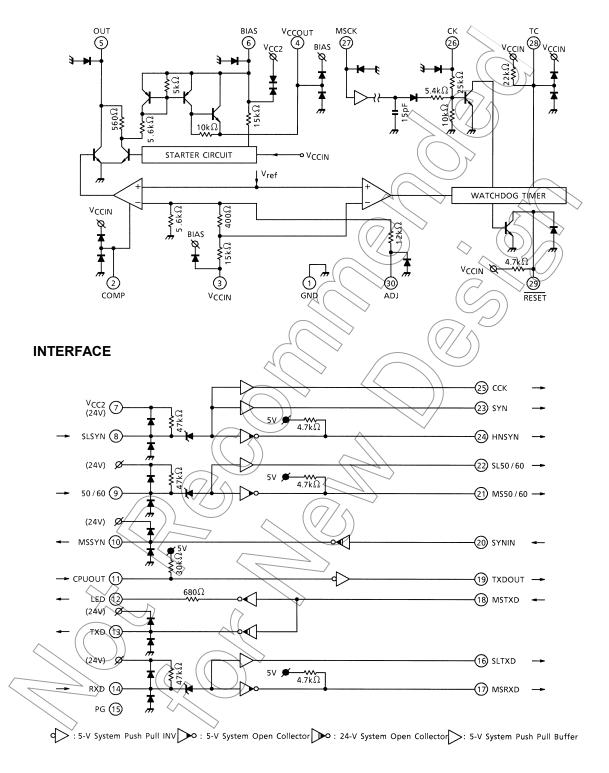
PIN CONNECTION

			_
GND [1	30] ADJ
сомр [2	29	RESET
V _{CCIN} [3	28] тс
∨ссоит [4	27] мѕск
оит [5	26] ск
BIAS [6	25] сск
V _{CC2} [7	24	HNSYN
SLSYN [8	23] SYN
50/60	9	22] SL50/60
MSSYN [10	21	MS50/60
CPUOUT [11	20	SYNIN
LED [12	19	ТХРООТ
TXD [13	18] MSTXD
RXD [14	17	MSRXD
PG [15	16] SLTXD

2006-06-14

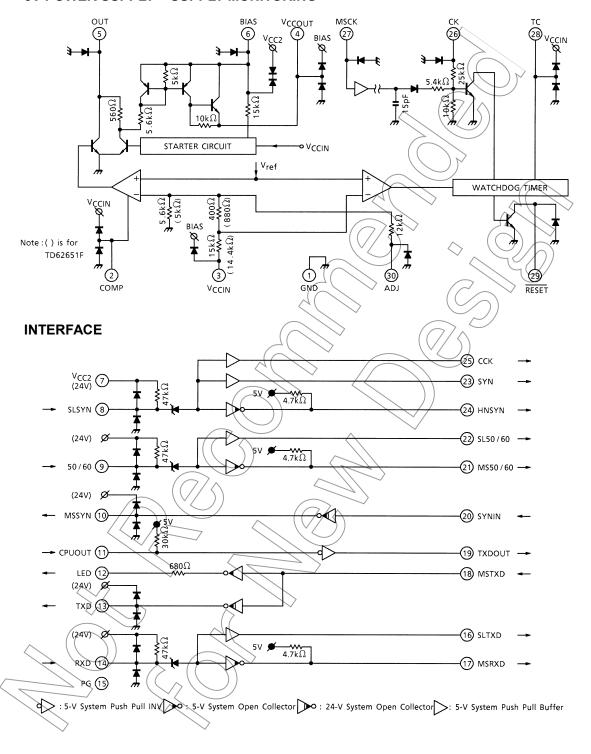
TD62650FG BLOCK DIAGRAM

5V POWER SUPPLY + SUPPLY MONITORING

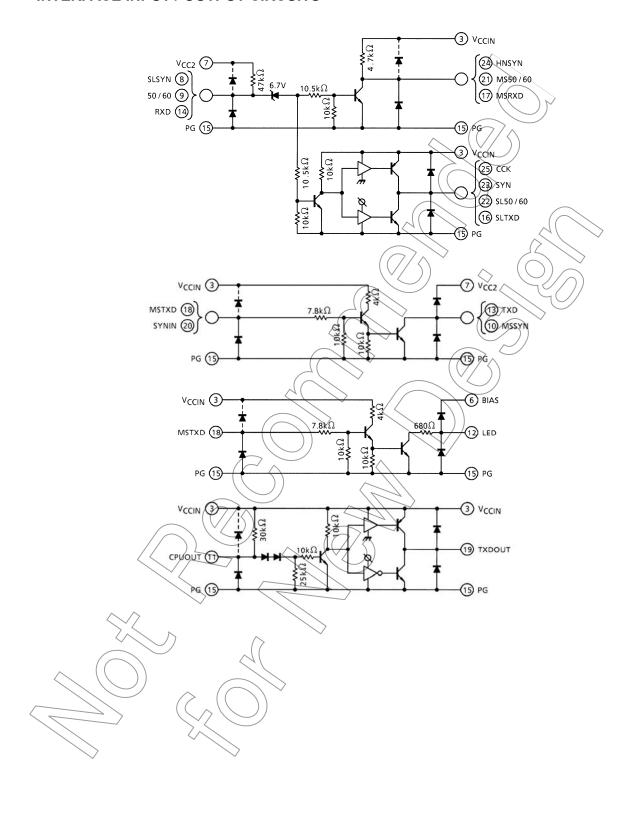


TD62651FG / TD62652FG BLOCK DIAGRAM

5V POWER SUPPLY + SUPPLY MONITORING



INTERFACE INPUT / OUTPUT CIRCUITS





PIN FUNCTION

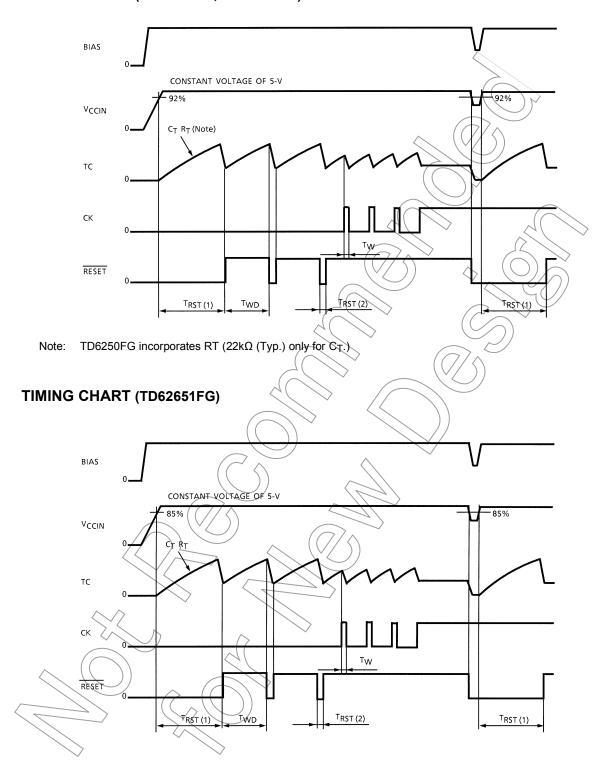
as an output pin for 5 V constant power supply through shorting with V _{CCIN} pin. Connected to the base of an external PNP transitior so that the output voltage is stabilized. Current design suitable for load capacities is thus possible. Since the recommended lour current is 5 mA, an output current of 300 mA is assured if the external transistor has an hFE of 60. When the internal transistor is used, it can be opened. Power supply starting pin. The starting current is supplied through a resistor to which the input voltage is applied. When V _{CCIN} rises above 3.0 V, the starting current is absorbed in the internal circuit; instead lour is supplied via V _{CCIN} . V _{CC2} Power supply pin for the 24–V system. Power supply pin for the 24–V system. Input pin for the 24–V system interface. Poll—up resistor 47 kΩ is incorporated at V _{CC2} pin. Input pin for the 24–V system interface. Pull—up resistor 47 kΩ is incorporated at V _{CC2} pin. Utput pin for the 24–V system Push / Pull inverter. Pull—up resistor 30 kΩ is incorporated at V _{CC1} pin. Pull input pin for the 24–V system open collector. LED LED lighting pin for the 8 system open collector. LED LED lighting pin for the 8 system open collector. AND Output pin for the 24–V system interface. Pull—up resistor 47 kΩ is incorporated at the V _{CC1} pin. PG GND pin for the 54–V system open collector. BLED LED lighting pin for the 54–V system interface. CHAPTER AND Input pin for the 54–V system open collector. Pull—up resistor 4.7 kΩ is incorporated at the V _{CC2} pin open collector. Pull—up resistor 4.7 kΩ is incorporated at the V _{CC2} pin open collector. Pull—up resistor 4.7 kΩ is incorporated at the V _{CC2} pin open collector. Pull—up resistor 4.7 kΩ is incorporated at the V _{CC2} pin open collector. Pull—up resistor 4.7 kΩ is incorporated at the V _{CC3} pin open collector. Pull—up resistor 4.7 kΩ is incorporated at the V _{CC4} pin open collector. Pull—up resistor 4.7 kΩ is incorporated at the V _{CC4} pin open collector. Pull—up resistor 4.7 kΩ is incorporated at V	PIN No.	PIN NAME	PIN FUNCTION
VCCIN Power supply pin for internal circuit. The output voltage can also be detected at this pin.	1	GND	GND pin for 5 V power supply and supply monitoring.
Output pin for built-in Power Tr, having a current capacitance of 300 ma (max). It is also use as an output pin for 5 V constant power supply through shorting with VCCIN pin. Connected to the base of an external PNP transistor, so that fife output voltage is stabilized. Current design suitable for load capacities is thus possible. Since the recommended lour current is 5 mA, an output current of 300 mA is assured if the external transistor has an hFE of 0.0. BIAS Power supply starting pin. The starting current is supplied through a resistor, to which the inproviding is applied. When VccIN rises above 3.0 V, the starting current is absorbed in the internal circuit; instead lour is supplied via VccIN. VCc2 Power supply pin for the 24-V system. SLSYN Input pin for the 24-V system interface. Pull-up resistor 47 kΩ is incorporated at Vcc2 pin. Input pin for the 24-V system open collector. Input pin for the 24-V system open collector. Input pin for the 5-V system open collector. LED LED lighting pin for the 8 system open collector. Full-up resistor 47 kΩ is incorporated. CUCIN pin. LED LED lighting pin for the 8 system open collector. Full-up resistor is incorporated. TXD Output pin for the 24-V system interface. Pull-up resistor 47 kΩ is incorporated at the Vcc2 pin. CUCIN pin. CED CED lighting pin for the 8 system open collector. Full-up resistor is incorporated. CUCIN pin. MSRXD Output pin for the 5-V system open collector. Pull-up resistor 4.7 kΩ is incorporated at the Vcc2 pin pin for the 5-V system open collector. Pull-up resistor 4.7 kΩ is incorporated at the Vcc3 pin for the 5-V system open collector. Pull-up resistor 4.7 kΩ is incorporated at the Vcc3 pin for the 5-V system pin for the formation pin formati	2	COMP	Phase compensation pin for output stabilization.
as an output pin for 5 V constant power supply through shorting with V _{CCIN} pin. Connected to the base of an external PNP transition so that the output voltage is stabilized. Current design suitable for load capacities is thus possible. Since the recommended logny current is 5 mA, an output current of 300 mA is assured if the external transistor has an hFE of 60. When the internal transistor has an hFE of 60. When the internal transistor has an hFE of 60. When the internal transistor has an hFE of 60. When V _{CCIN} pins sa pole 3.0 V, the starting current is absorbed in the internal circuit; instead voltage is applied. When V _{CCIN} pin for the 24–V system. Power supply pin for the 24–V system. SLSYN Input pin for the 24–V system interface. Pull-up resistor 47 kΩ is incorporated at V _{CC2} pin. Input pin for the 24–V system interface. Pull-up resistor 47 kΩ is incorporated at V _{CC2} pin. Uput pin for the 24–V system open collector. Input pin for the 5–V system open collector. LED LED lighting pin for the 8 system open collector. Both Uniquity pin for the 24–V system open collector. Both Uniquity pin for the 24–V system open collector. RXD Input pin for the 24–V system interface. Pull-up resistor 47 kΩ is incorporated at the V _{CC2} pin. TXD Output pin for the 24–V system open collector. Both Uniquity pin for the 24–V system open collector. RXD Input pin for the 24–V system interface. GND pin for (he 5–V) 24–V system interfaces. Output pin for the 5–V system open collector. Pull-up resistor 4.7 kΩ is incorporated at the V _{CC3} pin open collector. Pull-up resistor 4.7 kΩ is incorporated at the V _{CC4} pin open collector. Pull-up resistor 4.7 kΩ is incorporated at the V _{CC3} pin open collector. Pull-up pin for the 5–V system interface. SLTXD Output pin for the 5–V system interface. Output pin for the 5–V system open collector. Pull-up resistor 4.7 kΩ is incorporated at V _{CC1} pin. NSSO / 80 Output pin for the 5–V system open collector. Pull-up resistor 4.7 kΩ is incorporated at V _{CC1} pin. Output pin	3	V _{CCIN}	Power supply pin for internal circuit. The output voltage can also be detected at this pin.
Current design suitable for load capacities is thus possible. Since the recommended loar current is 5 mA, an output current of 300 mA is assured if the external transistor has an hFE of 60. When the internal transistor is used, it can be opened. Power supply starting pin. The starting current is supplied through a resistor to which the inproviding is applied. When Voca, rises above 3.0 V, the starting current is absorbed in the internal circuit, instead lour is supplied via Voca. Power supply pin for the 24–V system. Input pin for the 24–V system interface. Poll–up resistor 47 kΩ is incorporated at Voc2 pin. Input pin for the 24–V system interface. Poll–up resistor 47 kΩ is incorporated at Voc3 pin. CPUOUT Input pin for the 24–V system open collector. Input pin for the 5–V system open collector. 680 Q limiting resistor is incorporated. LED LED lighting pin for the 24–V system open collector. 680 Q limiting resistor is incorporated. LED Input pin for the 24–V system open collector. 680 Q limiting resistor is incorporated. RXD Input pin for the 24–V system open collector. 680 Q limiting resistor is incorporated. RXD Input pin for the 24–V system open collector. 680 Q limiting resistor is incorporated at the Voc2 pin. RXD Input pin for the 24–V system interface. Pull–up resistor 47 kΩ is incorporated at the Voc3 pin. RXD Input pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ is incorporated at the Voc3 pin. RXSXD Output pin for the 5–V system Push-Pull buffer. RXD Input pin for the 5–V system pine race. Pull–up resistor 4.7 kΩ is incorporated at the Voc3 pin. Input pin for the 5–V system pine race. Pull–up resistor 4.7 kΩ is incorporated at the Voc3 pin. Input pin for the 5–V system pine race. Pull–up resistor 4.7 kΩ is incorporated at Voc3 pin. Input pin for the 5–V system Push-Pull buffer. Output pin for the 5–V system Push-Pull buffer. Output pin for the 5–V system Push-Pull buffer.	4	V _{CCOUT}	Output pin for built-in Power Tr, having a current capacitance of 300 mA (max). It is also used as an output pin for 5 V constant power supply through shorting with V _{CCIN} pin.
Voc2 Power supply pin for the 24–V system. 7 Vcc2 Power supply pin for the 24–V system. 8 SLSYN Input pin for the 24–V system interface. Pull–up resistor 47 kΩ is incorporated at Vcc2 pin. 9 50 / 60 Input pin for 24–V system interface. Pull–up resistor 47 kΩ is incorporated at Vcc2 pin. 10 MSSYN Output pin for the 24–V system open collector. 11 CPUOUT Input pin for the 5–V system open collector. 12 LED LED lighting pin for the 8 system open collector. 13 TXD Output pin for the 24–V system interface. Pull–up resistor 30 kΩ is incorporated at Vcc1 pin. 14 RXD Input pin for the 8 system open collector. 15 PG GND pin for the 24–V system interface. Pull–up resistor 47 kΩ is incorporated at the Vcc2 pin. 16 SLTXD Output pin for the 5–V system interface. Pull–up resistor 47 kΩ is incorporated at the Vcc2 pin. 17 MSRXD Output pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ is incorporated at the Vcc1 pin. 18 MSTXD Input pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ is incorporated at the Vcc1 pin. 19 TXDOUT Output pin for the 5–V system push–Pull buffer. 19 SYNIN Input pin for the 5–V system interface. 20 Utput pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ is incorporated at Vcc1 pin. 21 MSSYN Output pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ is incorporated at Vcc1 pin. 22 SL50 / 60 Output pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ is incorporated at Vcc1 pin. 24 HNSYN Output pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ is incorporated at Vcc1 pin. 24 HNSYN Output pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ incorporated at Vcc1 pin.	5	ОИТ	Current design suitable for load capacities is thus possible. Since the recommended I _{OUT} current is 5 mA, an output current of 300 mA is assured if the external transistor has an hFE of 60.
SLSYN Input pin for the 24-V system interface. Pull-up resistor 47 kΩ is incorporated at V _{CC2} pin.	6	BIAS	When V _{CCIN} rises above 3.0 V, the starting current is absorbed in the internal circuit; instead,
9 50 / 60 Input pin for 24–V system interface. Pull-up resistor 47 kΩ is incorporated at V _{CC2} pin. 10 MSSYN Output pin for the 24–V system open collector. 11 CPUOUT Input pin for the 5–V system Push / Pull inverter. Pull-up resistor 30 kΩ is incorporated at V _{CCIN} pin. 12 LED LED lighting pin for the 8 system open collector. 680 Q limiting resistor is incorporated. 13 TXD Output pin for the 24–V system open collector. 14 RXD Input pin for the 24–V system interface. Pull-up resistor 47 kΩ is incorporated at the V _{CC2} pin. 15 PG GND pin for the 5–V system interfaces. 16 SLTXD Output pin for the 5–V system open collector. Pull-up resistor 4.7 kΩ is incorporated at the V _{CCIN} pin. 17 MSRXD Output pin for the 5–V system Push-Pull buffer. 18 MSTXD Input pin for the 5–V system interface, for input at LED (12 pin) and TXD (13 pin) pins. 19 TXDOUT Output pin for the 5–V system Push-Pull inverter (CPUOUT : 11 pin). 20 SYNIN Input pin for the 5–V system open collector. Pull-up resistor 4.7 kΩ is incorporated at V _{CCI} pin. 21 MS50 / 60 Output pin for the 5–V system open collector. Pull-up resistor 4.7 kΩ is incorporated at V _{CCI} pin. 22 SL50 / 60 Output pin for the 5–V system open collector. Pull-up resistor 4.7 kΩ is incorporated at V _{CCI} pin. Output pin for the 5–V system Push / Pull buffer. Output pin for the 5–V system Push / Pull buffer. Output pin for the 5–V system Push / Pull buffer.	7	V _{CC2}	Power supply pin for the 24–V system.
10 MSSYN Output pin for the 24–V system open collector. 11 CPUOUT Input pin for the 5–V system Push / Pull inverter. Pull–up resistor 30 kΩ is incorporated at VCCIN pin. 12 LED LED lighting pin for the 8 system open collector. 680 Ω limiting resistor is incorporated. 13 TXD Output pin for the 24–V system open collector. 14 RXD Input pin for the 24–V system interface. Pull–up resistor 47 kΩ is incorporated at the VCC2 pin. 15 PG GND pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ is incorporated at the VCC1 pin. 16 SLTXD Output pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ is incorporated at the VCC1 pin. 17 MSRXD Output pin for the 5–V system Push–Pull buffer. 18 MSTXD Input pin for the 5–V system Push–Pull inverter (CPUOUT : 11 pin). 19 TXDOUT Output pin for the 5–V system interface. 21 MS50 / 60 Output pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ is incorporated at VCC1 pin. 22 SL50 / 60 Output pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ is incorporated at VCC1 pin. Output pin for the 5–V system Push / Pull buffer. 23 SYN Output pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ is incorporated at VCC1 pin. Output pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ is incorporated at VCC1 pin. Output pin for the 5–V system Push - Pull buffer. Output pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ incorporated at VCC1 pin.	8	SLSYN	Input pin for the 24-V system interface. Pull-up resistor 47 kΩ is incorporated at V _{CC2} pin.
Input pin for the 5-V system Push / Pull inverter. Pull-up resistor 30 kΩ is incorporated a VCCIN pin. LED LED lighting pin for the 8 system open collector. 680 Q limiting) resistor is incorporated. TXD Output pin for the 24-V system open collector. RXD Input pin for the 24-V system interface. Pull-up resistor 47 kΩ is incorporated at the VCC2 pin. PG GND pin for the 5-V 24-V system interfaces. 16 SLTXD Output pin for the 5-V system open collector. Pull-up resistor 4.7 kΩ is incorporated at the VCCIN pin. 17 MSRXD Output pin for the 5-V system Push-Pull buffer. 18 MSTXD Input pin for the 5-V system interface, for input at LED (12 pin) and TXD (13 pin) pins. 19 TXDOUT Output pin for the 5-V system interface. 21 MS50 / 60 Output pin for the 5-V system open collector. Pull-up resistor 4.7 kΩ is incorporated at VCCI pin. 22 SL50 / 60 Output pin for the 5-V system Push / Pull buffer. 23 SYN Output pin for the 5-V system Push / Pull buffer. Output pin for the 5-V system Push / Pull buffer. Output pin for the 5-V system Push / Pull buffer. Output pin for the 5-V system Push / Pull buffer. Output pin for the 5-V system Push / Pull buffer. Output pin for the 5-V system open collector. Pull-up resistor 4.7 kΩ is incorporated at VCCI pin. Output pin for the 5-V system open collector. Pull-up resistor 4.7 kΩ is incorporated at VCCI pin.	9	50 / 60	Input pin for 24–V system interface. Pull-up resistor 47 k Ω is incorporated at V_{CC2} pin.
12 LED LED lighting pin for the 8 system open collector. 680 Ω limiting resistor is incorporated. 13 TXD Output pin for the 24–V system open collector. 14 RXD Input pin for the 24–V system interface. Pull–up resistor 47 kΩ is incorporated at the V _{CC2} pin 15 PG GND pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ is incorporated at the V _{CCIN} pin. 16 SLTXD Output pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ is incorporated at the V _{CCIN} pin. 17 MSRXD Output pin for the 5–V system Push–Pull buffer. 18 MSTXD Input pin for the 5–V system push–Pull inverter (CPUOUT : 11 pin). 19 TXDOUT Output pin for the 5–V system push–Pull inverter (CPUOUT : 11 pin). 20 SYNIN Input pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ is incorporated at V _{CCIN} pin. 21 MS50 / 60 Output pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ is incorporated at V _{CCIN} pin. 22 SL50 / 60 Output pin for the 5–V system Push / Pull buffer. 23 SYN Output pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ incorporated at V _{CCIN} pin. 24 HNSYN Output pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ incorporated at V _{CCIN} pin.	10	MSSYN	Output pin for the 24-V system open collector.
13 TXD Output pin for the 24–V system open collector. 14 RXD Input pin for the 24–V system interface. Pull-up resistor 47 kΩ is incorporated at the V _{CC2} pin 15 PG GND pin for the 5–V system open collector. Pull-up resistor 4.7 kΩ is incorporated at the V _{CC1} pin. 16 SLTXD Output pin for the 5–V system open collector. Pull-up resistor 4.7 kΩ is incorporated at the V _{CC1} pin. 17 MSRXD Output pin for the 5–V system Push-Pull buffer. 18 MSTXD Input pin for the 5–V system interface, for input at LED (12 pin) and TXD (13 pin) pins. 19 TXDOUT Output pin for the 5–V system Push-Pull inverter (CPUOUT : 11 pin). 20 SYNIN Input pin for the 5–V system open collector. Pull-up resistor 4.7 kΩ is incorporated at V _{CC1} pin. 21 MS50 / 60 Output pin for the 5–V system Push / Pull buffer. 23 SYN Output pin for the 5–V system Push-Pull buffer. 24 HNSYN Output pin for the 5–V system open collector. Pull-up resistor 4.7 kΩ incorporated at V _{CC1} pin.	11	CPUOUT	Input pin for the 5-V system Push / Pull inverter. Pull-up resistor 30 k Ω is incorporated at VCCIN pin.
Input pin for the 24–V system interface. Pull–up resistor 47 kΩ is incorporated at the V _{CC2} pin PG GND pin for the 5–V 24–V system interfaces. Output pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ is incorporated at the V _{CC1} pin. MSRXD Output pin for the 5–V system Push–Pull buffer. MSTXD Input pin for the 5–V system interface, for input at LED (12 pin) and TXD (13 pin) pins. TXDOUT Output pin for the 5–V system Push–Pull inverter (CPUOUT : 11 pin). SYNIN Input pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ is incorporated at V _{CC1} pin. Utput pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ is incorporated at V _{CC1} pin. Output pin for the 5–V system Push–Pull buffer. SYN Output pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ incorporated at V _{CC1} pin. Output pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ incorporated at V _{CC1} pin.	12	LED	LED lighting pin for the 8 system open collector. 680 Ω limiting resistor is incorporated.
15 PG GND pin for the 5–V \ 24–V system interfaces. 16 SLTXD Output pin for the 5–V system open collector. Pull-up resistor 4.7 kΩ is incorporated at the VCC/N pin. 17 MSRXD Output pin for the 5–V system Push–Pull buffer. 18 MSTXD Input pin for the 5–V system interface, for input at LED (12 pin) and TXD (13 pin) pins. 19 TXDOUT Output pin for the 5–V system Push–Pull inverter (CPUOUT : 11 pin). 20 SYNIN Input pin for the 5–V system interface. 21 MS50 / 60 Output pin for the 5–V system open collector. Pull-up resistor 4.7 kΩ is incorporated at VCCI pin. 22 SL50 / 60 Output pin for the 5–V system Push / Pull buffer. 23 SYN Output pin for the 5–V system open collector. Pull-up resistor 4.7 kΩ incorporated at VCCI pin. 24 HNSYN Output pin for the 5–V system open collector. Pull-up resistor 4.7 kΩ incorporated at VCCI pin.	13	TXD	Output pin for the 24-V system open collector.
16 SLTXD Output pin for the 5-V system open collector. Pull-up resistor 4.7 kΩ is incorporated at the V _{CCIN} pin. 17 MSRXD Output pin for the 5-V system Push-Pull buffer. 18 MSTXD Input pin for the 5-V system interface, for input at LED (12 pin) and TXD (13 pin) pins. 19 TXDOUT Output pin for the 5-V system Push-/Pull inverter (CPUOUT : 11 pin). 20 SYNIN Input pin for the 5-V system interface. 21 MS50 / 60 Output pin for the 5-V system open collector. Pull-up resistor 4.7 kΩ is incorporated at V _{CCI} pin. 22 SL50 / 60 Output pin for the 5-V system Push / Pull buffer. 23 SYN Output pin for the 5-V system open collector. Pull-up resistor 4.7 kΩ incorporated at V _{CCI} pin. 24 HNSYN Output pin for the 5-V system open collector. Pull-up resistor 4.7 kΩ incorporated at V _{CCI} pin.	14	RXD	Input pin for the 24–V system interface. Pull–up resistor 47 k Ω is incorporated at the V $_{CC2}$ pin.
VCCIN pin: 17 MSRXD Output pin for the 5–V system Push–Pull buffer. 18 MSTXD Input pin for the 5–V system interface, for input at LED (12 pin) and TXD (13 pin) pins. 19 TXDOUT Output pin for the 5–V system Push / Pull inverter (CPUOUT : 11 pin). 20 SYNIN Input pin for the 5–V system interface. 21 MS50 / 60 Output pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ is incorporated at VCCI pin. 22 SL50 / 60 Output pin for the 5–V system Push / Pull buffer. 23 SYN Output pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ incorporated at VCCI pin. Output pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ incorporated at VCCI pin.	15	PG	GND pin for the 5-V \ 24-V system interfaces.
MSTXD Input pin for the 5-V system interface, for input at LED (12 pin) and TXD (13 pin) pins. 19 TXDOUT Output pin for the 5-V system Push / Pull inverter (CPUOUT : 11 pin). 20 SYNIN Input pin for the 5-V system open collector. Pull-up resistor 4.7 kΩ is incorporated at V _{CCI} pin. 21 MS50 / 60 Output pin for the 5-V system Push / Pull buffer. 22 SL50 / 60 Output pin for the 5-V system Push / Pull buffer. 23 SYN Output pin for the 5-V system Push-Pull buffer. 24 HNSYN Output pin for the 5-V system open collector. Pull-up resistor 4.7 kΩ incorporated at V _{CCI} pin.	16	SLTXD	Output pin for the 5-V system open collector. Pull-up resistor 4.7 k Ω is incorporated at the VCCIN pin.
19 TXDOUT Output pin for the 5–V system Push / Pull inverter (CPUOUT : 11 pin). 20 SYNIN Input pin for the 5–V system interface. 21 MS50 / 60 Output pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ is incorporated at V _{CCI} pin. 22 SL50 / 60 Output pin for the 5–V system Push / Pull buffer. 23 SYN Output pin for the 5–V system Push–Pull buffer. 24 HNSYN Output pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ incorporated at V _{CCI} pin.	17	MSRXD	Output pin for the 5-V system Push-Pull buffer.
20 SYNIN Input pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ is incorporated at V _{CCI} 21 MS50 / 60 Output pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ is incorporated at V _{CCI} 22 SL50 / 60 Output pin for the 5–V system Push / Pull buffer. 23 SYN Output pin for the 5–V system Push–Pull buffer. 24 HNSYN Output pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ incorporated at V _{CCI}	18	MSTXD	Input pin for the 5-V system interface, for input at LED (12 pin) and TXD (13 pin) pins.
21 MS50 / 60 Output pin for the 5-V system open collector. Pull-up resistor 4.7 kΩ is incorporated at V _{CCI} pin. 22 SL50 / 60 Output pin for the 5-V system Push / Pull buffer. 23 SYN Output pin for the 5-V system Push-Pull buffer. 24 HNSYN Output pin for the 5-V system open collector. Pull-up resistor 4.7 kΩ incorporated at V _{CCI} pin.	19	TXDOUT	Output pin for the 5-V system Push / Pull inverter (CPUOUT : 11 pin).
pin. 22 SL50 / 60 Output pin for the 5–V system Push / Pull buffer. 23 SYN Output pin for the 5–V system Push–Pull buffer. 24 HNSYN Output pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ incorporated at V _{CCI}	20	SYNIN	Input pin for the 5-V system interface.
23 SYN Output pin for the 5–V system Push–Pull buffer. 24 HNSYN Output pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ incorporated at V _{CCI}	21	MS50 / 60	Output pin for the 5–V system open collector. Pull–up resistor 4.7 k Ω is incorporated at V _{CCIN} pin.
Output pin for the 5–V system open collector. Pull–up resistor 4.7 kΩ incorporated at V _{CCI} pin.	22	SL50 / 60	Output pin for the 5-V-system Push / Pull buffer.
pin.	23	SYN	Output pin for the 5-V system Push-Pull buffer.
25 CCK Output pin for the 5–V system Push–Pull buffer.	24	HNSYN	Output pin for the 5–V system open collector. Pull-up resistor 4.7 k Ω incorporated at V _{CCIN} pin.
	25 (CCK	Output pin for the 5-V system Push-Pull buffer.

PIN No.	PIN NAME	PIN FUNCTION					
26	СК	Input pin for watchdog timer. The pin is pulled up to V _{CCIN} if the IC is used only as a power–on reset timer.					
27	MSCK	To input clock pulses, one-shot pulses can be generated for CK (26 pin) inputs at the rise edge. When the pin is not used, short it with GND.					
28	TC	Time setting pin for the reset and watchdog timers.					
29	RESET	NPN transistor open-collector output. (1) The signal goes low when the output voltage drops below the specified 92% (TD62650 / 652) or 85% (651) level. (2) The pin generates a reset signal that is determined by the external condenser connected to the TC pin. (3) The pin generates reset pulses intermittently if no clock is attached to the CK pin. This function can be used as a watchdog time for microcomputers.					
30	ADJ	Output voltage adjusting pin. The voltage will increase when a resistor is connected between ADJ and GND (1 pin). It can reduce the voltage when the resistor is inserted between ADJ and V_{CCIN} (3 pin). The voltage can be changed by a maximum of \pm 1V.					



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TIMING CHART (TD62650FG, TD62652FG)





ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT	PIN
	VV _{CC24}	-0.4~35	V	V _{CC2} , BIAS
Input Voltage	VV _{CCIN}	-0.4~7	V	VCCIN
	V _{IN24} (Condition 1) (Condition 2)	-0.4~VV _{CC2} + 0.4-0.4~30	V	SLSYN, 50 / 60, RXD
	V _{IN5}	-0.4~VV _{CCIN} + 0.4	٧	CRUOUT, MSCK, ADJ, COMP, CK, TC, SYNIN, MSTXD
	V _{OUT24}	-0.4~VV _{CC2} + 0.4	V	MSSYN, TXD
	VVccout	-0.4~V _{BIAS} + 0.4	v_((VCCOUT, OUT
Output Voltage	V _{LED} (Condition 3) (Condition 4)	-0.4~V _{BIAS} + 0.4-0.4~10	(X)	LED 🔷
	V _{OUT5}	-0.4~VVCCIN + 0.4	1	RESET, CCK, HNSYN, SYN, SL50 / 60, MS50 / 60, TXDOUT, MSRXD, SLTXD
	lout	10	>mA	OUT)
	I _{RESET}	4	mA	RESET
Output Current	I _{OUT} Push / Pull	±4	mA / ch	CCK, SYN, SL50 / 60, TXDOUT, SLTXD
	I _{OUT5}	10	m/ch	HNSYN, MS50 / 60, LED, MSRXD
	louf24	24	mA / ch	MSSYN, TXD
	IACCONT)) 300	mA	Vccouт
Power Dissipation	P _D (Note 5)	1.47	⟨ w	·
Operating Temperature	(T _{opr})	-40~85)°¢	
Storage Temperature	Tstg	-55~150	(°C)	

Condition 1: $VV_{CC2} \le 29.6 \text{ V}$ Condition 2: $VV_{CC2} > 29.6 \text{ V}$ Condition 3: $V_{BIAS} \le 9.6 \text{ V}$ Condition 4: $V_{BIAS} > 9.6 \text{ V}$

Note 5: Board mounting time $(50 \times 50 \times 4.6 \text{ mm, Cu} = 30\%)$





DC ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{CCIN} = 5 V)

Interface Section

CHARACTERISTIC	SYMBOL	PIN	TEST CIR- CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Input Voltage	V _{IH5}	(Note 1)			V _{CCIN} × 70%	1/2	l	
	V _{IL5}	(14010-1)	_				V _{CCIN} × 30%	V
	V _{IH24}	(Note 1)			(13)	l	V _{CC2} + 0.4	
	V _{IL24}				-0.4	_	7	
	I _{IH5-1}	(Note 3)		V _{IN} = 5 V	320	462	600	μA / ch
	I _{IL5-1}	(Note 3)		VIN = ØV	-	0 (10	
	I _{IH5-2}	(Note 7)		V _{IN} = 5 V	480	690	940	μA
Input Current	I _{IL5-2}	(14010-17)	- (V _{IIN} ₹0, V	115	170	240	
	I _{IH24}	(Note 2)		V _{IN} = 24 V	1.1	1.6	2.1	mA / ch
	I _{IL24}		1	V _{IN} = 0 V	350	510	690	μA
	V _{OH5-1}	4		J _{OH} = -20 μA	Vec -0.1) –	_	
	V _{OH5-2}	(Note 4)		I _{OH} = -4 mA	V _{CCIN} × 70%	_	_	
	V _{OL5-1}		~	I _O _L = 20 μA	<u>/</u> _	_	0.1	٧
Output Voltage	V _{OL5-2}		_ <	I _{OL} = 4 mA	1	l	V _{CCIN} × 30%	
	V _{OL5} -3	(Note 5)		I _{IN} = 500 μA I _{OL} = 10 mA	ı	ı	0.5	
	(VOL LED	LED		l _{IN} = 200 μA lo _L = 1 mA	-	_	1.4	
	V _{OL24}	(Note 6)		I _{IN} = 200 μA I _{OL} = 24 mA	1	l	0.5	
Output Impedance	R _{OL} LED	LED	\rightarrow	(Note 8)	540	680	1000	Ω
Surpar Impodantos	R _{OH5}	(Note 5)	($)$	(Note 9)	3.2	4.7	6.2	kΩ
Current Consumption 24	IV _{CC2}			VV _{CC2} = 24 V	_	1.6	2.1	mA
Leakage Current	ILEAK24	(Note 6)	_	V _{OH} = 24.0 V			10	μA
	I _{LEAK5}	(Note 4)		V _{OH} = 5 V	_	_	10	μΛ
Output Shorting Current	I _{OS} (Note)	(Note 4)		V _{CCIN} = 5.25 V V _{OH} = 0 V	_	17.5	_	mA

Note: Two outputs or more must not be shorted at the same time. Shorting duration must be limited to less than 1 second.

Note 1: CPUOUT, SYNIN, MSTXD

Note 2: SLSYN, 50 / 60, RXD/

Note 3: SYNIN, MSTXD

Note 4: CCK, SYN, SL50 / 60, TXDQUT, SLTXD

Note 5: HNSYN, MS50 / 60, MSRXD

Note 6: MSSYN, TXD

Note 7: CPUOUT

Note 8: $(V_{OL} (@l_{OL} = 5 \text{ mA}) - V_{OL} (@l_{OL} = 1 \text{ mA})) \div 4 \text{ mA}$

Note 9: $4 \text{ V} \div (@I_{OH} (V_{OH} = 0 \text{ V}) - @I_{OH} (VOH = 4 \text{ V}))$



DC ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{BIAS} = 7 to 17 V, Ta = -40 to 85°C) 5V power supply, supply monitoring section

CHARACTERISTIC	SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Output Voltage	V _{CCOUT}	_	IV _{CCOUT} = 0.1 A	4.75	5.0	5.25	٧
Input Stability	V _{CCOUT} LINE		V _{BIAS} = 7~35 V		0.1	0.5	%
Load Stability	V _{CCOUT} LOAD		IVCCOUT = 1~150 mA		0.1	0.5	%
Temperature Coefficient	V _{CCOUT} t)	0.01	_	% / °C
Output Voltage	V _{OL} RESET		I _{OL} = 2 mA)/-		0.5	٧
Output Leakage Current	LEAK RESET		V _{RESET} = 7 V	_	-<	(5/	μA
Input Current	I _{TC}		V _{TC} = 0 to 3.5 V (Note 8)	-3	1	3/	μA
Threshold Voltage	V _{TC} H		RESET "High" to "Low"	<>- (80% × VCCIN	7(3	V
Threshold Voltage	V _{TC} L		RESET "Low" to "High"		40% × V _{CCIN}		•
Input Current	I _{CK}		V _{IN} = 5 V (Note 8)	G	0.3	0.7	mA
Input Voltage	V_{IH}		(Note 4)	V _{CCIN} × 70%	<i>/</i> –	l	V
input voitage	V _{IL}	7	(Note 4))}	1	V _{CCIN} × 30%	
Reset Detecting Voltage	V _{CC} RESET		TD62650 /652FG	89% × V _{CCIN}	92% × V _{CCIN}	95% × V _{CCIN}	V
Neset Detecting Voltage	VCC KLOLI		TD62651FG	82% × V _{CCIN}	85% × V _{CCIN}	88% × V _{CCIN}	V
Output Impedance	RESET		TD62650FG (Note 1)	3.2	4.7	6.2	kΩ
	ROH TC		TD62650FG (Note 1)	15	22	29	
Current Consumption 5	IVCCIN		(Note 2)	_	5	6.5	mA
ourient consumption o	IVCCIN		(Note 5)	_	11.5	15.0	ША
Bias Current Consumption	7 I _{BIAS}	/-/	V _{BIAS} = 8V (Note 7)		1.73	2.25	mA
Watchdog Timer	TWD		TD62650FG (Note 6)	15.4 × CT	24.2 × CT	33.0 × CT	ms
	TWD		TD62651 /652FG	0.9 × CTRT	1.1 × CTRT	1.3 × CTRT	s
Reset Timer (1) (Note 3)	(1)		TD62650FG (Note 6)	24.2 × CT	35.2 × CT	48.4 × CT	ms
Note 3)	TRST (1)		TD62651 / 652FG	1.3 × CTRT	1.6 × CTRT	1.9 × CTRT	ø
Reset Timer (Note 3)	T _R ST (2)	_	(Note 6)	300 × CT	600 × CT	900 × CT	ms

CHARACTERISTIC	SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Clock Input Pulse width	TW CK	_		3	_	_	μs
Maximum Response Frequency 1	f _{MAX} MSCK	_		2	_	_	kHz
Maximum Response Frequency 2	f _{MAX} CK	_		10	7	_	kHz
Msck Pin Input Signal Rise Time	tr MSCK	_	(Note 9)	+/	7	500	ns
Minimum Input / Output Voltage Difference	V _{OH} V _{CCOUT}		IV _{CCOUT} = 0.1 A	77		1.5	V

Note 1: $4 \text{ V} \div (@I_{OH} (V_{OH} = 0 \text{ V}) - @I_{OH} (V_{OH} = 4 \text{ V})$

Note 2: V_{BIAS} = 8 V, V_{CCIN} - V_{CCOUT} Short Open Collector I / O : Open

Open Collector I / O : Open
Push-Pull I / O : Open
MSCK Input : Open

Note 3: Reset Timer (1) : Power On Reset Time

Reset Timer (2) : Watchdog Reset Time

Note 4: MSCK, CK Pins

Note 5: HNSYN, MS50 / 60, MSRXD Pull / UP Resistance + CCK, SYN, SL50 / 60, TXDOUT, SLTXD Driving Current

Note 6: CT Unit (μF)

Note 7: V_{CCIN}, V_{CCOUT} Open Note 8: Only TD62651FG, TD62652FG

Note 9: Input Condition 5 V : 0 to 100%

AC ELECTRICAL CHARACTERISTICS (Ta = 25°C)

		1		1				
CHARACTERISTIC	CHARACTERISTIC / INPUT CONDITION	SYMBOL	TEST CIR- CUIT	OUTPUT CONDITION	MIN	TYP.	MAX	UNIT
	SLSYN-CCK	tpLH		(Note 4)	P	0.6	-	
	(Note 1)	tpHL		(Note 4)	-	1.5	_	
	SLSYN-SYN	tpLH		(Note 4)	+	0.6	_	
	(Note 1)	tpHL		(Note 4)	\ \ \ \		_	
	SLSYN-HNSYN	tpLH		(Note 5)	//-\	0.5	1	
	(Note 1)	tpHL		(Note 5)		0.1	_	
	50 / 60-MS50 / 60	tpLH		(Note 5)	>-	0.5	_	
	(Note 1)	tpHL		(1.5.0 3)	<i>)</i> –	0.1	_	
	50 / 60-SL50 / 60	tpLH		(Note 4)	_	0.6	$\overline{}$	
	(Note 1)	tpHL		(11342-1)	_	1.5	_ \	7
Propagation Delay Time (tpLH: 50%-50%,	SYNIN-MSSYN	tpLH	4	(Note 3)	- /	1.0	\nearrow	μs
tpHL: 50%-50%)	(Note 2)	tpHL		(10.00)	>- \	0.1		
	CPUOUT-TXDOUT	tpLH ((Note 4)	_/	1.0	<i>JF</i>	
	(Note 2)	tpHL		\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	<u> </u>	1.2		
	MSTXD-LED (Note 2)	tpLH	>> >	(Note 5)	\mathcal{L}_{p}	0.5	_	
		tpHL		(0)	<u> </u>	0.1	_	
	MSTXD-TXD (Note 2)	tpLH		(Note 3)) -	1.0	_	
		tpHL			_	0.1	_	
	RXD-SLTXD (Note 1)	tpLH		(Note 4)	_	0.6	_	
	(Note I)	tpHL	\wedge		_	1.5	_	
	RXD-MSRXD (Note 1)	tpLH		(Note 5)		0.5		
		tpHL				0.1	_	
	MS50 / 60	_	16	<u> </u>	_	0.3	_	
	SL50/60/		7/	>	_	0.2	_	
	LED	(0)			_	0.2	_	
	MSSYN				_	1.1	_	
Rise Time	TXDOUT					0.2	_	
(tr: 10%-90%)	TXD	tr	_		_	1.1	_	μs
	SYN				_	0.2	_	
	CCK	· ·			_	0.2		
	HNSYN				_	0.3		
	SLTXD					0.2		
	WIGHT			<u> </u>		0.5		

CHARACTERISTIC	CHARACTERISTIC / INPUT CONDITION	SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
	MS50 / 60					0.1	_	
	SL50 / 60				4	0.5	_	
	LED				7	0.1	_	
	MSSYN				+/	0).1	_	
Fall Time	TXDOUT					0.5	I	
(tr: 90%-10%)	TXD	tf	_		$\langle\!/-\!\rangle)$	0.1	I	μs
(11. 3070 1070)	SYN))	0.5	1	
	ССК				>	0.5		
	HNSYN				/ _	0.1	١ (
	SLTXD			$\mathcal{A}(\mathcal{A})$		0.5	/	>
	MSRXD				_	0.1		<i>Y</i>

Input / Output Conditions

Input Condition

Note 1: 24-V System $\,:\,$ 0.2 μ s at 2 to 22-V Note 2: 5-V System : 0.1µs at 30 to 70%

Output Conditions

Note 3: 24-V System : C_L = 50 pF Note 4: 5-V System : C_L = 50 pF

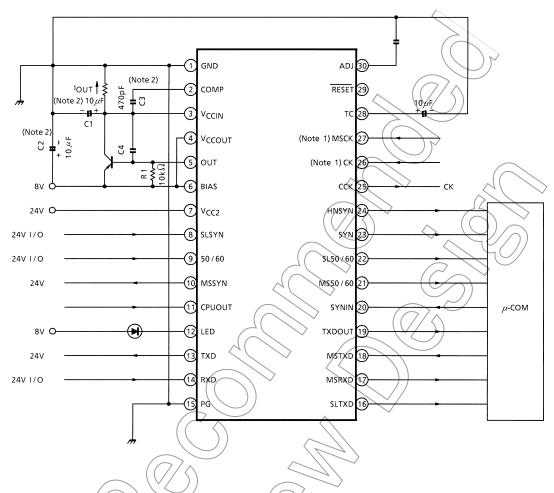
 $R_L = 5 k\Omega$

: C_L = 50 pF Note 5: 5-V System

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APPLICATION CIRCUIT

When using an external PNP transistor:



Note 1: When using the MSCK pin, short circuit the CK pin with GND.

When using the CK pin, short circuit the MSCK pin with GND.

Note 2: C1 and C2 are necessary to absorb external noise, etc. Connect them as close to the IC as possible.

C3 is used for phase correction, but this also must be connected as close to the IC as possible.

We recommend that C4 be connected between OUT and V_{CCIN}.

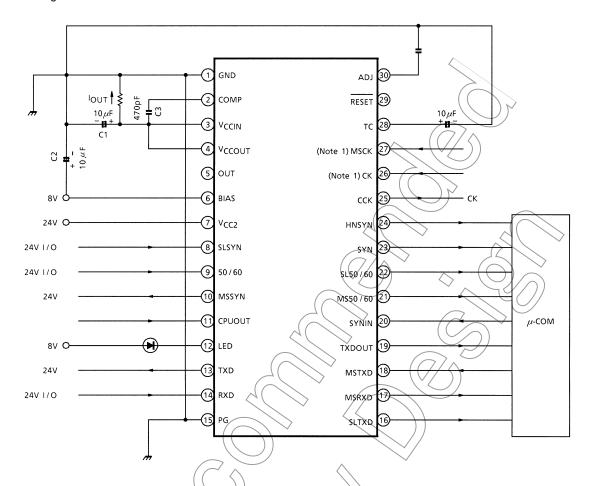
PRECAUTIONS for USING

This IC does not integrate protection circuits such as overcurrent and overvoltage protectors.

Thus, if excess current or voltage is applied to the IC, the IC may be damaged. Please design the IC so that excess current or voltage will not be applied to the IC.

Utmost care is necessary in the design of the output line, VCC (VCCIN, VCCOUT, BIAS, VCC2) and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

When using a built-in PNP transistor:



Note 1: When using the MSCK pin, short the CK pin with GND.

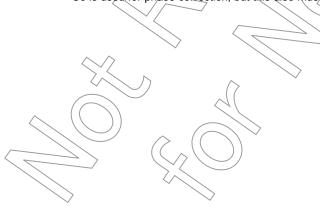
When using the CK pin, short the MSCK pin with GND.

Note 2: C1 and C2 are necessary to absorb external noise, etc.

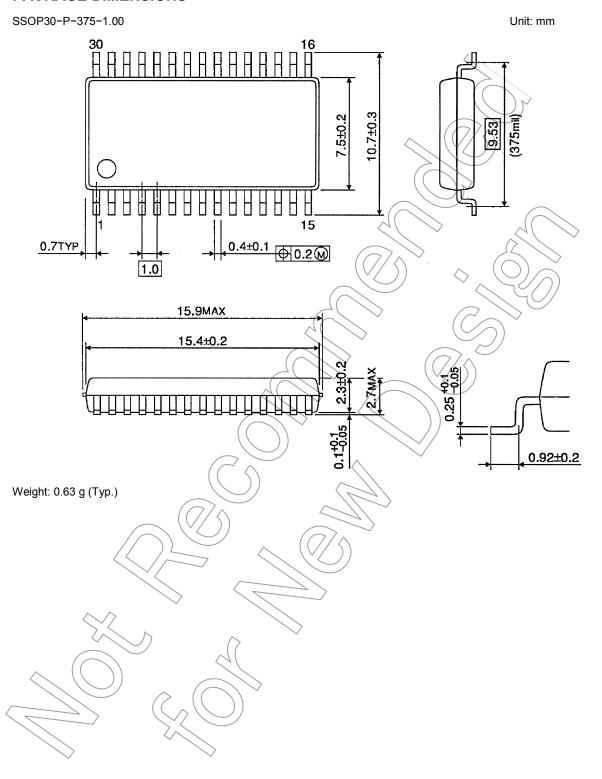
Connect them as close to the IC as possible.

C3 is used for phase correction, but this also must be connected as close to the IC as possible.

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PACKAGE DIMENSIONS



Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only.

Thorough evaluation is required, especially at the mass production design stage.

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IC Usage Considerations

Notes on Handling of ICs

- (1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.

 Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
- (2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.
- (3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.

 Use a stable power supply with ICs with built in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.
- (4) (Do not insert devices in the wrong orientation or incorrectly.

 Make sure that the positive and negative terminals of power supplies are connected properly.

 Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
 - In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.
- (5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.

 If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

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Points to Remember on Handling of ICs

(1) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (Tj) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(2) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink-eapability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.



About solderability, following conditions were confirmed

- · Solderability
 - (1) Use of Sn-37Pb solder Bath
 - · solder bath temperature = 230°C
 - · dipping time = 5 seconds
 - · the number of times = once
 - · use of R-type flux
 - (2) Use of Sn-3.0Ag-0.5Cu solder Bath
 - · solder bath temperature = 245°C
 - · dipping time = 5 seconds
 - · the number of times = once
 - · use of R-type flux

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