



3-wire Serial EEPROM 1K (64 x 16)

DATASHEET

Features

- Low-voltage and Standard-voltage Operation
 - V_{CC} = 1.8V to 5.5V
- User-selectable Internal Organization
 - 1K: 64 x 16
- 3-wire Serial Interface
- 2MHz Clock Rate (5.0V)
- Self-timed Write Cycle (5ms Max)
- High Reliability
 - Endurance: 1,000,000 Write Cycles
 - Data Retention: 100 Years
- 8-lead PDIP, 8-lead JEDEC SOIC, 8-lead, and TSSOP Packages
- Lead-free/Halogen-free Device

Description

The Atmel[®] AT93C46E provides 1,024 bits of Serial Electrically-Erasable Programmable Read-Only Memory (EEPROM) organized as 64 words of 16 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The AT93C46E is available in space-saving 8-lead PDIP, 8-lead JEDEC SOIC, 8-lead, and TSSOP packages.

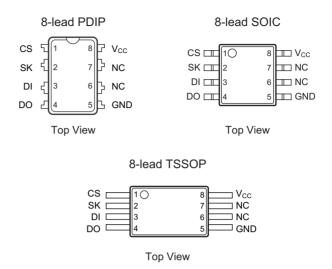
The AT93C46E is enabled through the Chip Select pin (CS) and accessed via a 3-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a Read instruction at DI, the address is decoded and the data is clocked out serially on the data output DO pin. The write cycle is completely self-timed, and no separate erase cycle is required before write. The write cycle is only enabled when the part is in the Erase/Write Enable state. When CS is brought high following the initiation of a write cycle, the DO pin outputs the Ready/Busy status of the part.

The AT93C46E is available from 1.8V to 5.5V.

1. Pin Descriptions and Pinouts

Table 1-1. Pin Configurations

Pin	Function			
CS	Chip Select			
SK	Serial Data Clock			
DI	Serial Data Input			
DO	Serial Data Output			
GND	Ground			
V _{CC}	Power Supply			
NC	No Connect			



Note: Drawings are not to scale.

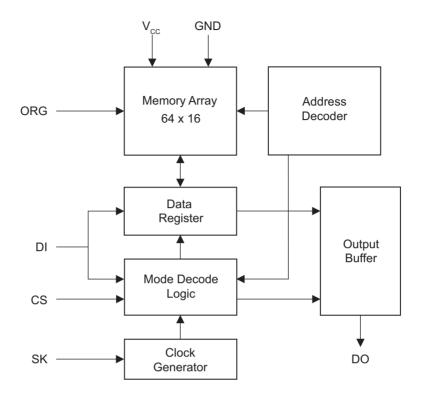
2. Absolute Maximum Ratings*

Operating Temperature55°C to +125°C
Storage Temperature65°C to +150°C
Voltage on Any Pin with Respect to Ground1.0V to +7.0V
Maximum Operating Voltage 6.25V
DC Output Current

*Notice: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3. Block Diagram

Figure 3-1. Block Diagram





Electrical Characteristics 4.

4.1 Pin Capacitance

Table 4-1. Pin Capacitance⁽¹⁾

Applicable over recommended operating range from T_A = 25°C, f = 1.0MHz, V_{CC} = +5.0V (unless otherwise noted).

Symbol	Test Conditions	Max	Units	Conditions
C _{OUT}	Output Capacitance (DO)	5	pF	V _{OUT} = 0V
C _{IN}	Input Capacitance (CS, SK, DI)	5	pF	V _{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

4.2 **DC Characteristics**

Table 4-2. DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Тур	Max	Units
V _{CC1}	Supply Voltage			1.8		5.5	V
V _{CC2}	Supply Voltage			2.7		5.5	V
V _{CC3}	Supply Voltage			4.5		5.5	V
	Supply Current	V _{CC} = 5.0V	Read at 1.0MHz		0.5	2.0	mA
I _{CC}	Supply Current	V _{CC} = 3.0V	Write at 1.0MHz		0.5	2.0	mA
I _{SB1}	Standby Current	V _{CC} = 1.8V	CS = 0V		0.4	1.0	μA
I _{SB2}	Standby Current	V _{CC} = 2.7V			6.0	10.0	μA
I _{SB3}	Standby Current	V _{CC} = 5.0V			10.0	15.0	μA
I _{IL}	Input Leakage	V _{IN} = 0V to V _{CC}			0.1	1.0	μA
I _{OL}	Output Leakage	V _{IN} = 0V to V _{CC}			0.1	1.0	μA
V _{IL1} ⁽¹⁾	Input Low Voltage	$2.7V \le V_{CC} \le 5.5V$		-0.6		0.8	V
V _{IH1} ⁽¹⁾	Input High Voltage	2.7 v ≤ v _{CC} ≤ 5.5 v		2.0		V _{CC} + 1	V
V _{IL2} ⁽¹⁾	Input Low Voltage	$1.8V \le V_{CC} \le 2.7V$		-0.6		V _{CC} x 0.3	V
V _{IH2} ⁽¹⁾	Input High Voltage	1.0V ≤ V _{CC} ≤ 2.7 V		V _{CC} x 0.7		V _{CC} + 1	V
V _{OL1}	Output Low Voltage	2.7V ≤ V _{CC} ≤ 5.5V	I _{OL} = 2.1mA			0.4	V
V _{OH1}	Output High Voltage	2.7 v ≤ v _{CC} ≤ 5.5 v	I _{OH} = -0.4mA	2.4			V
V _{OL2}	Output Low Voltage	1.8V ≤ V _{CC} ≤ 2.7V	I _{OL} = 0.15mA			0.2	V
V _{OH2}	Output High Voltage	1.0 v ≤ v _{CC} ≤ 2.7 v	I _{OH} = -100μA	V _{CC} - 0.2			V

1. V_{IL} min and V_{IH} max are reference only and are not tested. Note:



4.3 AC Characteristics

Table 4-3. AC Characteristics

Applicable over recommended operating range from $T_A = -40^{\circ}\text{C}$ to + 85°C, $V_{CC} = +2.7\text{V}$ to + 5.5V, CL = 1 TTL Gate and 100pF (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Тур	Max	Units	
			$4.5V \le V_{CC} \le 5.5V$	0		2		
f_{SK}	SK Clock Frequency		$2.7V \le V_{CC} \le 5.5V$	0		1	MHz	
			$1.8V \le V_{CC} \le 5.5V$	0		0.25		
			$4.5V \le V_{CC} \le 5.5V$	250				
t _{SKH}	SK High Time		$2.7V \le V_{CC} \le 5.5V$	250			ns	
			$1.8V \le V_{CC} \le 5.5V$	1,000			_	
			$4.5V \le V_{CC} \le 5.5V$	250				
t _{SKL}	SK Low Time		$2.7V \le V_{CC} \le 5.5V$	250			ns	
			$1.8V \le V_{CC} \le 5.5V$	1,000				
			$4.5V \le V_{CC} \le 5.5V$	250				
t _{CS}	Minimum CS Low Time		$2.7V \le V_{CC} \le 5.5V$	250			ns	
	00 2011 111110		$1.8V \le V_{CC} \le 5.5V$	1,000				
			$4.5V \le V_{CC} \le 5.5V$	50				
t_{CSS}	CS Setup Time	Relative to SK	$2.7V \le V_{CC} \le 5.5V$	50			ns	
			$1.8V \le V_{CC} \le 5.5V$	200				
			$4.5V \le V_{CC} \le 5.5V$	100				
t _{DIS}	DI Setup Time	Relative to SK	$2.7V \le V_{CC} \le 5.5V$	100			ns	
			$1.8V \le V_{CC} \le 5.5V$	400				
t _{CSH}	CS Hold Time	Relative to SK		0			ns	
			$4.5 \text{V} \leq \text{V}_{\text{CC}} \leq 5.5 \text{V}$	100				
t _{DIH}	DI Hold Time	Relative to SK	$2.7 \text{V} \leq \text{V}_{\text{CC}} \leq 5.5 \text{V}$	100			ns	
			$1.8V \le V_{CC} \le 5.5V$	400				
			$4.5V \le V_{CC} \le 5.5V$			250		
t _{PD1}	Output Delay to "1"	AC Test	$2.7V \le V_{CC} \le 5.5V$			250	ns	
			$1.8V \le V_{CC} \le 5.5V$			1,000		
			$4.5V \le V_{CC} \le 5.5V$			250		
t _{PD0}	Output Delay to "0"	AC Test	$2.7 \text{V} \leq \text{V}_{\text{CC}} \leq 5.5 \text{V}$			250	ns	
			$1.8V \le V_{CC} \le 5.5V$			1,000		
			$4.5V \leq V_{CC} \leq 5.5V$			250		
t_{SV}	CS to Status Valid	AC Test	$2.7V \le V_{CC} \le 5.5V$			250	ns	
			$1.8V \le V_{CC} \le 5.5V$			1,000		
	004 001 111 1		$4.5V \le V_{CC} \le 5.5V$			100		
t _{DF}	CS to DO in High Impedance	AC Test CS = V _{IL}	$2.7V \le V_{CC} \le 5.5V$			150	ns	
	poddiioo		$1.8V \le V_{CC} \le 5.5V$			400		
t _{WP}	Write Cycle Time			0.10	3	5	ms	
Endurance ⁽¹⁾	5.0V, 25°C			1M			Write Cycle	

Note: 1. This parameter is ensured by characterization.



5. Functional Description

The AT93C46E is accessed via a simple and versatile three-wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. A valid instruction starts with a rising edge of CS and consists of a Start condition (Logic 1) followed by the appropriate opcode and the desired memory address location.

Table 5-1. Instruction Set

			Address	
Instruction	SB	Opcode	x16	Comments
READ	1	10	$A_5 - A_0$	Reads data stored in memory, at specified address.
EWEN	1	00	11XXXX	Write enable must precede all programming modes.
ERASE	1	11	$A_5 - A_0$	Erase memory location $A_n - A_0$.
WRITE	1	01	$A_5 - A_0$	Writes memory location $A_n - A_0$.
ERAL	1	00	10XXXX	Erases all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
WRAL	1	00	01XXXX	Writes all memory locations. Valid only at $V_{\rm CC}$ = 4.5V to 5.5V.
EWDS	1	00	00XXXX	Disables all programming instructions.

READ: The READ instruction contains the address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the Serial Output (DO) pin. Output data changes are synchronized with the rising edges of Serial Clock (SK).

Note: It should be noted that a dummy bit (Logic 0) precedes the 16-bit data output string.

ERASE/WRITE ENABLE (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out.

Note: Once in the EWEN state, programming remains enabled until an EWDS instruction is executed or V_{CC} power is removed from the device.

ERASE: The ERASE instruction programs all bits in the specified memory location to the Logic 1 state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the Ready/Busy status of the device if CS is brought high after being kept low for a minimum of 250ns (t_{CS}). A Logic 1 at pin DO indicates that the selected memory location has been erased and the part is ready for another instruction.

WRITE: The WRITE instruction contains the 16 bits of data to be written into the specified memory location. The self-timed programming cycle, t_{WP} , starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250ns (t_{CS}). A Logic 0 at DO indicates that programming is still in progress. A Logic 1 indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions. A Ready/Busy status cannot be obtained if the CS is brought high after the end of the self-timed programming cycle, t_{WP} .

ERASE ALL (ERAL): The Erase All (ERAL) instruction programs every bit in the memory array to the Logic 1 state and is primarily used for testing purposes. The DO pin outputs the ready/busy status of the part if CS is brought high after being kept low for a minimum of 250ns (t_{CS}). The ERAL instruction is valid only at V_{CC} = 5.0V \pm 10%.

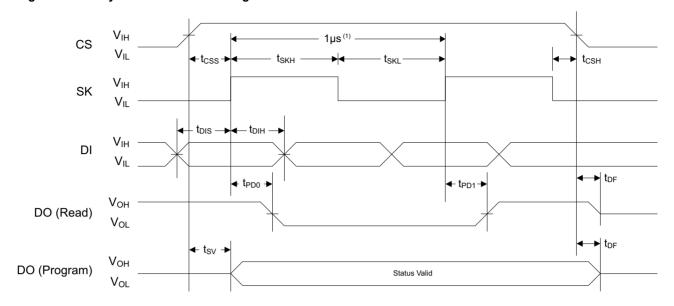
WRITE ALL (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250ns (t_{CS}). The WRAL instruction is valid only at V_{CC} = 5.0V \pm 10%.

Erase/Write Disable (EWDS): To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the Read instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.



6. Timing Diagrams

Figure 6-1. Synchronous Data Timing



Note: 1. This is the minimum SK period.

Table 6-1. Organization Key for Timing Diagrams

I/O	x16
A _N	A ₅
D_N	D ₁₅



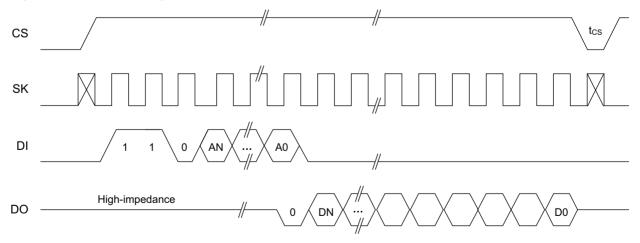
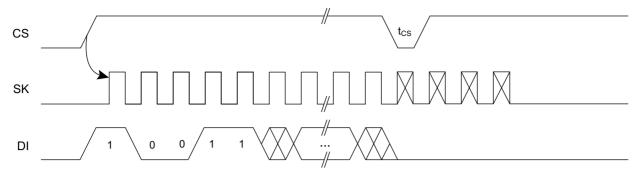


Figure 6-3. EWEN Timing⁽¹⁾



Note: 1. Requires a minimum of nine clock cycles.

Figure 6-4. ERASE Timing

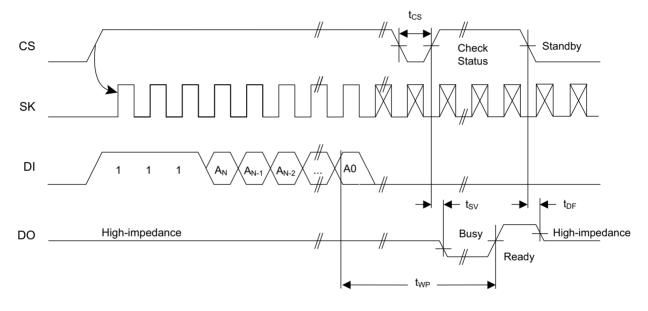


Figure 6-5. Write Timing

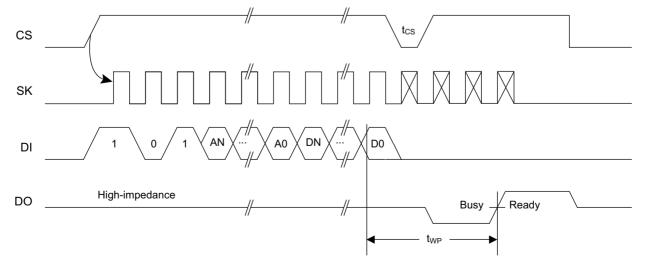
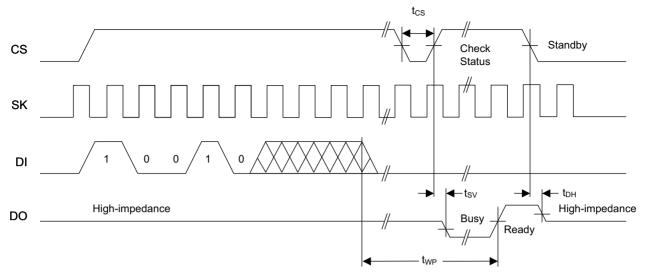


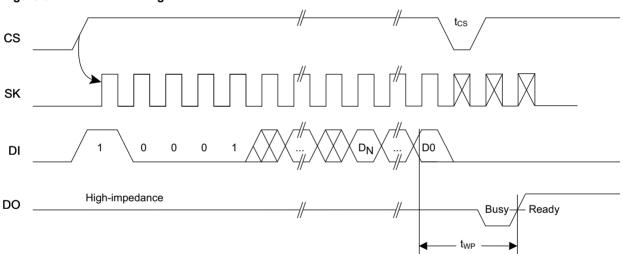


Figure 6-6. ERAL Timing⁽¹⁾



Note: 1. Valid only at $V_{CC} = 4.5V$ to 5.5V.

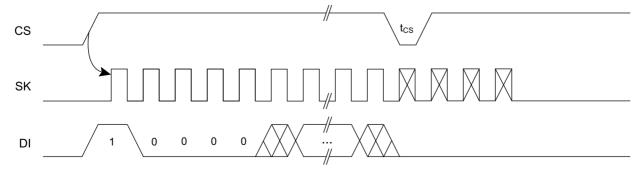
Figure 6-7. WRAL Timing^{(1) (2)}



Notes: 1. Valid only at $V_{CC} = 4.5V$ to 5.5V.

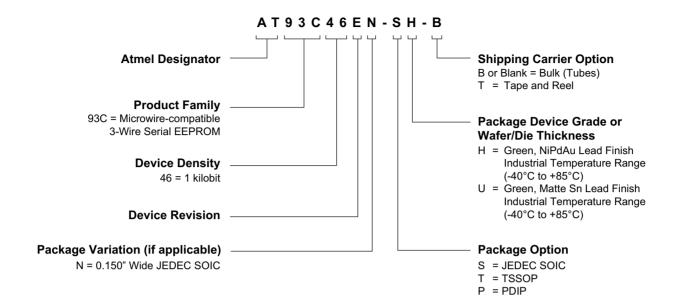
2. Requires a minimum of nine clock cycles.

Figure 6-8. EWDS Timing⁽¹⁾



Note: 1. Requires a minimum of nine clock cycles.

7. Ordering Code Detail





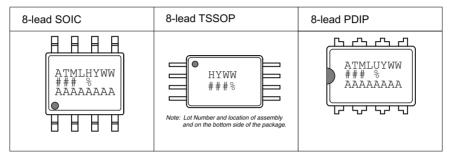
8. Ordering Information

			Delivery Ir	nformation	Operation
Atmel Ordering Code	Lead Finish	Package	Form	Quantity	Range
AT93C46EN-SH-B		8S1	Bulk (Tubes)	100 per Tube	
AT93C46EN-SH-T	NiPdAu	031	Tape and Reel	4,000 per Reel	
AT93C46E-TH-B	(Lead-free/Halogen-free)	8X	Bulk (Tubes)	100 per Tube	Industrial Temperature (-40°C to 85°C)
AT93C46E-TH-T		0.7	Tape and Reel	5,000 per Reel	(10 0 10 00 0)
AT93C46E-PU	Matte Tin (Lead-free/Halogen-free)	8P3	Bulk (Tubes)	50 per Tube	

	Package Type
8S1	8-lead, 0.150" wide, Plastic Gull Wing, Small Outline (JEDEC SOIC)
8X	8-lead, 0.170" wide, Thin Shrink Small Outline Package (TSSOP)
8P3	8-lead, 0.300" wide body, Plastic Dual In-line Package (PDIP)

9. Part Markings

AT93C46E: Package Marking Information



Note 1: designates pin 1

Note 2: Package drawings are not to scale

Catalog Number Truncation							
AT93C46E Truncation Code ###: 46E							
Date Code	es				Voltage	s	
Y = Year		M = Month		WW = Work Week of Assembly	% =	= Minimum Voltage	
4: 2014 5: 2015 6: 2016 7: 2017	8: 2018 9: 2019 0: 2020 1: 2021	A: January B: Februar L: Decemb	y	02: Week 2 04: Week 4 52: Week 52	1:	1.8V min	
Country o	f Assembly	•	Lot Nu	mber	Grade/L	ead Finish Material	
@ = Country of Assembly		AAA/	A = Atmel Wafer Lot Number	U: H:	Industrial/Matte Tin/SnAgCu Industrial/NiPdAu		
Trace Code				Atmel T	runcation		
XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB YZ, ZZ			AT: ATM: ATML:	7 1111101			

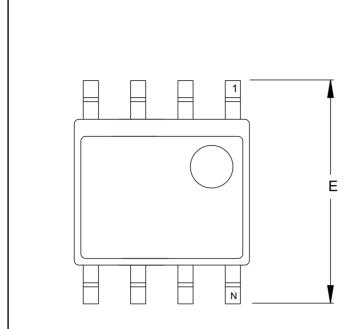
3/13/14

Atmel	TITLE	DRAWING NO.	REV.	
Package Mark Contact: DL-CSO-Assy_eng@atmel.com	93C46ESM, AT93C46E Package Marking Information	93C46ESM	А	

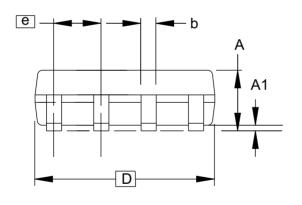


10. Packaging Information

10.1 8S1 — 8-lead JEDEC SOIC



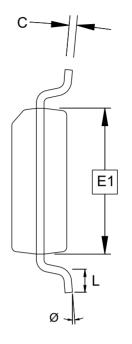
TOP VIEW



SIDE VIEW

Notes: This drawing is for general information only.

Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.



END VIEW

COMMON DIMENSIONS (Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
А	1.35	_	1.75	
A1	0.10	_	0.25	
b	0.31	_	0.51	
С	0.17	_	0.25	
D	4.80	_	5.05	
E1	3.81	_	3.99	
E	5.79	_	6.20	
е		1.27 BSC	,	
L	0.40	_	1.27	
Ø	0°	_	8°	

6/22/11

Atmel

Package Drawing Contact: packagedrawings@atmel.com

TITLE

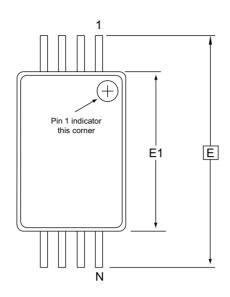
8S1, 8-lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)

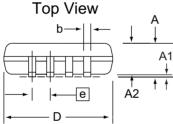
GPC SWB

C DRAWING NO. 8S1

REV.

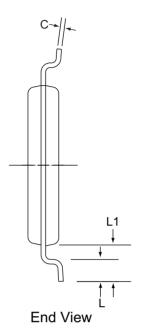
10.2 8X — 8-lead TSSOP





Side View

- Notes: 1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
 - 2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
 - 3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
 - 4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
 - 5. Dimension D and E1 to be determined at Datum Plane H.



COMMON DIMENSIONS (Unit of Measure = mm)

1IN -	NOM -	MAX 1.20	NOTE
-	-	1 20	
٥.		1.20	
05	-	0.15	
80	1.00	1.05	
90	3.00	3.10	2, 5
6.40 BSC			
30	4.40	4.50	3, 5
19	0.25	0.30	4
0.65 BSC			
45	0.60	0.75	
	1.00 REF		
09	-	0.20	
	05 80 90 30 19 45	80 1.00 90 3.00 6.40 BSC 30 4.40 19 0.25 0.65 BSC 45 0.60 1.00 REF	80 1.00 1.05 90 3.00 3.10 6.40 BSC 30 4.40 4.50 19 0.25 0.30 0.65 BSC 45 0.60 0.75 1.00 REF

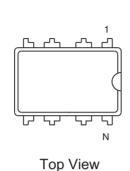
2/27/14

Atmel

Package Drawing Contact: packagedrawings@atmel.com TITLE 8X, 8-lead 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP) GPC DRAWING NO. REV. **TNR** 8X Ε

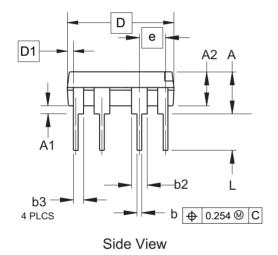


10.3 8P3 — 8-lead PDIP



Ε .381 eА

End View



COMMON DIMENSIONS (Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
Α	-	-	5.334	2
A1	0.381	-	-	
A2	2.921	3.302	4.953	
b	0.356	0.457	0.559	5
b2	1.143	1.524	1.778	6
b3	0.762	0.991	1.143	6
С	0.203	0.254	0.356	
D	9.017	9.271	10.160	3
D1	0.127	0.000	0.000	3
E	7.620	7.874	8.255	4
E1	6.096	6.350	7.112	3
е	2.540 BSC			
eA	7.620 BSC			4
L	2.921	3.302	3.810	2

Notes:

- 1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
- 2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
 3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
 4. E and eA measured with the leads constrained to be perpendicular to datum.
- 5. Pointed or rounded lead tips are preferred to ease insertion.
- 6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

07/31/14

Atmel	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	8P3, 8-lead, 0.300" Wide Body, Plastic Dual In-line Package (PDIP)	PTC	8P3	E

11. Revision History

Doc. Rev.	Date	Comments
5207F	01/2015	Updated ordering information section.
5207E	10/2014	Added the part markings and ordering code detail. Updated the package outline drawings and the 8A2 to 8X. Updated the template, Atmel logos, and the disclaimer page.
5207D	01/2008	Removed 'preliminary' status
5207C	11/2007	Modified 'max' value on AC Characteristics table
5207B	08/2007	Modified Part Marking Scheme Tables
5207A	01/2007	Initial document release













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