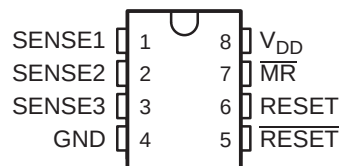


TRIPLE PROCESSOR SUPERVISORS

FEATURES

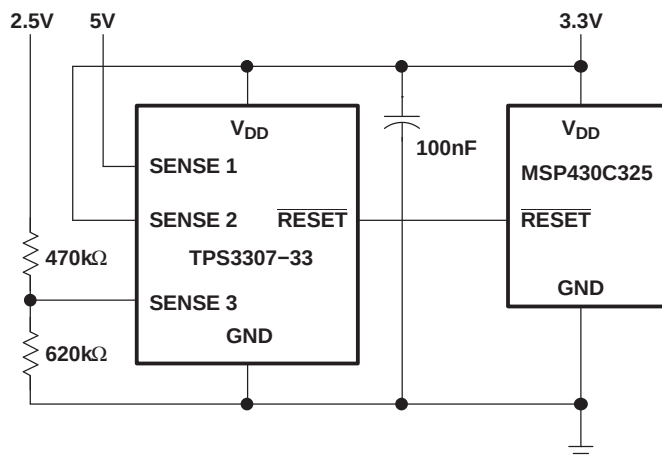
- Triple Supervisory Circuits for DSP and Processor-Based Systems
- Power-On Reset Generator With Fixed Delay Time of 200ms, No External Capacitor Needed
- Temperature-Compensated Voltage Reference
- Maximum Supply Current of 40µA
- Supply Voltage Range: 2V to 6V
- Defined $\overline{\text{RESET}}$ Output From $V_{\text{DD}} \geq 1.1\text{V}$
- MSOP-8 and SO-8 Packages
- Temperature Range : -40°C to $+85^{\circ}\text{C}$

D OR DGN PACKAGE
(TOP VIEW)



TYPICAL APPLICATIONS

Figure 1 lists some of the typical applications for the TPS3307 family, and a schematic diagram for a processor-based system application. This application uses TI part numbers [TPS3307-33](#) and [MSP430C325](#).



- Applications using DSPs, Microcontrollers or Microprocessors
- Industrial Equipment
- Programmable Controls
- Automotive Systems
- Portable/Battery Powered Equipment
- Intelligent Instruments
- Wireless Communication Systems
- Notebook/Desktop Computers

Figure 1. Applications Using the TPS3307 Family

DESCRIPTION

The TPS3307 family is a series of micropower supply voltage supervisors designed for circuit initialization primarily in DSP and processor-based systems, which require more than one supply voltage.

The product spectrum of the TPS3307-xx is designed for monitoring three independent supply voltages: 3.3V/1.8V/adj, 3.3V/2.5V/adj or 3.3V/5V/adj. The adjustable SENSE input allows the monitoring of any supply voltage $>1.25\text{V}$.

The various supply voltage supervisors are designed to monitor the nominal supply voltage as shown in the following [supply voltage monitoring table](#).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

During power-on, $\overline{\text{RESET}}$ is asserted when the supply voltage V_{DD} becomes higher than 1.1V. Thereafter, the supply voltage supervisor monitors the SENSE_n inputs and keeps $\overline{\text{RESET}}$ active as long as SENSE_n remain below the threshold voltage V_{IT+} .

An internal timer delays the return of the $\overline{\text{RESET}}$ output to the inactive state (high) to ensure proper system reset. The delay time, $t_{d(\text{typ})} = 200\text{ms}$, starts after all SENSE_n inputs have risen above the threshold voltage V_{IT+} . When the voltage at any SENSE input drops below the threshold voltage V_{IT-} , the $\overline{\text{RESET}}$ output becomes active (low) again.

The TPS3307-xx family of devices incorporates a manual reset input, $\overline{\text{MR}}$. A low level at $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to become active. In addition to the active-low $\overline{\text{RESET}}$ output, the TPS3307-xx family includes an active-high RESET output.

The devices are available in either 8-pin MSOP or standard 8-pin SO packages.

The TPS3307-xx devices are characterized for operation over a temperature range of -40°C to $+85^{\circ}\text{C}$.

SUPPLY VOLTAGE MONITORING

DEVICE	NOMINAL SUPERVISED VOLTAGE			THRESHOLD VOLTAGE (TYP)		
	SENSE1	SENSE2	SENSE3	SENSE1	SENSE2	SENSE3
TPS3307-18	3.3V	1.8V	User defined	2.93V	1.68V	1.25V ⁽¹⁾
TPS3307-25	3.3V	2.5V	User defined	2.93V	2.25V	1.25V ⁽¹⁾
TPS3307-33	5V	3.3V	User defined	4.55V	2.93V	1.25V ⁽¹⁾

(1) The actual sense voltage has to be adjusted by an external resistor divider according to the application requirements.

AVAILABLE OPTIONS⁽¹⁾

T_A	PACKAGED DEVICES		MARKING DGN PACKAGE	CHIP FORM (Y)
	SMALL OUTLINE (D)	PowerPAD™ μ-SMALL OUTLINE (DGN)		
-40°C to $+85^{\circ}\text{C}$	TPS3307-18D	TPS3307-18DGN	TIAAP	TPS3307-18Y
	TPS3307-25D	TPS3307-25DGN	TIAAQ	TPS3307-25Y
	TPS3307-33D	TPS3307-33DGN	TIAAR	TPS3307-33Y

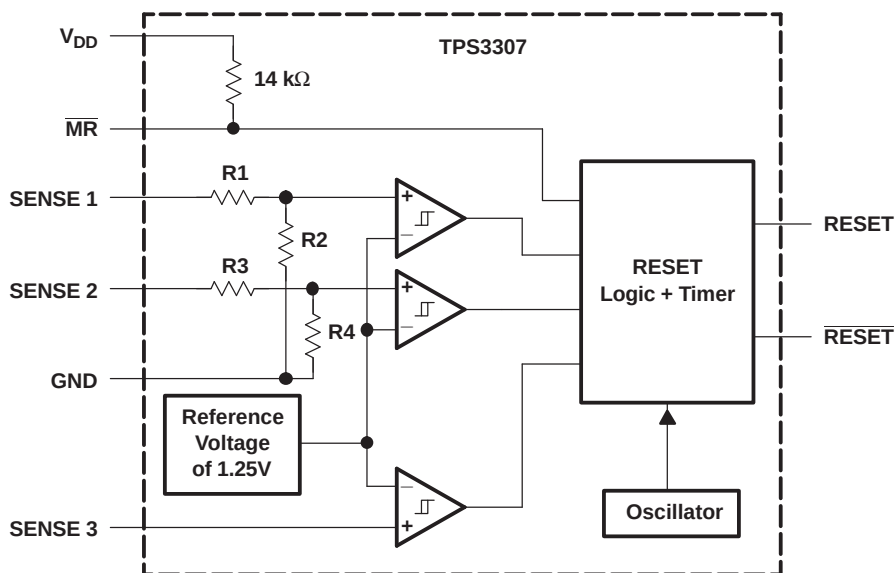
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

Function/Truth Tables

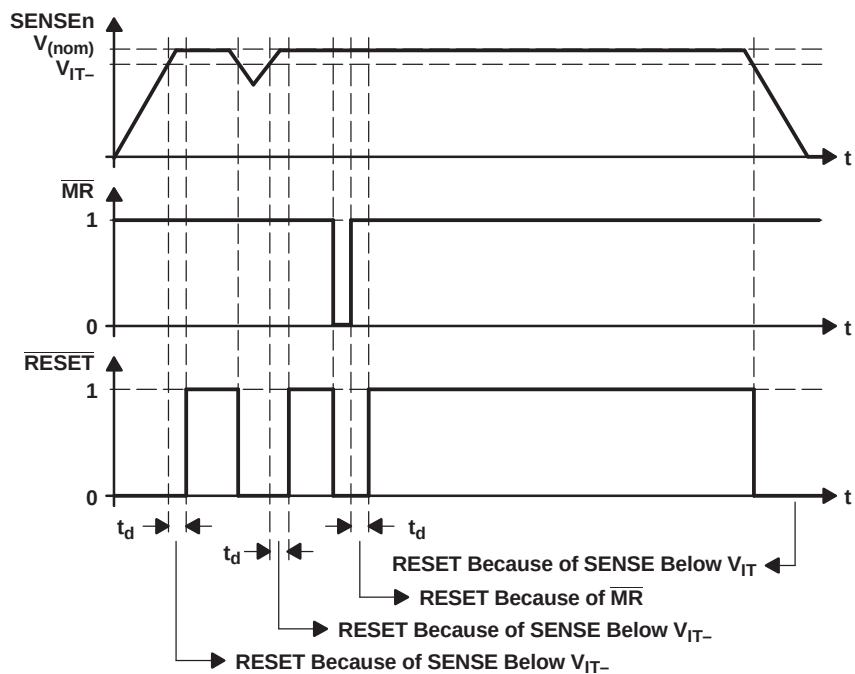
$\overline{\text{MR}}$	$\text{SENSE1} > V_{IT1}$	$\text{SENSE2} > V_{IT2}$	$\text{SENSE3} > V_{IT3}$	$\overline{\text{RESET}}$	RESET
L	X ⁽¹⁾	X ⁽¹⁾	X	L	H
H	0	0	0	L	H
H	0	0	1	L	H
H	0	1	0	L	H
H	0	1	1	L	H
H	1	0	0	L	H
H	1	0	1	L	H
H	1	1	0	L	H
H	1	1	1	H	L

(1) X = Don't care

Functional Block Diagram



Timing Diagram



TPS3307Y Chip Information

These chips, when properly assembled, display characteristics similar to those of the TPS3307. Thermal compression or ultrasonic bonding may take place on the doped aluminium bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

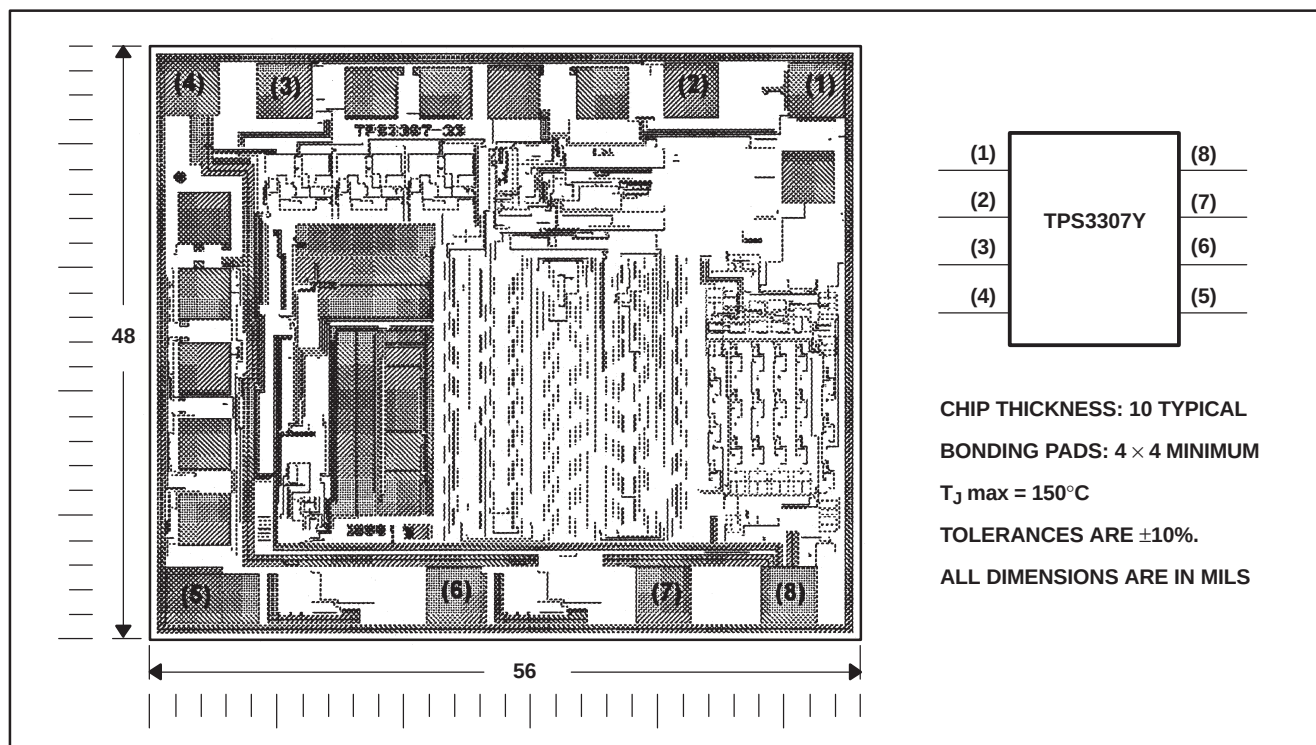


Table 2. Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
GND	4		Ground
$\overline{\text{MR}}$	7	I	Manual reset
$\overline{\text{RESET}}$	5	O	Active-low reset output
RESET	6	O	Active-high reset output
SENSE1	1	I	Sense voltage input 1
SENSE2	2	I	Sense voltage input 2
SENSE3	3	I	Sense voltage input 3
V_{DD}	8		Supply voltage

Absolute Maximum Ratings⁽¹⁾

Over operating free-air temperature range (unless otherwise noted).

	UNIT
Supply voltage, V_{DD} ⁽²⁾	7V
$\overline{MR}$ pin	-0.3V to V_{DD} +0.3V
All other pins ⁽²⁾	-0.3V to 7V
Maximum low output current, I_{OL}	5mA
Maximum high output current, I_{OH}	-5mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$)	±20mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)	±20mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	-40°C to +85°C
Storage temperature range, T_{stg}	-65°C to +150°C
Soldering temperature	+260°C

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND. For reliable operation the device must not be operated at 7V for more than $t = 1000h$ continuously.

Dissipation Rating Table

PACKAGE	$T_A \leq +25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = +25^\circ\text{C}$	$T_A = +70^\circ\text{C}$ POWER RATING	$T_A = +85^\circ\text{C}$ POWER RATING
DGN	2.14W	17.1mW/°C	1.37W	1.11W
D	725mW	5.8mW/°C	464mW	377mW

Recommended Operating Conditions

At specified temperature range.

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2	6	V
Input voltage at $\overline{MR}$ and SENSE3, V_I	0	$V_{DD} + 0.3$	V
Input voltage at SENSE1 and SENSE2, V_I	0	$(V_{DD}+0.3)V_{IT}/1.25V$	V
High-level input voltage at $\overline{MR}$, V_{IH}	$0.7 \times V_{DD}$		V
Low-level input voltage at $\overline{MR}$, V_{IL}		$0.3 \times V_{DD}$	V
Input transition rise and fall rate at $\overline{MR}$, $\Delta t/\Delta V$		50	ns/V
Operating free-air temperature range, T_A	-40	+85	°C

Electrical Characteristics

Over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OH}	High-level output voltage		V _{DD} = 2V to 6V, I _{OH} = −20 μA	V _{DD} − 0.2V			V
			V _{DD} = 3.3V, I _{OH} = −2mA	V _{DD} − 0.4V			
			V _{DD} = 6V, I _{OH} = −3mA	V _{DD} − 0.4V			
V _{OL}	Low-level output voltage		V _{DD} = 2V to 6V, I _{OL} = 20μA			0.2	V
			V _{DD} = 3.3V, I _{OL} = 2mA			0.4	
			V _{DD} = 6V, I _{OL} = 3mA			0.4	
Power-up reset voltage ⁽¹⁾			V _{DD} ≥ 1.1V, I _{OL} = 20μA			0.4	V
V _{IT−}	Negative-going input threshold voltage ⁽²⁾		V _{DD} = 2V to 6V, T _A = 0°C to +85°C	1.22	1.25	1.28	V
				1.64	1.68	1.72	
				2.20	2.25	2.30	
				2.86	2.93	3	
				4.46	4.55	4.64	
			V _{DD} = 2V to 6V, T _A = −40°C to +85°C	1.22	1.25	1.29	V
				1.64	1.68	1.73	V
				2.20	2.25	2.32	
				2.86	2.93	3.02	
				4.46	4.55	4.67	
V _{hys}	Hysteresis at VSENSEn input		V _{IT−} = 1.25V		10	mV	
			V _{IT−} = 1.68V		15		
			V _{IT−} = 2.25V		20		
			V _{IT−} = 2.93V		30		
			V _{IT−} = 4.55V		40		
I _H	High-level input current		$\overline{MR}$	$\overline{MR} = 0.7 \times V_{DD}$, V _{DD} = 6V	−130	−180	μA
			SENSE1	VSENSE1 = V _{DD} = 6V	5	8	
			SENSE2	VSENSE2 = V _{DD} = 6V	6	9	
			SENSE3	VSENSE3 = V _{DD}	−25	25	nA
I _L	Low-level input current		$\overline{MR}$	$\overline{MR} = 0V$, V _{DD} = 6V	−430	−600	μA
			SENSEn	VSENSE1,2,3 = 0V	−25	25	nA
I _{DD}	Supply current					40	μA
C _i	Input capacitance		V _I = 0V to V _{DD}		10		pF

(1) The lowest supply voltage at which $\overline{RESET}$ becomes active. $t_r, V_{DD} \geq 15\mu s/V$

(2) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic 0.1 μF) should be placed close to the supply terminals.

Timing Requirements

At $V_{DD} = 2V$ to $6V$, $R_L = 1M\Omega$, $C_L = 50pF$, $T_A = +25^\circ C$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width	SENSEn	$V_{SENSEnL} = V_{IT-} - 0.2V$, $V_{SENSEnH} = V_{IT+} + 0.2V$			μs
		$\overline{MR}$	$V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.3 \times V_{DD}$			ns

Switching Characteristics

At $V_{DD} = 2V$ to $6V$, $R_L = 1M\Omega$, $C_L = 50pF$, $T_A = +25^\circ C$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Delay time	$V_{I(SENSEn)} \geq V_{IT+} + 0.2V$, $\overline{MR} \geq 0.7 \times V_{DD}$. See Timing Diagram .	140	200	280	ms
t_{PHL}	Propagation (delay) time, high-to-low level output	$\overline{MR}$ to $\overline{RESETMR}$ to RESET		200	500	ns
t_{PLH}	Propagation (delay) time, low-to-high level output	$\overline{MR}$ to $\overline{RESETMR}$ to RESET				
t_{PHL}	Propagation (delay) time, high-to-low level output	SENSEn to $\overline{RESET}$ SENSEn to RESET		1	5	μs
t_{PLH}	Propagation (delay) time, low-to-high level output	SENSEn to $\overline{RESET}$ SENSEn to RESET				

Typical Characteristics

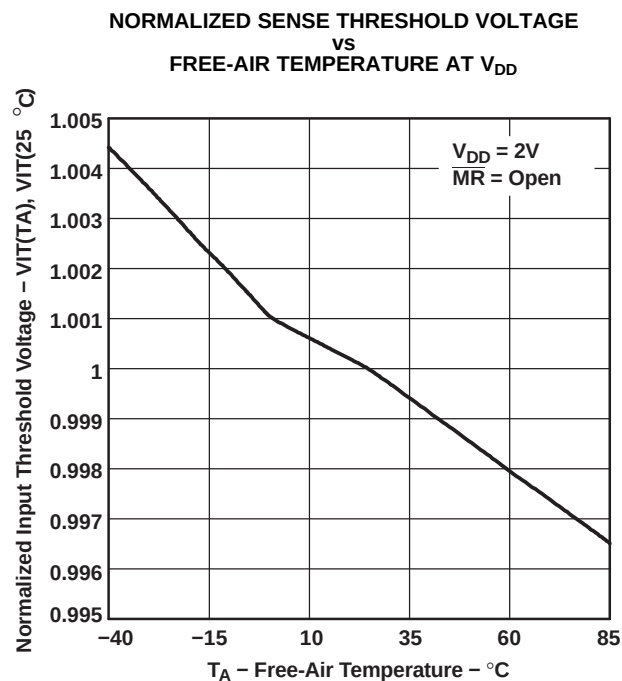


Figure 2.

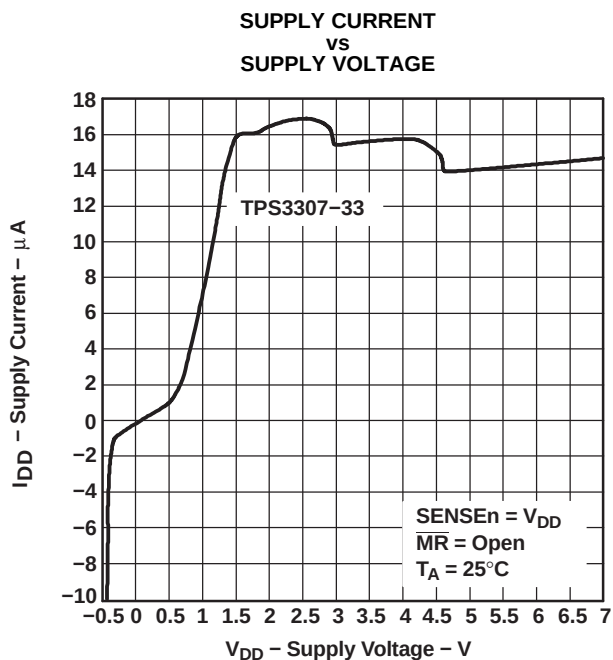


Figure 3.

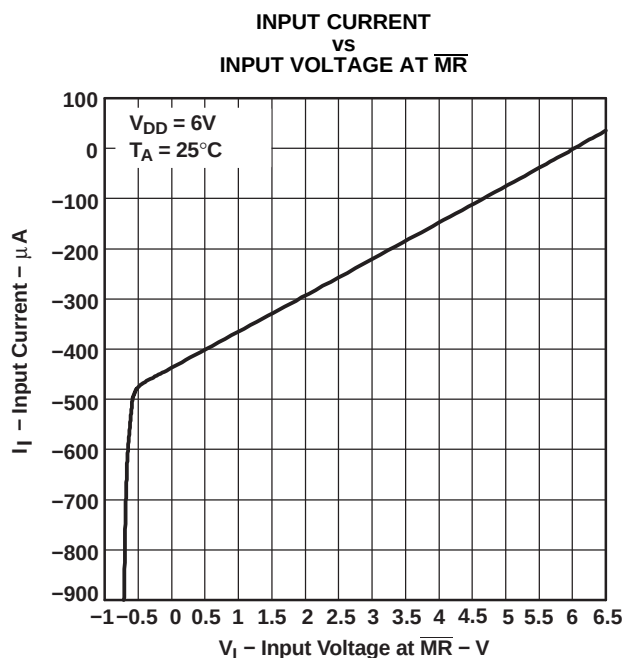


Figure 4.

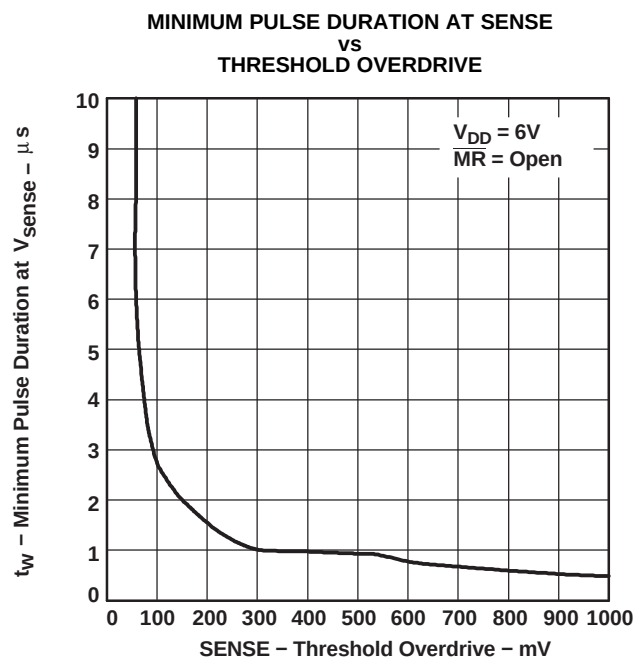


Figure 5.

Typical Characteristics (continued)

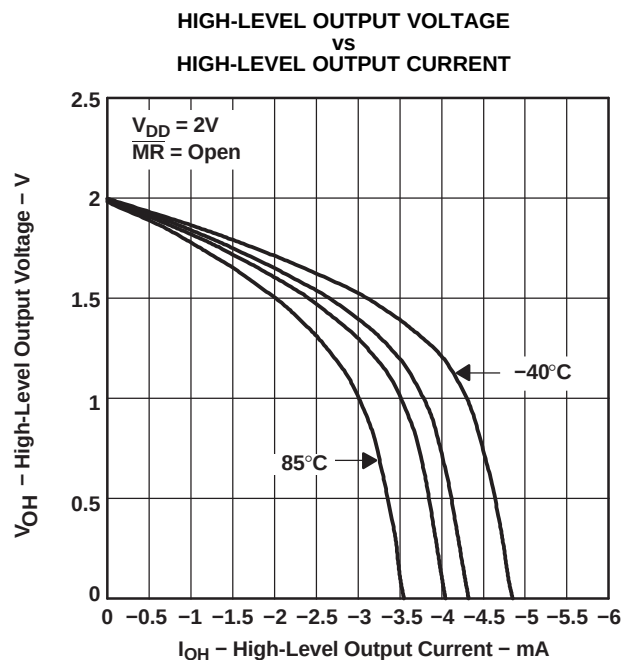


Figure 6.

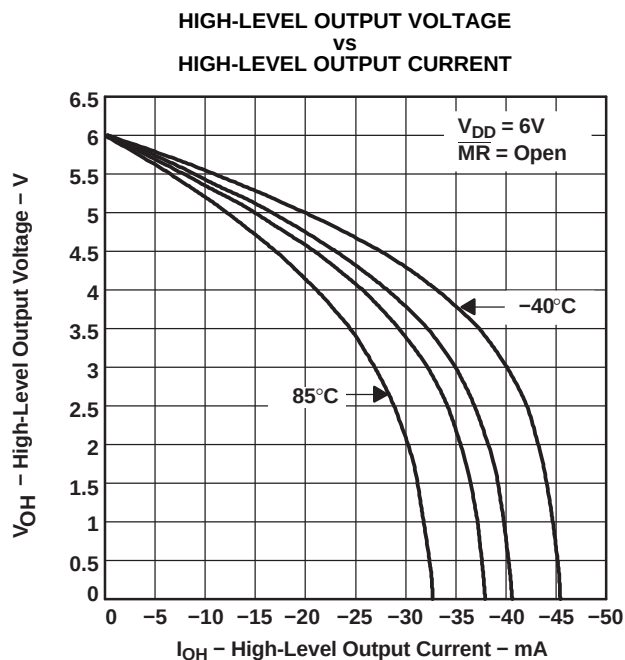


Figure 7.

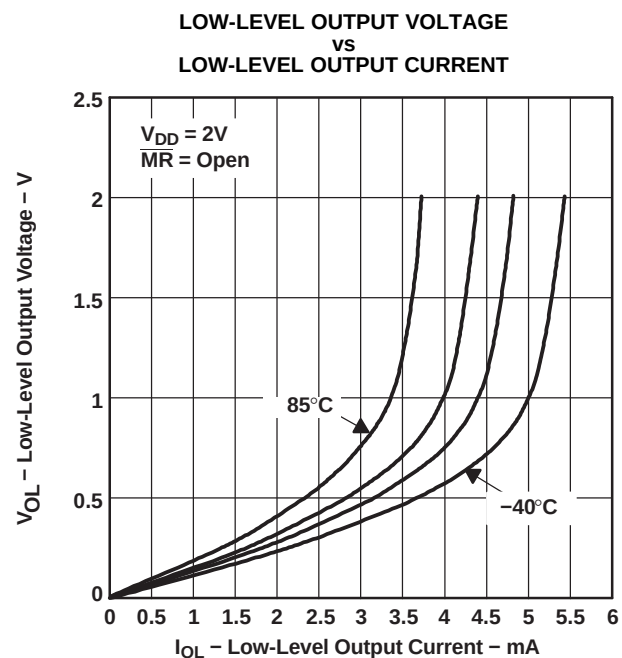


Figure 8.

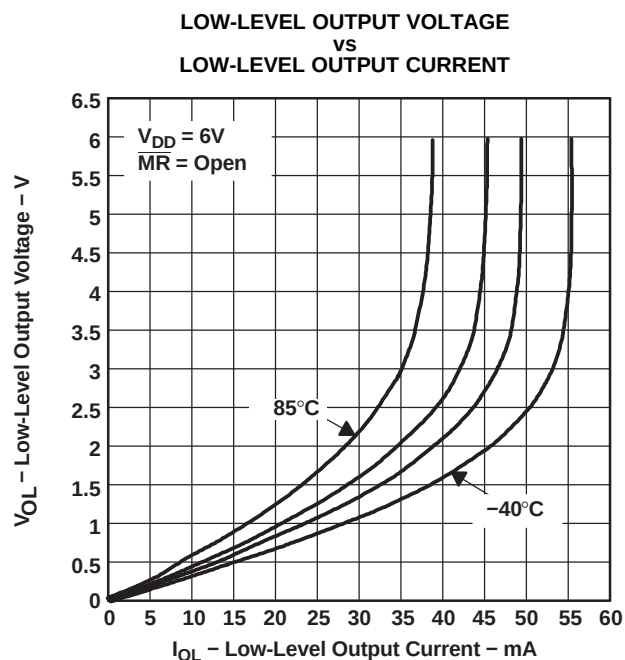


Figure 9.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3307-18D	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30718
TPS3307-18D.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30718
TPS3307-18DGN	Active	Production	HVSSOP (DGN) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAP
TPS3307-18DGN.A	Active	Production	HVSSOP (DGN) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAP
TPS3307-18DGNR	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAP
TPS3307-18DGNR.A	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAP
TPS3307-18DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30718
TPS3307-18DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30718
TPS3307-25D	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30725
TPS3307-25D.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30725
TPS3307-25DGN	Active	Production	HVSSOP (DGN) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAQ
TPS3307-25DGN.A	Active	Production	HVSSOP (DGN) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAQ
TPS3307-25DGNR	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAQ
TPS3307-25DGNR.A	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAQ
TPS3307-25DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30725
TPS3307-25DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30725
TPS3307-33D	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30733
TPS3307-33D.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30733
TPS3307-33DGN	Active	Production	HVSSOP (DGN) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAR
TPS3307-33DGN.A	Active	Production	HVSSOP (DGN) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAR
TPS3307-33DGNR	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAR
TPS3307-33DGNR.A	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAR
TPS3307-33DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30733
TPS3307-33DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30733

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS3307 :

- Enhanced Product : [TPS3307-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

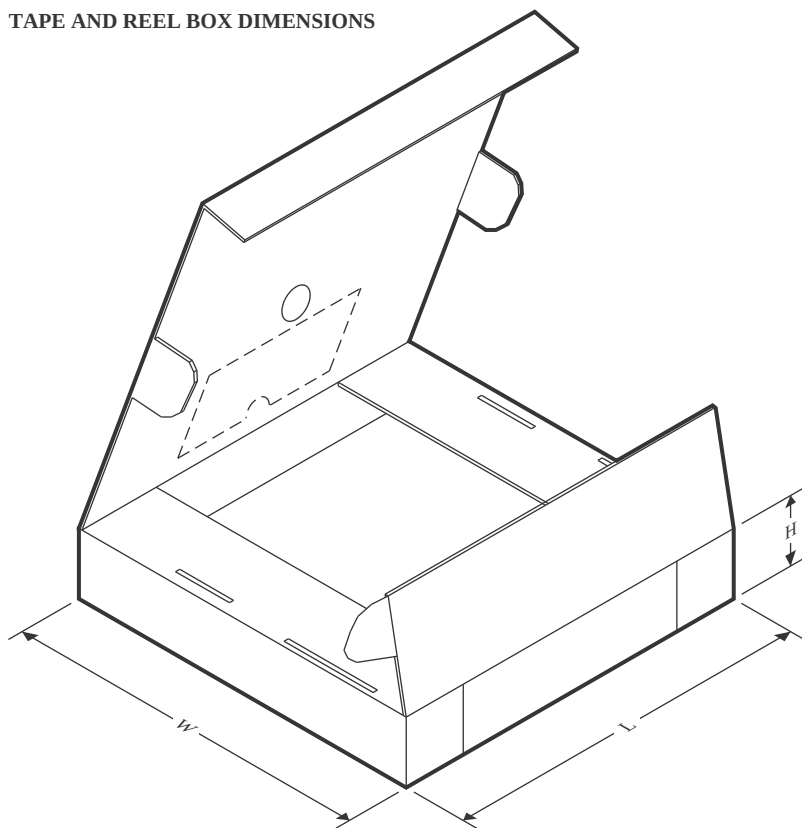
TAPE AND REEL INFORMATION



*All dimensions are nominal

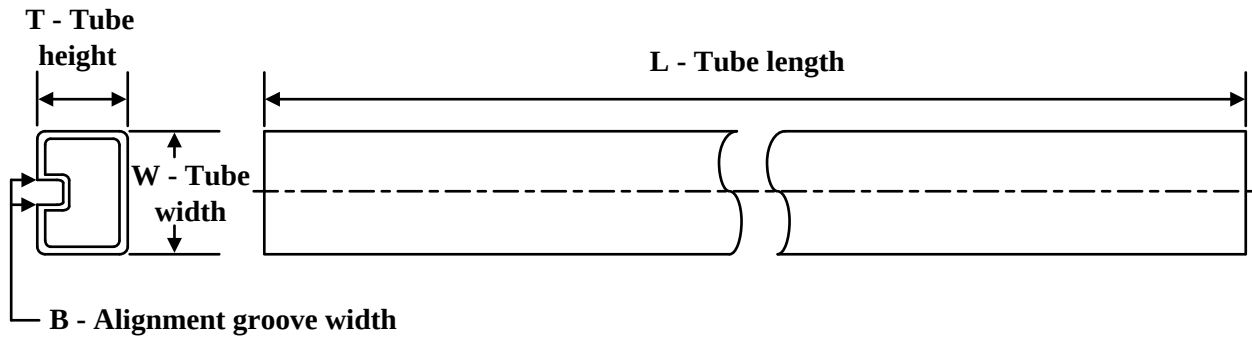
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3307-18DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3307-18DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3307-25DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3307-25DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3307-33DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3307-33DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3307-18DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
TPS3307-18DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS3307-25DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
TPS3307-25DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS3307-33DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
TPS3307-33DR	SOIC	D	8	2500	350.0	350.0	43.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TPS3307-18D	D	SOIC	8	75	505.46	6.76	3810	4
TPS3307-18D.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS3307-25D	D	SOIC	8	75	505.46	6.76	3810	4
TPS3307-25D.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS3307-33D	D	SOIC	8	75	505.46	6.76	3810	4
TPS3307-33D.A	D	SOIC	8	75	505.46	6.76	3810	4

GENERIC PACKAGE VIEW

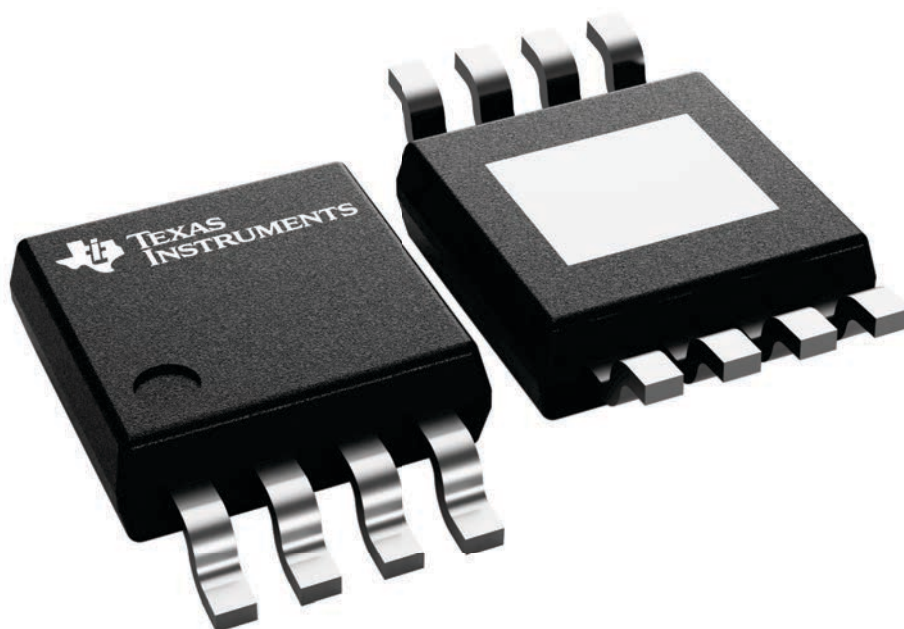
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

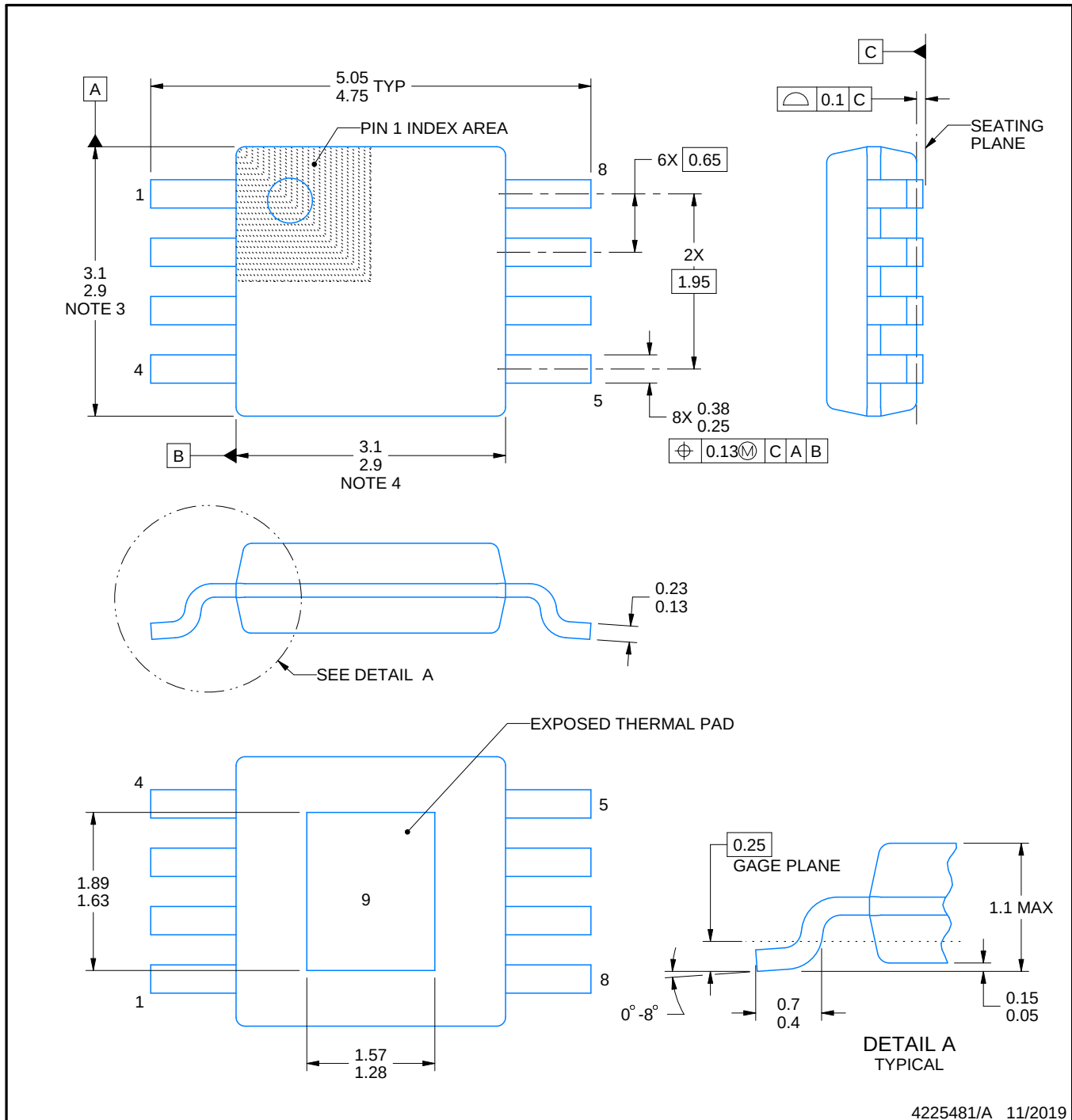
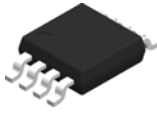
3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/B



4225481/A 11/2019

NOTES:

PowerPAD is a trademark of Texas Instruments.

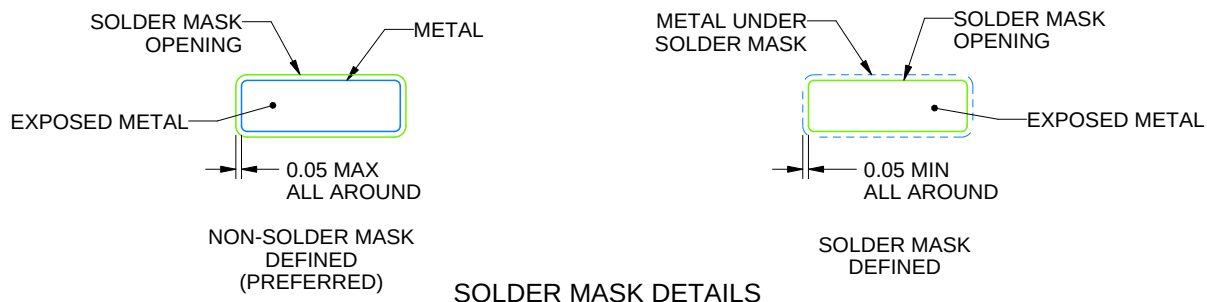
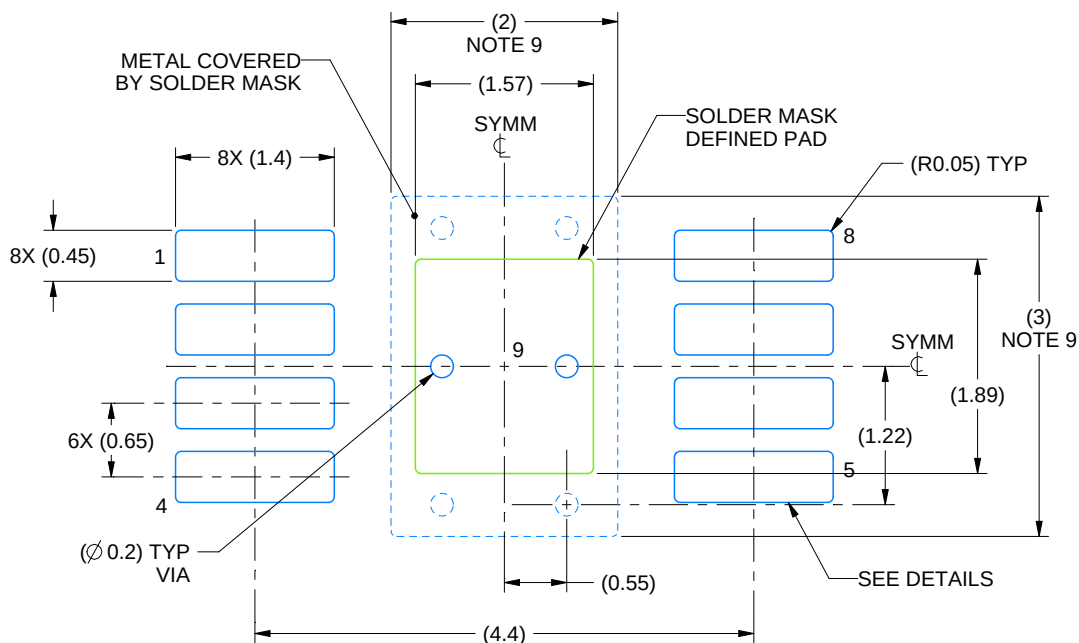
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGN0008D

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4225481/A 11/2019

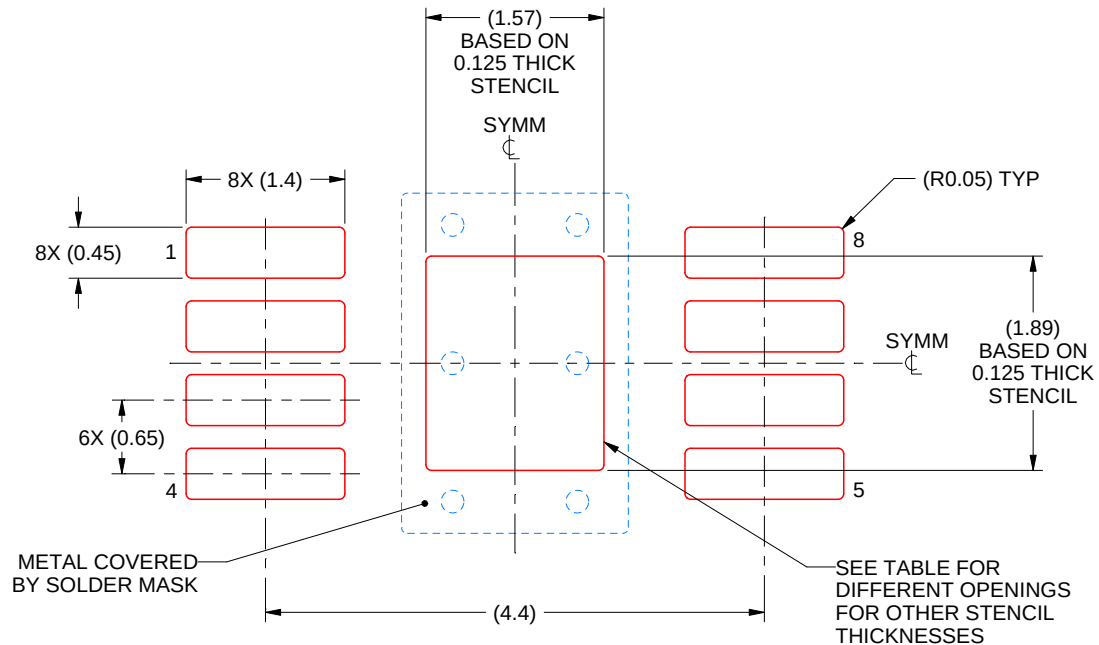
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

DGN0008D

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE

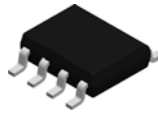
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

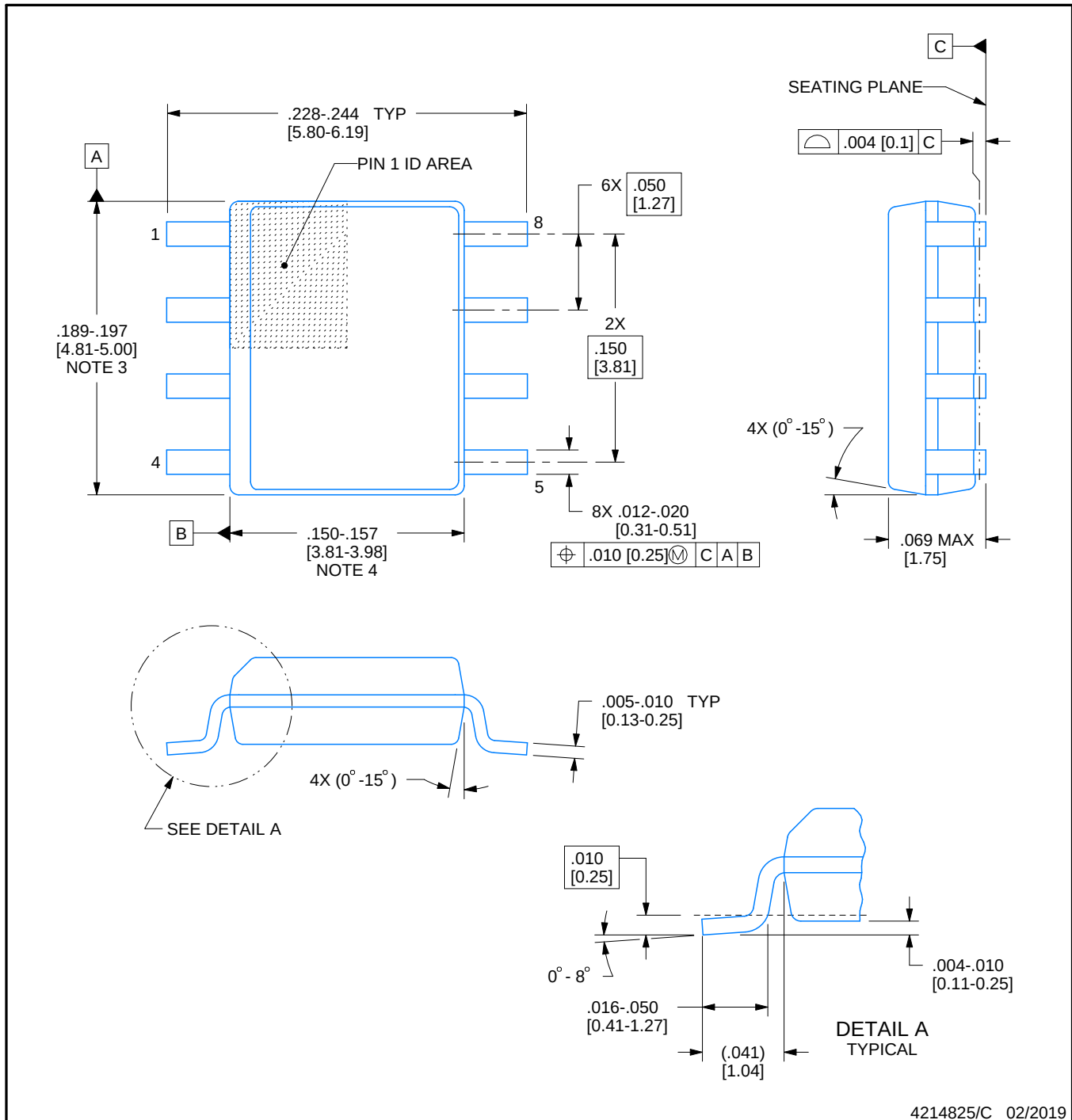
4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

D0008A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

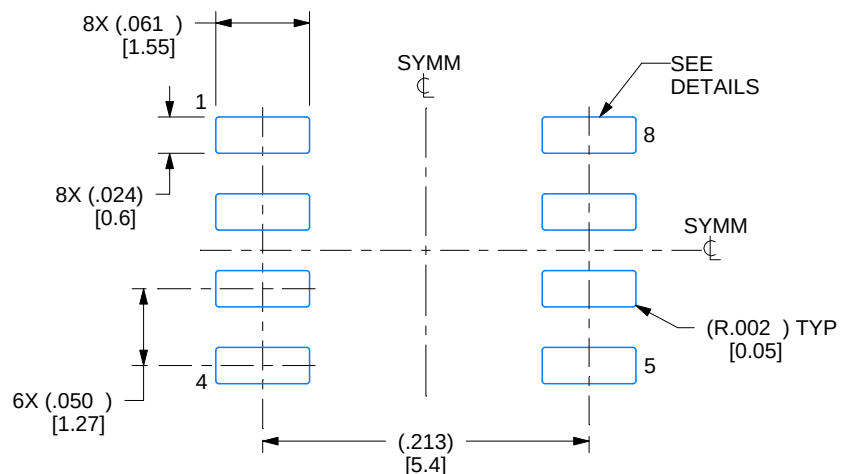
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

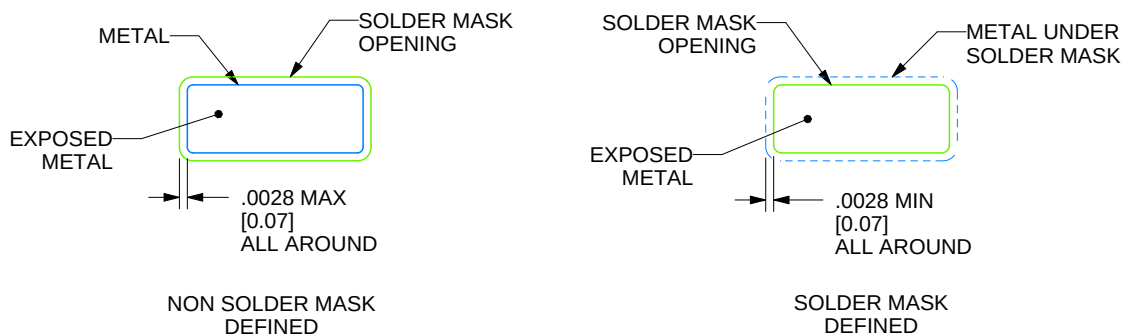
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

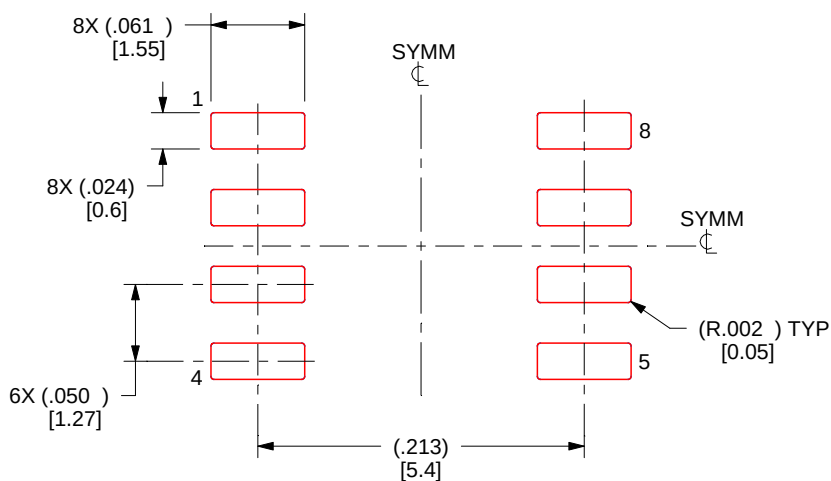
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated