



## High Performance Sensorless Motor Control IC

### Description

IRMCF171 is a high performance flash memory based motion control IC designed primarily for appliance applications. IRMCF171 is designed to achieve low cost yet high performance control solutions for advanced inverterized appliance motor control. IRMCF171 contains two computation engines integrated into one monolithic chip. One is the Flexible Motion Control Engine (MCE™) for sensorless control of permanent magnet or induction motors; the other is an 8-bit high-speed microcontroller (8051). The user can program a motion control algorithm by connecting control elements using a graphic compiler. Key components of the complex sensorless control algorithms, such as the Angle Estimator, are provided as complete pre-defined control blocks. A unique analog/digital circuit and algorithm fully supports single or leg shunt current reconstruction. The MCE and 8051 microcontroller communicate via dual port RAM for signal monitoring and command input. An advanced graphic compiler for the MCE™ is seamlessly integrated into the MATLAB/Simulink environment, while third party JTAG-based emulator tools are supported for 8051 software development including a flash programmer. IRMCF171 comes in a 48 pin QFP package.

### Features

- MCE™ (Flexible Motion Control Engine) - Dedicated computation engine for high efficiency sinusoidal sensorless motor control
- Built-in hardware peripheral for single or two shunt current feedback reconstruction and analog circuits
- Supports induction machine and both interior and surface permanent magnet motor sensorless control
- Loss minimization Space Vector PWM
- Two-channel analog output (PWM)
- Embedded 8-bit high speed microcontroller (8051) for flexible I/O and man-machine control
- JTAG programming port for emulation/debugger
- Serial communication interface (UART)
- I2C/SPI serial interface
- Three general purpose timers/counters
- Two special timers: periodic timer, capture timer
- Watchdog timer with independent internal clock
- Internal 64 Kbyte flash memory
- 5V tolerant I/O
- 3.3V single supply

### Product Summary

|                                              |                            |
|----------------------------------------------|----------------------------|
| Maximum clock input ( $f_{\text{crystal}}$ ) | 60 MHz                     |
| Maximum Internal clock (SYSCLK)              | 120MHz                     |
| Maximum 8051 clock (8051CLK)                 | 30MHz                      |
| Sensorless control computation time          | 35 $\mu\text{sec}$ @100MHz |
| MCE™ computation data range                  | 16 bit signed              |
| 8051 Program Flash                           | 52KB                       |
| 805/MCE Data RAM                             | 4KB                        |
| MCE Program RAM                              | 12KB                       |
| GateKill latency (digital filtered)          | 2 $\mu\text{sec}$          |
| PWM carrier frequency                        | 20 bits/ SYSCLK            |
| A/D input channels                           | 7                          |
| A/D converter resolution                     | 12 bits                    |
| A/D converter conversion speed               | 2 $\mu\text{sec}$          |
| Analog output (PWM) resolution               | 8 bits                     |
| UART baud rate (typ)                         | 57.6K bps                  |
| Number of digital I/O (max)                  | 14                         |
| Package (lead free)                          | QFP48                      |
| Typical 3.3V operating current               | 30mA                       |

| Base Part Number | Package Type | Standard Pack |          | Orderable Part Number |
|------------------|--------------|---------------|----------|-----------------------|
|                  |              | Form          | Quantity |                       |
| IRMCF171         | LQFP48       | Tape and Reel | 2000     | IRMCF171TR            |
| IRMCF171         | LQFP48       | Tray          | 2500     | IRMCF171TY            |

## Table of Contents

|      |                                                      |    |
|------|------------------------------------------------------|----|
| 1    | Overview.....                                        | 5  |
| 2    | Pinout .....                                         | 6  |
| 3    | IRMCF171 Block Diagram and Main Functions .....      | 7  |
| 4    | Application connection and Pin function .....        | 9  |
| 4.1  | 8051 Peripheral Interface Group.....                 | 10 |
| 4.2  | Motion Peripheral Interface Group.....               | 11 |
| 4.3  | Analog Interface Group.....                          | 11 |
| 4.4  | Power Interface Group.....                           | 12 |
| 4.5  | Test Interface Group.....                            | 12 |
| 5    | DC Characteristics.....                              | 13 |
| 5.1  | Absolute Maximum Ratings .....                       | 13 |
| 5.2  | System Clock Frequency and Power Consumption.....    | 13 |
| 5.3  | Digital I/O DC Characteristics .....                 | 14 |
| 5.4  | PLL and Oscillator DC characteristics .....          | 15 |
| 5.5  | Analog I/O DC Characteristics.....                   | 15 |
| 5.6  | Under Voltage Lockout DC characteristics .....       | 16 |
| 5.7  | Itrip comparator DC characteristics.....             | 16 |
| 5.8  | CNEXT and AREF Characteristics .....                 | 16 |
| 6    | AC Characteristics .....                             | 17 |
| 6.1  | Digital PLL AC Characteristics.....                  | 17 |
| 6.2  | Analog to Digital Converter AC Characteristics ..... | 18 |
| 6.3  | Op amp AC Characteristics .....                      | 19 |
| 6.4  | SYNC to SVPWM and A/D Conversion AC Timing.....      | 20 |
| 6.5  | GATEKILL to SVPWM AC Timing .....                    | 21 |
| 6.6  | Itrip AC Timing.....                                 | 21 |
| 6.7  | Interrupt AC Timing.....                             | 22 |
| 6.8  | I <sup>2</sup> C AC Timing.....                      | 23 |
| 6.9  | SPI AC Timing .....                                  | 24 |
|      | SPI Write AC timing .....                            | 24 |
|      | SPI Read AC Timing.....                              | 25 |
| 6.10 | UART AC Timing .....                                 | 26 |
| 6.11 | CAPTURE Input AC Timing.....                         | 27 |
| 6.12 | JTAG AC Timing.....                                  | 28 |
| 7    | I/O Structure .....                                  | 29 |
| 8    | Pin List.....                                        | 32 |
| 9    | Package Dimensions .....                             | 34 |
| 10   | Part Marking Information .....                       | 35 |
| 11   | Qualification Information† .....                     | 35 |

## List of Tables

|                                                          |    |
|----------------------------------------------------------|----|
| Table 2. Absolute Maximum Ratings .....                  | 13 |
| Table 3. System Clock Frequency .....                    | 13 |
| Table 4. Digital I/O DC Characteristics .....            | 14 |
| Table 5 PLL DC Characteristics .....                     | 15 |
| Table 6. Analog I/O DC Characteristics .....             | 15 |
| Table 7. UVcc DC Characteristics .....                   | 16 |
| Table 8. Itrip DC Characteristics .....                  | 16 |
| Table 9. CMEXT and AREF DC Characteristics .....         | 16 |
| Table 10. PLL AC Characteristics .....                   | 17 |
| Table 11 . A/D Converter AC Characteristics .....        | 18 |
| Table 12 Current Sensing OP Amp AC Characteristics ..... | 19 |
| Table 13. SYNC AC Characteristics .....                  | 20 |
| Table 14. GATEKILL to SVPWM AC Timing .....              | 21 |
| Table 15. Itrip AC Timing .....                          | 21 |
| Table 16. Interrupt AC Timing .....                      | 22 |
| Table 17. I <sup>2</sup> C AC Timing .....               | 23 |
| Table 18. SPI Write AC Timing .....                      | 24 |
| Table 19. SPI Read AC Timing .....                       | 25 |
| Table 20. UART AC Timing .....                           | 26 |
| Table 21. CAPTURE AC Timing .....                        | 27 |
| Table 22. JTAG AC Timing .....                           | 28 |
| Table 23. Pin List .....                                 | 33 |

## List of Figures

|                                                                            |    |
|----------------------------------------------------------------------------|----|
| Figure 1. Typical Application Block Diagram Using IRMCF171 .....           | 5  |
| Figure 2. Pinout of IRMCF171 .....                                         | 6  |
| Figure 3. IRMCF171 Block Diagram .....                                     | 7  |
| Figure 4. IRMCF171 Leg Shunt Connection Diagram .....                      | 9  |
| Figure 5. IRMCF171 Single Shunt Connection Diagram .....                   | 10 |
| Figure 6. Crystal circuit example .....                                    | 17 |
| Figure 7. Voltage droop and S/H hold time .....                            | 18 |
| Figure 8 Op amp output capacitor .....                                     | 19 |
| Figure 9. SYNC timing .....                                                | 20 |
| Figure 10. Gatekill timing .....                                           | 21 |
| Figure 11. ITRIP timing .....                                              | 21 |
| Figure 12. Interrupt timing .....                                          | 22 |
| Figure 13. I <sup>2</sup> C Timing .....                                   | 23 |
| Figure 14. SPI write timing .....                                          | 24 |
| Figure 15. SPI read timing .....                                           | 25 |
| Figure 16. UART timing .....                                               | 26 |
| Figure 17. CAPTURE timing .....                                            | 27 |
| Figure 18. JTAG timing .....                                               | 28 |
| Figure 19. PWMUL/PWMUH/PWMVL/PWMVH/PWMWL/PWMWH output .....                | 29 |
| Figure 20. All digital I/O except motor PWM output .....                   | 29 |
| Figure 21. RESET, GATEKILL I/O .....                                       | 29 |
| Figure 22. Analog input .....                                              | 30 |
| Figure 24 Analog operational amplifier output and AREF I/O structure ..... | 30 |
| Figure 25. VSS,AVSS pin I/O structure .....                                | 30 |
| Figure 26. VDD1,VDDCAP pin I/O structure .....                             | 31 |
| Figure 27. XTAL0/XTAL1 pins structure .....                                | 31 |

## 1 Overview

IRMCF171 is a new generation International Rectifier integrated circuit device primarily designed as a one-chip solution for complete inverterized appliance motor control applications. Unlike a traditional microcontroller or DSP, the IRMCF171 provides a built-in closed loop sensorless control algorithm using the unique flexible Motion Control Engine (MCE™) for permanent magnet motors as well as induction motors. The MCE™ consists of a collection of control elements, motion peripherals, a dedicated motion control sequencer and dual port RAM to map internal signal nodes. IRMCF171 also employs a unique single shunt current reconstruction circuit in addition to two leg shunt current sensing circuit to eliminate additional analog/digital circuitry and enables a direct shunt resistor interface to the IC. Motion control programming is achieved using a dedicated graphical compiler integrated into the MATLAB/Simulink™ development environment. Sequencing, user interface, host communication, and upper layer control tasks can be implemented in the 8051 high-speed 8-bit microcontroller. The 8051 microcontroller is equipped with a JTAG port to facilitate emulation and debugging tools. Figure 1 shows a typical application schematic using the IRMCF171.

IRMCF171 contains 64 Kbytes of Flash program memory. The IRMCK171 contains 32 Kbytes OTP memory and is intended for high volume production purposes while the IRMCF171 is intended for flexible volume production. Both the Flash and ROM versions come in a 48-pin QFP package with identical pin configuration to facilitate PC board layout and transition to mass production.

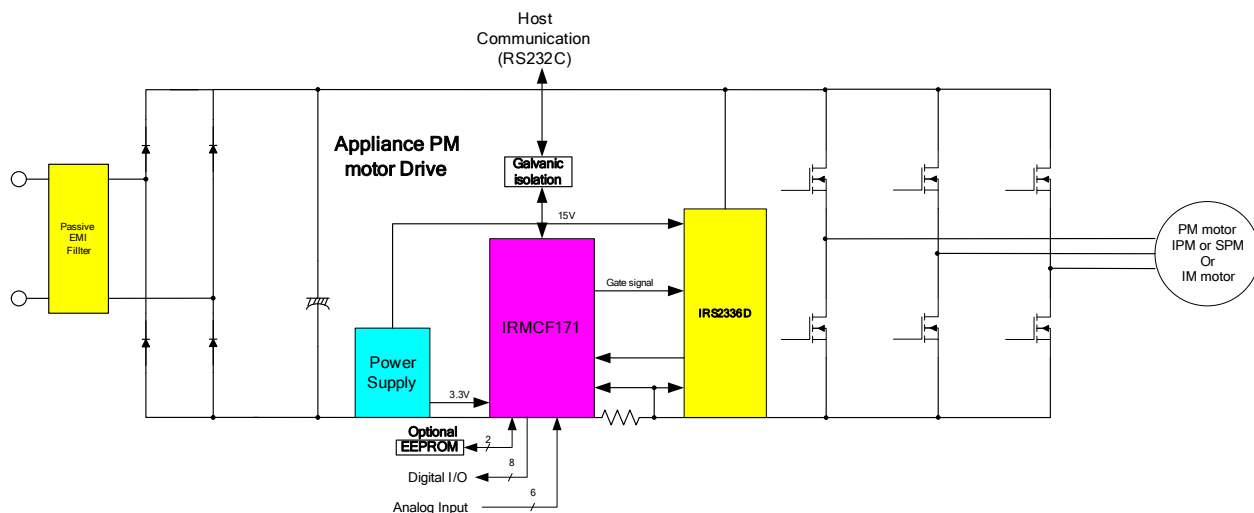


Figure 1. Typical Application Block Diagram Using IRMCF171

## 2 Pinout

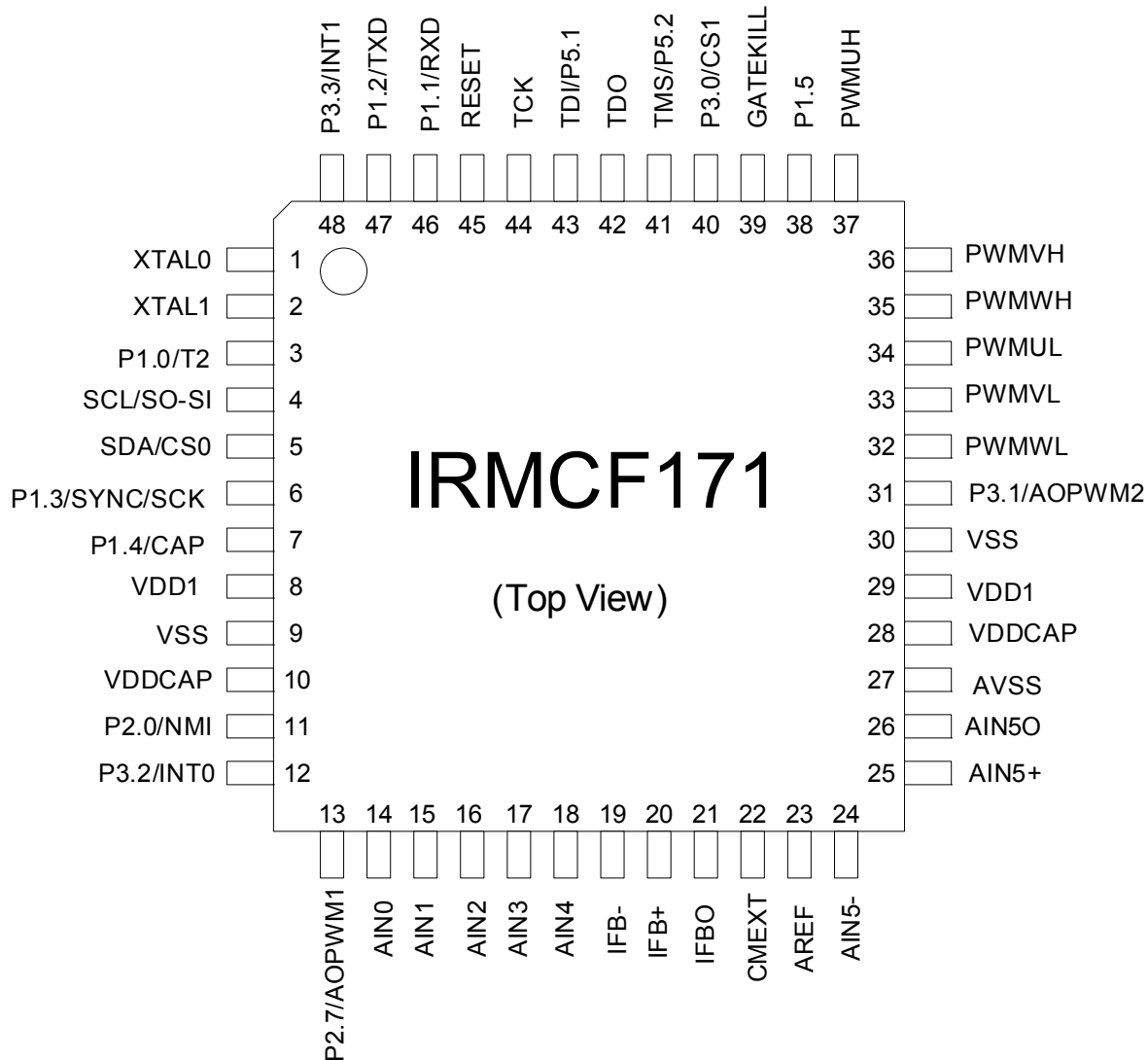


Figure 2. Pinout of IRMCF171

### 3 IRMCF171 Block Diagram and Main Functions

IRMCF171 block diagram for leg shunt mode is shown in Figure 3.

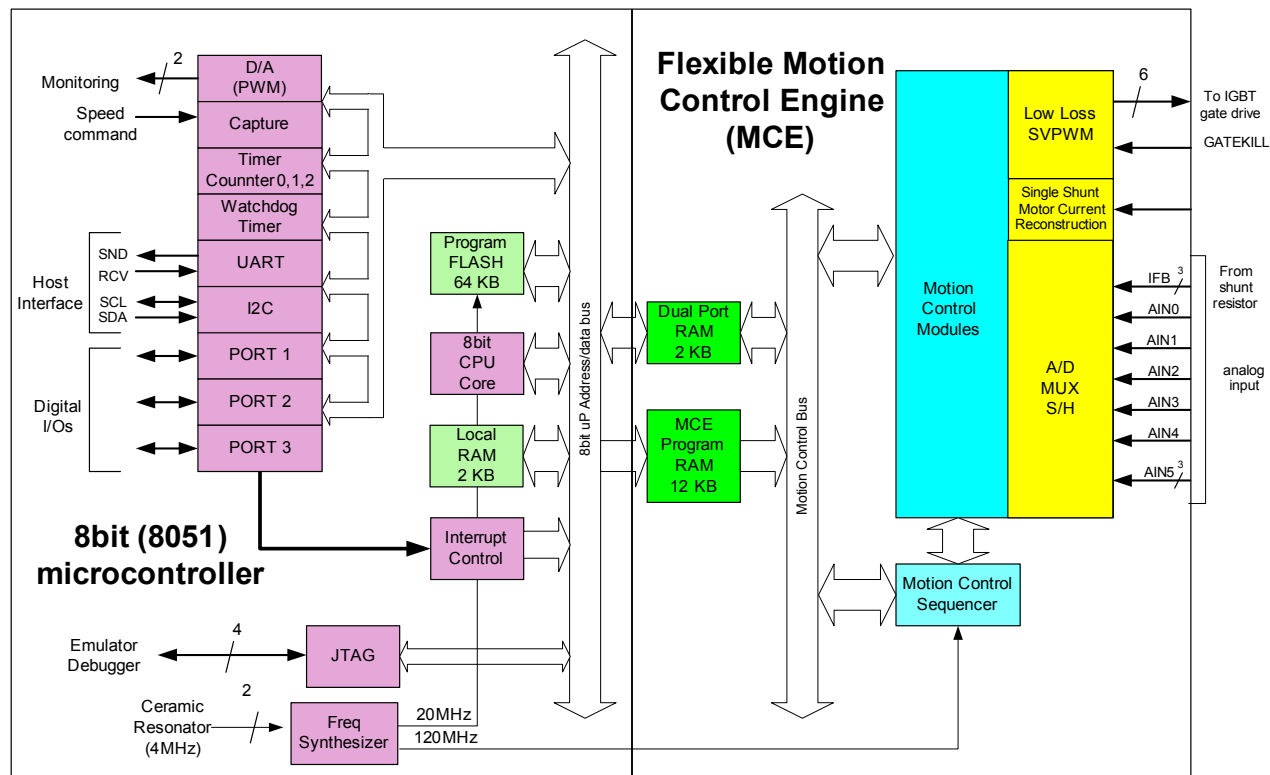


**Figure 3. IRMCF171 Block Diagram**

IRMCF171 contains the following functions for sensorless AC motor control applications:

#### Motion Control Engine (MCE™)

- Sensorless FOC (complete sensorless field oriented control)
- Proportional plus Integral block
- Low pass filter
- Differentiator and lag (high pass filter)
- Ramp
- Limit
- Angle estimate (sensorless control)
- Inverse Clark transformation
- Vector rotator
- Bit latch
- Peak detect
- Transition
- Multiply-divide (signed and unsigned)
- Adder
- Divide (signed and unsigned)

#### 8051 microcontroller

- Two 16 bit timer/counters
- One 16 bit periodic timer
- One 16 bit watchdog timer
- One 16 bit capture timer
- Up to 14 discrete digital I/Os
- Seven-channel 12 bit A/D
  - Buffered (current sensing) two channels (0 – 1.2V input)
  - Unbuffered five channels (0 – 1.2V input)
- JTAG port (4 pins)
- Up to two channels of analog output (8 bit PWM)
- UART
- I<sup>2</sup>C/SPI port
- 2K byte data RAM

- Subtractor
  - Comparator
  - Counter
  - Accumulator
  - Switch
  - Shift
  - ATAN (arc tangent)
  - Function block (any curve fitting, nonlinear function)
  - 16 bit wide Logic operations (AND, OR, XOR, NOT, NEGATE)
  - MCE™ program memory and dual port RAM (6K byte)
  - MCE™ control sequencer
- 64K byte Flash memory

## 4 Application connection and Pin function

Figure 4 shows the application connections in leg shunt mode. Figure 5 shows the application connections in single shunt mode.

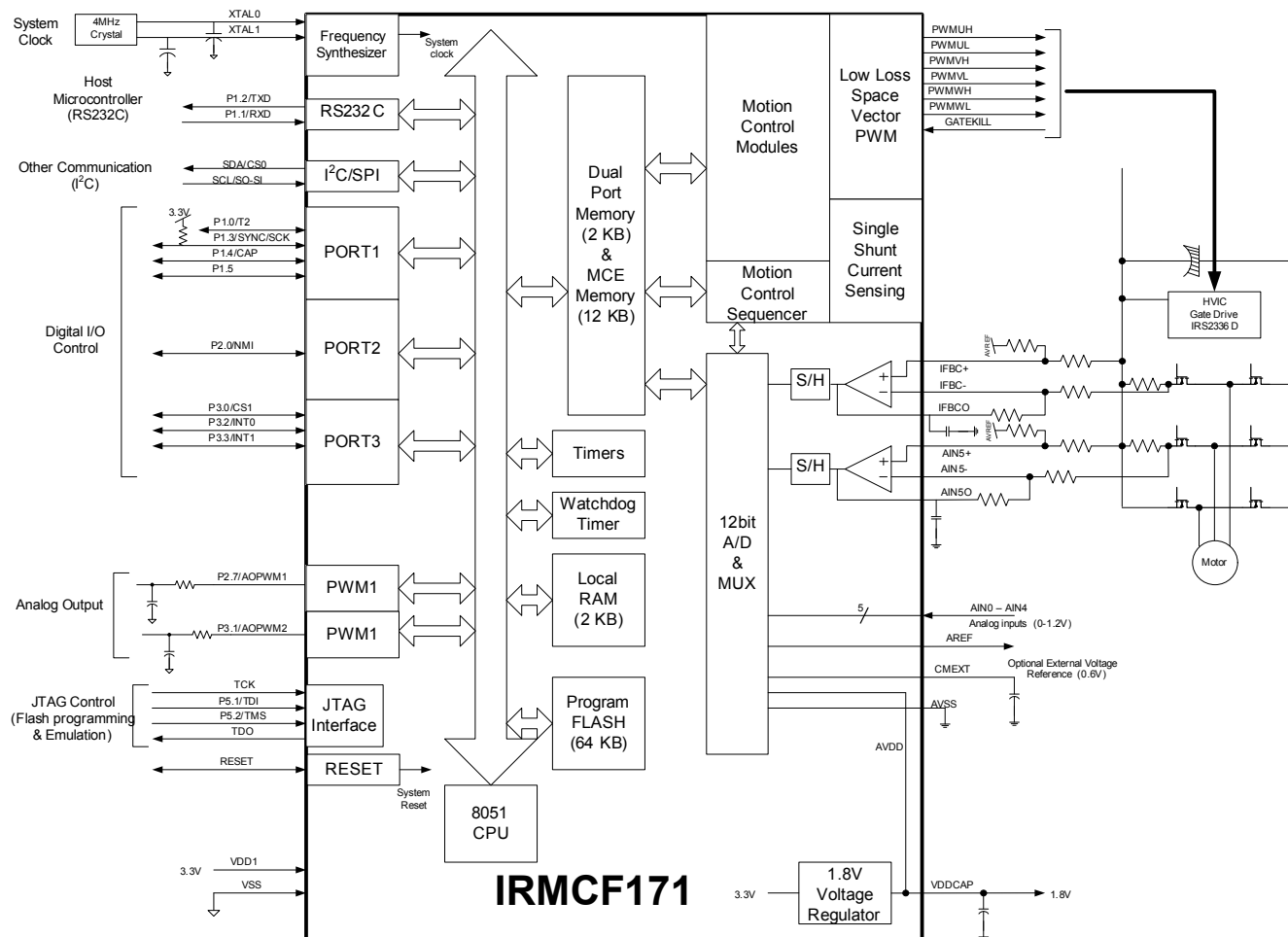


**Figure 4. IRMCF171 Leg Shunt Connection Diagram**

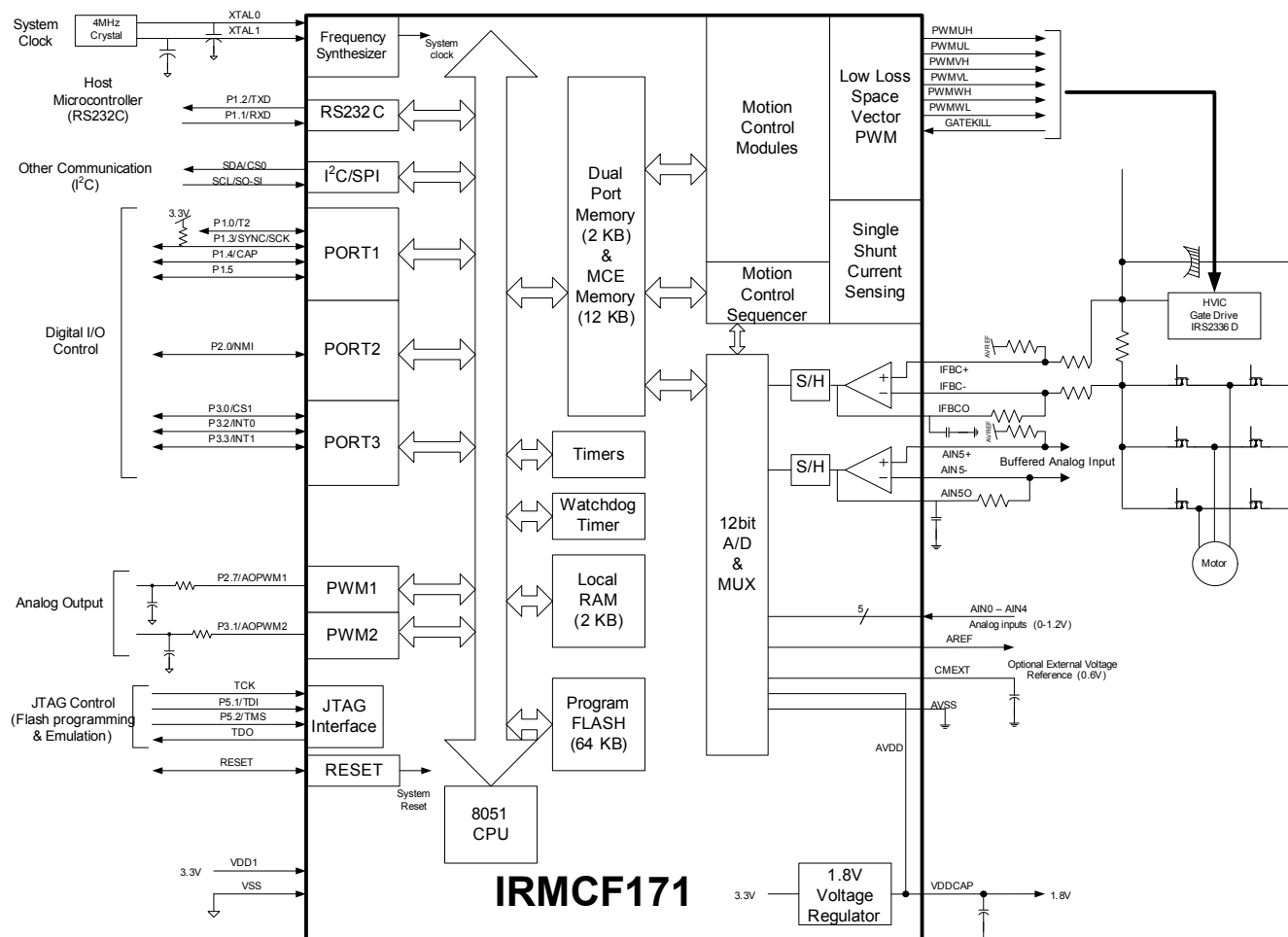


Figure 5. IRMCF171 Single Shunt Connection Diagram

## 4.1 8051 Peripheral Interface Group

### UART Interface

|          |                                     |
|----------|-------------------------------------|
| P1.2/TXD | Output, Transmit data from IRMCF171 |
| P1.1/RXD | Input, Receive data to IRMCF171     |

### Discrete I/O Interface

|               |                                                                             |
|---------------|-----------------------------------------------------------------------------|
| P1.0/T2       | Input/output port 1.0, can be configured as Timer/Counter 2 input           |
| P1.1/RXD      | Input/output port 1.1, can be configured as RXD input                       |
| P1.2/TXD      | Input/output port 1.2, can be configured as TXD output                      |
| P1.3/SYNC/SCK | Input/output port 1.3, can be configured as SYNC output or SPI clock output |
| P1.4/CAP      | Input/output port 1.4, can be configured as Capture Timer input             |
| P1.5          | Input/output port 1.5                                                       |
| P2.0/NMI      | Input/output port 2.0, can be configured as non-maskable interrupt input    |
| P2.7/AOPWM1   | Input/output port 2.7, can be configured as AOPWM1 output                   |
| P3.0/INT2/CS1 | Input/output port 3.0, can be configured as INT2 input or SPI chip select 1 |
| P3.1/AOPWM2   | Input/output port 3.1, can be configured as AOPWM2 output                   |
| P3.2/NINT0    | Input/output port 3.2, can be configured as INT0 input                      |
| P3.3/NINT1    | Input/output port 3.3, can be configured as INT1 input                      |
| P5.1/TDI      | Input port 5.1, configured as JTAG port by default                          |

P5.2/TMS      Input port 5.2, configured as JTAG port by default

#### **Analog Output Interface**

P2.7/AOPWM1      Input/output, can be configured as 8-bit PWM output 1 with programmable carrier frequency  
P3.1/AOPWM2      Input/output, can be configured as 8-bit PWM output 2 with programmable carrier frequency

#### **Crystal Interface**

XTAL0      Input, connected to crystal  
XTAL1      Output, connected to crystal

#### **Reset Interface**

RESET      Input and Output, system reset, doesn't require external RC time constant

#### **I<sup>2</sup>C Interface**

SCL/SO-SI      Output, I<sup>2</sup>C clock output, or SPI data  
SDA/CS0      Input/output, I<sup>2</sup>C Data line or SPI chip select 0

#### **I<sup>2</sup>C/SPI Interface**

SCL/SO-SI      Output, I<sup>2</sup>C clock output, or SPI data  
SDA/CS0      Input/output, I<sup>2</sup>C data line or SPI chip select 0  
P1.3/SYNC/SCK      Input/output port 1.3, can be configured as SYNC output or SPI clock output  
P3.0/INT2/CS1      Input/output port 3.0, can be configured as INT2 input or SPI chip select 1

## **4.2 Motion Peripheral Interface Group**

### **PWM**

PWMUH      Output, PWM phase U high side gate signal, internally pulled down by 58kΩ, configured high true at a power up  
PWMUL      Output, PWM phase U low side gate signal, internally pulled down by 58kΩ, configured high true at a power up  
PWMVH      Output, PWM phase V high side gate signal, internally pulled down by 58kΩ, configured high true at a power up  
PWMVL      Output, PWM phase V low side gate signal, internally pulled down by 58kΩ, configured high true at a power up  
PWMWH      Output, PWM phase W high side gate signal, internally pulled down by 58kΩ, configured high true at a power up  
PWMWL      Output, PWM phase W low side gate signal, internally pulled down by 58kΩ, configured high true at a power up  
PFCPWM      Output, PFCPWM output signal, internally pulled up by 70kΩ, configured low true at a power up

### **Fault**

GATEKILL      Input, upon assertion this negates all six PWM signals, active low, internally pulled up by 70kΩ

## **4.3 Analog Interface Group**

AVSS      Analog power return, (analog internal 1.8V power is shared with VDDCAP)  
AREF      0.6V buffered output  
CMEXT      Unbuffered 0.6V, input to the AREF buffer, capacitor needs to be connected.  
IFB+      Input, Operational amplifier positive input for shunt resistor current sensing

|       |                                                                                                           |
|-------|-----------------------------------------------------------------------------------------------------------|
| IFB-  | Input, Operational amplifier negative input for shunt resistor current sensing                            |
| IFBO  | Output, Operational amplifier output for shunt resistor current sensing                                   |
| AIN0  | Input, Analog input channel 0 (0 – 1.2 V), typically configured for DC bus voltage input                  |
| AIN1  | Input, Analog input channel 1 (0 – 1.2 V), needs to be pulled down to AVSS if unused                      |
| AIN2  | Input, Analog input channel 2 (0 – 1.2 V), needs to be pulled down to AVSS if unused                      |
| AIN3  | Input, Analog input channel 3 (0 – 1.2 V), needs to be pulled down to AVSS if unused                      |
| AIN4  | Input, Analog input channel 4 (0 – 1.2 V), needs to be pulled down to AVSS if unused                      |
| AIN5+ | Input, Operational amplifier positive input for shunt resistor current sensing                            |
| AIN5- | Input, Operational amplifier negative input for shunt resistor current sensing                            |
| AIN5O | Output, Operational amplifier output for AIN5 output, there is a single sample/hold circuit on the output |

#### 4.4 Power Interface Group

|        |                                                                                                                                                                                                                                                    |
|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VDD1   | Digital power (3.3V)                                                                                                                                                                                                                               |
| VDDCAP | Internal 1.8V output, requires capacitors to the pin. Shared with analog power pad internally<br><b>Note:</b> The internal 1.8V supply is not designed to power any external circuits or devices. Only capacitors should be connected to this pin. |
| VSS    | Digital common                                                                                                                                                                                                                                     |

#### 4.5 Test Interface Group

|          |                                            |
|----------|--------------------------------------------|
| P5.2/TMS | JTAG test mode input or input digital port |
| TDO      | JTAG data output                           |
| P5.1/TDI | JTAG data input, or input digital port     |
| TCK      | JTAG test clock                            |

## 5 DC Characteristics

### 5.1 Absolute Maximum Ratings

| Symbol           | Parameter             | Min    | Typ | Max    | Condition       |
|------------------|-----------------------|--------|-----|--------|-----------------|
| V <sub>DD1</sub> | Supply Voltage        | -0.3 V | -   | 3.6 V  | Respect to VSS  |
| V <sub>IA</sub>  | Analog Input Voltage  | -0.3 V | -   | 1.98 V | Respect to AVSS |
| V <sub>ID</sub>  | Digital Input Voltage | -0.3 V | -   | 6.0 V  | Respect to VSS  |
| T <sub>A</sub>   | Ambient Temperature   | -40 °C | -   | 85 °C  |                 |
| T <sub>S</sub>   | Storage Temperature   | -65 °C | -   | 150 °C |                 |

**Table 1. Absolute Maximum Ratings**

**Caution:** Stresses beyond those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and function of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

### 5.2 System Clock Frequency and Power Consumption

C<sub>AREF</sub> = 1nF, C<sub>MEXT</sub> = 100nF. VDD1=3.3V, Unless specified, Ta = 25°C.

| Symbol         | Parameter         | Min | Typ               | Max | Unit |
|----------------|-------------------|-----|-------------------|-----|------|
| SYSCLK         | System Clock      | 32  | -                 | 120 | MHz  |
| P <sub>D</sub> | Power consumption |     | 100 <sup>1)</sup> | -   | mW   |

**Table 2. System Clock Frequency**

Note 1) The value is based on the condition of MCE clock=120MHz, 8051 clock 30MHz with a actual motor running by a typical MCE application program and 8051 code.

### 5.3 Digital I/O DC Characteristics

| Symbol          | Parameter                 | Min     | Typ         | Max             | Condition               |
|-----------------|---------------------------|---------|-------------|-----------------|-------------------------|
| $V_{DD1}$       | Supply Voltage            | 3.0 V   | 3.3 V       | 3.6 V           | Recommended             |
| $V_{IL}$        | Input Low Voltage         | -0.3 V  | -           | 0.8 V           | Recommended             |
| $V_{IH}$        | Input High Voltage        | 2.0 V   |             | 3.6 V           | Recommended             |
| $C_{IN}$        | Input capacitance         | -       | 3.6 pF      | -               | (1)                     |
| $I_L$           | Input leakage current     |         | $\pm 10$ nA | $\pm 1$ $\mu$ A | $V_O = 3.3$ V or 0 V    |
| $I_{OL1}^{(2)}$ | Low level output current  | 8.9 mA  | 13.2 mA     | 15.2 mA         | $V_{OL} = 0.4$ V<br>(1) |
| $I_{OH1}^{(2)}$ | High level output current | 12.4 mA | 24.8 mA     | 38 mA           | $V_{OH} = 2.4$ V<br>(1) |
| $I_{OL2}^{(3)}$ | Low level output current  | 17.9 mA | 26.3 mA     | 33.4 mA         | $V_{OL} = 0.4$ V<br>(1) |
| $I_{OH2}^{(3)}$ | High level output current | 24.6 mA | 49.5 mA     | 81 mA           | $V_{OH} = 2.4$ V<br>(1) |

**Table 3. Digital I/O DC Characteristics**

Note:

- (1) Data guaranteed by design.
- (2) Applied to SCL/SO-SI, SDA/CS0 pins.
- (3) Applied to all digital I/O pins except SCL/SO-SI and SDA/CS0 pins.

## 5.4 PLL and Oscillator DC characteristics

$C_{\text{AREF}} = 1\text{nF}$ ,  $C_{\text{MEXT}} = 100\text{nF}$ .  $V_{\text{DD1}} = 3.3\text{V}$ , Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol              | Parameter                                  | Min                          | Typ | Max                          | Condition                                  |
|---------------------|--------------------------------------------|------------------------------|-----|------------------------------|--------------------------------------------|
| $V_{\text{IL OSC}}$ | Oscillator (XTAL0,1)<br>Input Low Voltage  | 0                            | -   | $0.2 \cdot V_{\text{DDCAP}}$ | $V_{\text{DDCAP}}$ = voltage at VDDCAP pin |
| $V_{\text{IH OSC}}$ | Oscillator (XTAL0,1)<br>Input High Voltage | $0.8 \cdot V_{\text{DDCAP}}$ | -   | $V_{\text{DDCAP}}$           | $V_{\text{DDCAP}}$ = voltage at VDDCAP pin |

**Table 4 PLL DC Characteristics**

## 5.5 Analog I/O DC Characteristics

- OP amps for current sensing (IFB+, IFB-, IFBO, AIN5+, AIN5-, AIN5O)

$C_{\text{AREF}} = 1\text{nF}$ ,  $C_{\text{MEXT}} = 100\text{nF}$ .  $V_{\text{DD1}} = 3.3\text{V}$ , Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol                      | Parameter                        | Min                  | Typ               | Max           | Condition                              |
|-----------------------------|----------------------------------|----------------------|-------------------|---------------|----------------------------------------|
| $V_{\text{OFFSET}}$         | Input Offset Voltage             | -                    | -                 | 26 mV         | $V_{\text{AVDD}} = 1.8\text{ V}$       |
| $V_{\text{I}}$              | Input Voltage Range              | 0 V                  |                   | 1.2 V         | Recommended                            |
| $V_{\text{OUTSW}}$          | OP amp output<br>operating range | 50 mV <sup>(1)</sup> | -                 | 1.2 V         | $V_{\text{AVDD}} = 1.8\text{ V}$       |
| $C_{\text{IN}}$             | Input capacitance                | -                    | 3.6 pF            | -             | (1)                                    |
| $R_{\text{FDBK}}$           | OP amp feedback<br>resistor      | 5 k $\Omega$         | -                 | 20 k $\Omega$ | Requested<br>between IFBO and<br>IFB-  |
| $\text{OP}_{\text{GAINCL}}$ | Operating Close loop<br>Gain     | 80 db                | -                 | -             | (1)                                    |
| CMRR                        | Common Mode<br>Rejection Ratio   | -                    | 80 db             | -             | (1)                                    |
| $I_{\text{SRC}}$            | Op amp output source<br>current  | -                    | 1 mA              | -             | $V_{\text{OUT}} = 0.6\text{ V}$<br>(1) |
| $I_{\text{SNK}}$            | Op amp output sink<br>current    | -                    | 100 $\mu\text{A}$ | -             | $V_{\text{OUT}} = 0.6\text{ V}$<br>(1) |

**Table 5. Analog I/O DC Characteristics**

Note:

(1) Data guaranteed by design.

## 5.6 Under Voltage Lockout DC characteristics

Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol     | Parameter                     | Min    | Typ    | Max    | Condition |
|------------|-------------------------------|--------|--------|--------|-----------|
| $UV_{CC+}$ | UVcc positive going Threshold | 2.78 V | 3.04 V | 3.23 V | (1)       |
| $UV_{CC-}$ | UVcc negative going Threshold | 2.78 V | 2.97 V | 3.23 V |           |
| $UV_{CCH}$ | UVcc Hysteresys               | -      | 73 mV  | -      | (1)       |

**Table 6. UVcc DC Characteristics**

Note:

(1) Data guaranteed by design.

## 5.7 Itrip comparator DC characteristics

Unless specified,  $V_{DD1}=3.3\text{V}$ ,  $T_a = 25^\circ\text{C}$ .

| Symbol      | Parameter                      | Min | Typ   | Max | Condition                |
|-------------|--------------------------------|-----|-------|-----|--------------------------|
| $I_{trip+}$ | Itrip positive going Threshold | -   | 1.22V | -   | $V_{DD1} = 3.3\text{ V}$ |
| $I_{trip-}$ | Itrip negative going Threshold | -   | 1.10V | -   | $V_{DD1} = 3.3\text{ V}$ |
| $I_{tripH}$ | Itrip Hysteresys               | -   | 120mV | -   |                          |

**Table 7. Itrip DC Characteristics**

## 5.8 CMEXT and AREF Characteristics

$C_{AREF} = 1\text{nF}$ ,  $C_{MEXT} = 100\text{nF}$ . Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol       | Parameter                        | Min    | Typ    | Max    | Condition                 |
|--------------|----------------------------------|--------|--------|--------|---------------------------|
| $V_{CM}$     | CMEXT voltage                    | 495 mV | 600 mV | 700 mV | $V_{VDD1} = 3.3\text{ V}$ |
| $V_{AREF}$   | Buffer Output Voltage            | 495 mV | 600 mV | 700 mV | $V_{VDD1} = 3.3\text{ V}$ |
| $\Delta V_o$ | Load regulation ( $V_{DC}-0.6$ ) | -      | 1 mV   | -      | (1)                       |
| PSRR         | Power Supply Rejection Ratio     | -      | 75 db  | -      | (1)                       |

**Table 8. CMEXT and AREF DC Characteristics**

Note:

(1) Data guaranteed by design.

## 6 AC Characteristics

### 6.1 Digital PLL AC Characteristics

| Symbol      | Parameter                   | Min                  | Typ      | Max           | Condition                            |
|-------------|-----------------------------|----------------------|----------|---------------|--------------------------------------|
| $F_{CLKIN}$ | Crystal input frequency     | 3.2 MHz              | 4 MHz    | 60 MHz        | <sup>(1)</sup><br>(see figure below) |
| $F_{PLL}$   | Internal clock frequency    | 32 MHz               | 50 MHz   | 128 MHz       | <sup>(1)</sup>                       |
| $F_{LWPPW}$ | Sleep mode output frequency | $F_{CLKIN} \div 256$ | -        | -             | <sup>(1)</sup>                       |
| $J_S$       | Short time jitter           | -                    | 200 psec | -             | <sup>(1)</sup>                       |
| $D$         | Duty cycle                  | -                    | 50 %     | -             | <sup>(1)</sup>                       |
| $T_{LOCK}$  | PLL lock time               | -                    | -        | 500 $\mu$ sec | <sup>(1)</sup>                       |

**Table 9. PLL AC Characteristics**

Note:

(1) Data guaranteed by design.

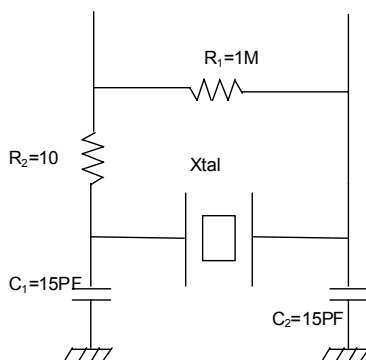


**Figure 6. Crystal circuit example**

## 6.2 Analog to Digital Converter AC Characteristics

Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol            | Parameter                     | Min | Typ | Max                  | Condition                                         |
|-------------------|-------------------------------|-----|-----|----------------------|---------------------------------------------------|
| $T_{\text{CONV}}$ | Conversion time               | -   | -   | 2.05 $\mu\text{sec}$ | (1)                                               |
| $T_{\text{HOLD}}$ | Sample/Hold maximum hold time | -   | -   | 10 $\mu\text{sec}$   | Voltage droop $\leq 15$ LSB<br>(see figure below) |

**Table 10 . A/D Converter AC Characteristics**

Note:

(1) Data guaranteed by design.

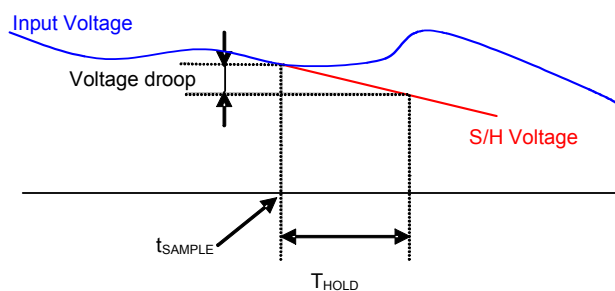


**Figure 7. Voltage droop and S/H hold time**

### 6.3 Op amp AC Characteristics

Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol     | Parameter          | Min | Typ                   | Max | Condition                                                     |
|------------|--------------------|-----|-----------------------|-----|---------------------------------------------------------------|
| $OP_{SR}$  | OP amp slew rate   | -   | 10 V/ $\mu\text{sec}$ | -   | $V_{DD1} = 3.3\text{ V}$ , $CL = 33\text{ pF}$ <sup>(1)</sup> |
| $OP_{IMP}$ | OP input impedance | -   | $10^8\ \Omega$        | -   | <sup>(1)</sup> <sup>(2)</sup>                                 |
| $T_{SET}$  | Settling time      | -   | 400 ns                | -   | $V_{DD1} = 3.3\text{ V}$ , $CL = 33\text{ pF}$ <sup>(1)</sup> |

**Table 11 Current Sensing OP Amp AC Characteristics**

Note:

(1) Data guaranteed by design.

(2) To guarantee stability of the operational amplifier, it is recommended to load the output pin by a capacitor of 47pF, see Figure 8. Here only the single shunt current amplifier is shown but all op amp outputs should be loaded with this capacitor value.

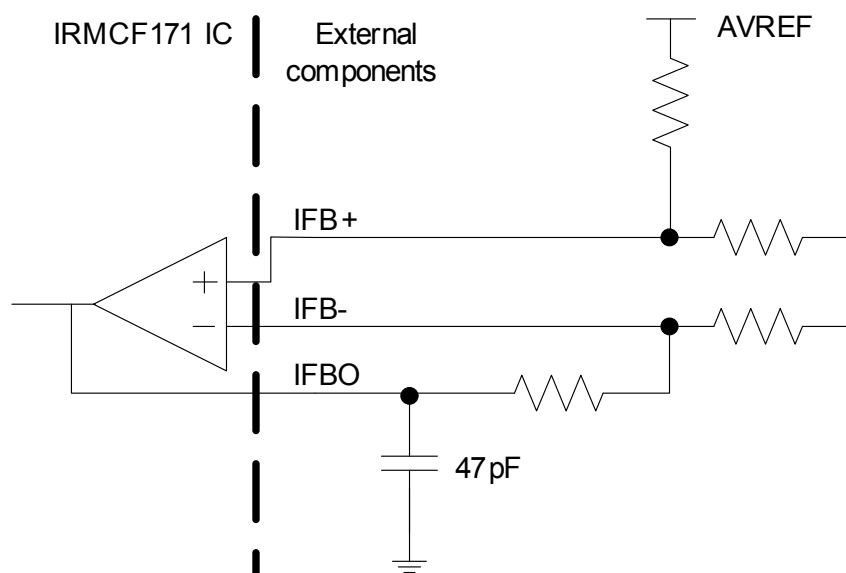


**Figure 8 Op amp output capacitor**

## 6.4 SYNC to SVPWM and A/D Conversion AC Timing

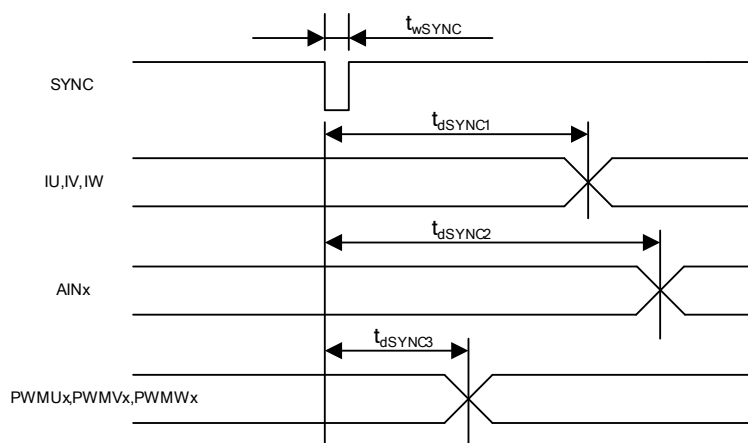


**Figure 9. SYNC timing**

Unless specified, Ta = 25°C.

| Symbol              | Parameter                                               | Min | Typ | Max | Unit                  |
|---------------------|---------------------------------------------------------|-----|-----|-----|-----------------------|
| $t_{w\text{SYNC}}$  | SYNC pulse width                                        | -   | 32  | -   | SYSCLK                |
| $t_{d\text{SYNC1}}$ | SYNC to current feedback conversion time                | -   | -   | 100 | SYSCLK                |
| $t_{d\text{SYNC2}}$ | SYNC to AIN0-4, ADCH, ADCL analog input conversion time | -   | -   | 200 | SYSCLK <sup>(1)</sup> |
| $t_{d\text{SYNC3}}$ | SYNC to PWM output delay time                           | -   | -   | 2   | SYSCLK                |

**Table 12. SYNC AC Characteristics**

Note:

(1) AIN1 – AIN5 channels are converted once every 5 SYNC events

## 6.5 GATEKILL to SVPWM AC Timing

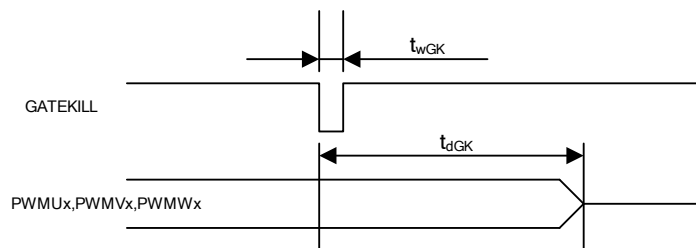


**Figure 10. Gatekill timing**

Unless specified, Ta = 25°C.

| Symbol    | Parameter                    | Min | Typ | Max | Unit  |
|-----------|------------------------------|-----|-----|-----|-------|
| $t_{wGK}$ | GATEKILL pulse width         | 32  | -   | -   | SYCLK |
| $t_{dGK}$ | GATEKILL to PWM output delay | -   | -   | 100 | SYCLK |

**Table 13. GATEKILL to SVPWM AC Timing**

## 6.6 Itrip AC Timing

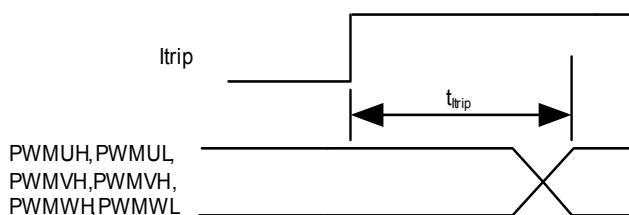


**Figure 11. ITRIP timing**

Unless specified, Ta = 25°C.

| Symbol      | Parameter               | Min | Typ | Max                 | Unit       |
|-------------|-------------------------|-----|-----|---------------------|------------|
| $t_{ITRIP}$ | Itrip propagation delay | -   | -   | 100(sysclk)+1.0usec | SYCLK+usec |

**Table 14. Itrip AC Timing**

## 6.7 Interrupt AC Timing

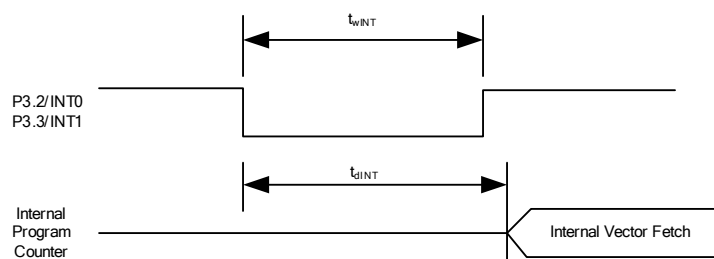


**Figure 12. Interrupt timing**

Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol     | Parameter                           | Min | Typ | Max | Unit    |
|------------|-------------------------------------|-----|-----|-----|---------|
| $t_{WINT}$ | INT0, INT1 Interrupt Assertion Time | 4   | -   | -   | SYSCCLK |
| $t_{dINT}$ | INT0, INT1 latency                  | -   | -   | 4   | SYSCCLK |

**Table 15. Interrupt AC Timing**

## 6.8 I<sup>2</sup>C AC Timing

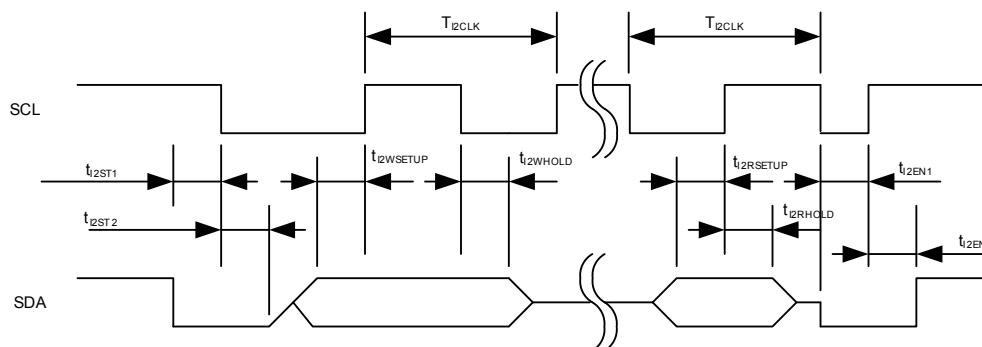


**Figure 13. I<sup>2</sup>C Timing**

Unless specified, Ta = 25°C.

| Symbol                | Parameter                         | Min                                         | Typ | Max  | Unit               |
|-----------------------|-----------------------------------|---------------------------------------------|-----|------|--------------------|
| T <sub>I2CLK</sub>    | I <sup>2</sup> C clock period     | 10                                          | -   | 8192 | SYCLK              |
| t <sub>I2ST1</sub>    | I <sup>2</sup> C SDA start time   | 0.25                                        | -   | -    | T <sub>I2CLK</sub> |
| t <sub>I2ST2</sub>    | I <sup>2</sup> C SCL start time   | 0.25                                        | -   | -    | T <sub>I2CLK</sub> |
| t <sub>I2WSETUP</sub> | I <sup>2</sup> C write setup time | 0.25                                        | -   | -    | T <sub>I2CLK</sub> |
| t <sub>I2WHOLD</sub>  | I <sup>2</sup> C write hold time  | 0.25                                        | -   | -    | T <sub>I2CLK</sub> |
| t <sub>I2RSETUP</sub> | I <sup>2</sup> C read setup time  | I <sup>2</sup> C filter time <sup>(1)</sup> | -   | -    | SYCLK              |
| t <sub>I2RHOLD</sub>  | I <sup>2</sup> C read hold time   | 1                                           | -   | -    | SYCLK              |

**Table 16. I<sup>2</sup>C AC Timing**

Note:

(1) I<sup>2</sup>C read setup time is determined by the programmable filter time applied to I<sup>2</sup>C communication.

## 6.9 SPI AC Timing

### SPI Write AC timing

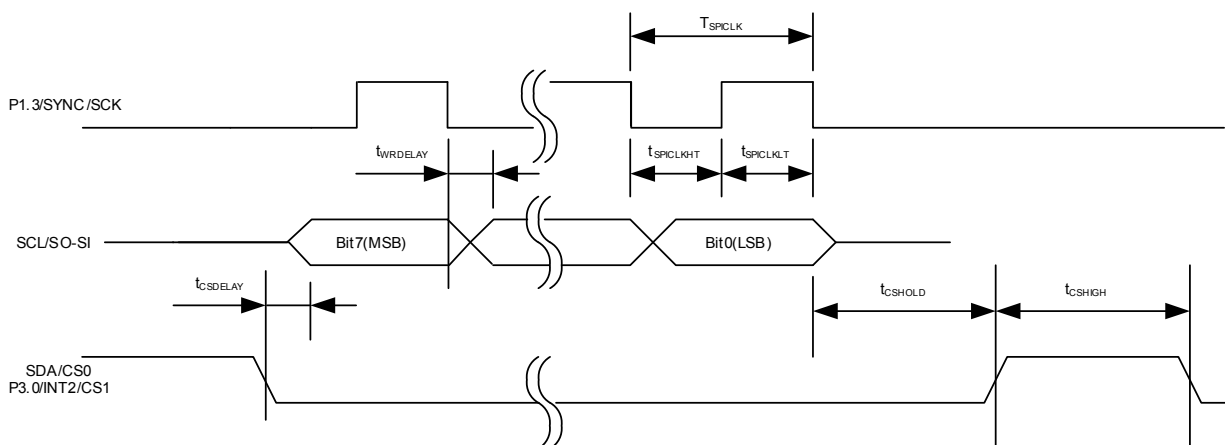


**Figure 14. SPI write timing**

Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol         | Parameter                                          | Min | Typ | Max | Unit         |
|----------------|----------------------------------------------------|-----|-----|-----|--------------|
| $T_{SPICLK}$   | SPI clock period                                   | 4   | -   | -   | SYSCCLK      |
| $t_{SPICLKHT}$ | SPI clock high time                                | -   | 1/2 | -   | $T_{SPICLK}$ |
| $t_{SPICLKLT}$ | SPI clock low time                                 | -   | 1/2 | -   | $T_{SPICLK}$ |
| $t_{CSDelay}$  | CS to data delay time                              | -   | -   | 10  | nsec         |
| $t_{WRDELAY}$  | CLK falling edge to data delay time                | -   | -   | 10  | nsec         |
| $t_{CSHIGH}$   | CS high time between two consecutive byte transfer | 1   | -   | -   | $T_{SPICLK}$ |
| $t_{CSHOLD}$   | CS hold time                                       | -   | 1   | -   | $T_{SPICLK}$ |

**Table 17. SPI Write AC Timing**

## SPI Read AC Timing

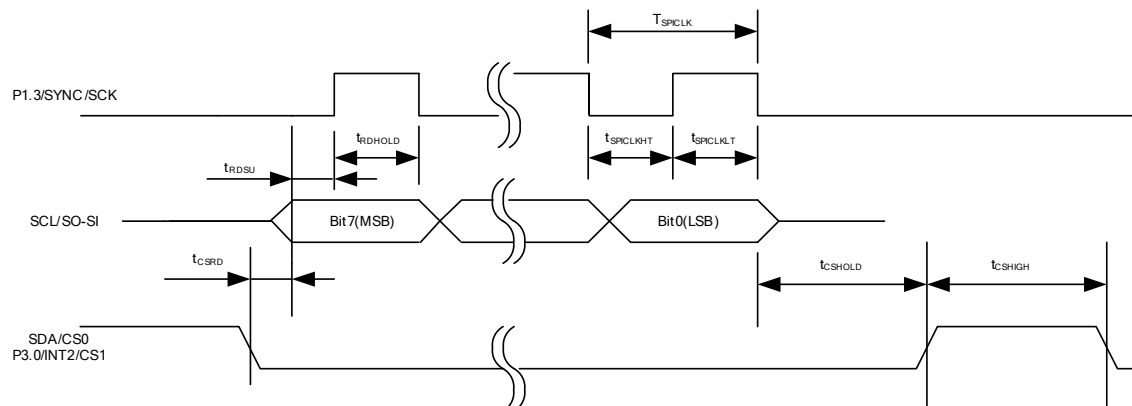


**Figure 15. SPI read timing**

Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol         | Parameter                                          | Min | Typ | Max | Unit         |
|----------------|----------------------------------------------------|-----|-----|-----|--------------|
| $T_{SPICLK}$   | SPI clock period                                   | 4   | -   | -   | SYSCCLK      |
| $t_{SPICLKHT}$ | SPI clock high time                                | -   | 1/2 | -   | $T_{SPICLK}$ |
| $t_{SPICLKLT}$ | SPI clock low time                                 | -   | 1/2 | -   | $T_{SPICLK}$ |
| $t_{CSRd}$     | CS to data delay time                              | -   | -   | 10  | nsec         |
| $t_{RDSU}$     | SPI read data setup time                           | 10  | -   | -   | nsec         |
| $t_{RDHOLD}$   | SPI read data hold time                            | 10  | -   | -   | nsec         |
| $t_{CSHIGH}$   | CS high time between two consecutive byte transfer | 1   | -   | -   | $T_{SPICLK}$ |
| $t_{CSHOLD}$   | CS hold time                                       | -   | 1   | -   | $T_{SPICLK}$ |

**Table 18. SPI Read AC Timing**

## 6.10 UART AC Timing

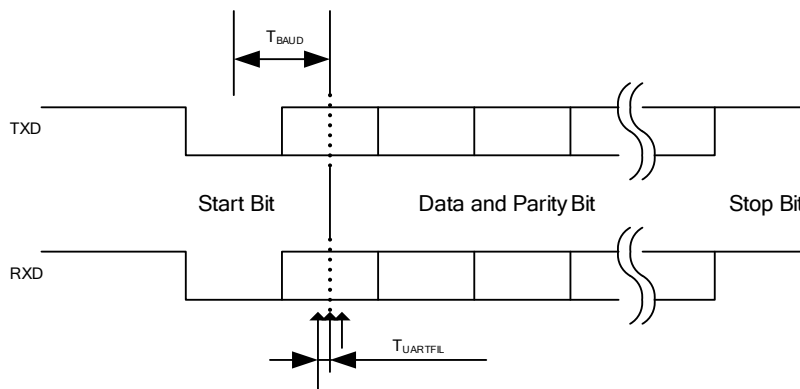


**Figure 16. UART timing**

Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol        | Parameter                                  | Min | Typ   | Max | Unit       |
|---------------|--------------------------------------------|-----|-------|-----|------------|
| $T_{BAUD}$    | Baud Rate Period                           | -   | 57600 | -   | bit/sec    |
| $T_{UARTFIL}$ | UART sampling filter period <sup>(1)</sup> | -   | 1/16  | -   | $T_{BAUD}$ |

**Table 19. UART AC Timing**

Note:

- (1) Each bit including start and stop bit is sampled three times at center of a bit at an interval of  $1/16 T_{BAUD}$ . If three sampled values do not agree, then UART noise error is generated.

## 6.11 CAPTURE Input AC Timing

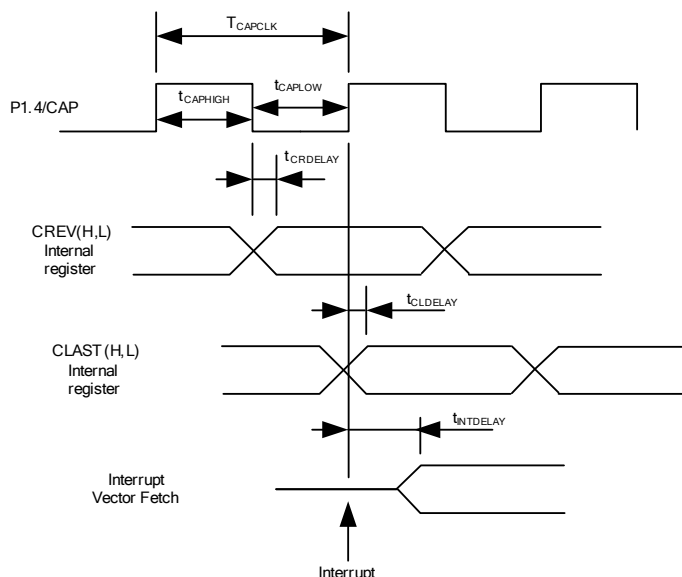


**Figure 17. CAPTURE timing**

Unless specified,  $T_a = 25^\circ\text{C}$ .

| Symbol         | Parameter                                           | Min | Typ | Max | Unit    |
|----------------|-----------------------------------------------------|-----|-----|-----|---------|
| $T_{CAPCLK}$   | CAPTURE input period                                | 8   | -   | -   | SYSCCLK |
| $t_{CAPHIGH}$  | CAPTURE input high time                             | 4   | -   | -   | SYSCCLK |
| $t_{CAPLOW}$   | CAPTURE input low time                              | 4   | -   | -   | SYSCCLK |
| $t_{CRDELAY}$  | CAPTURE falling edge to capture register latch time | -   | -   | 4   | SYSCCLK |
| $t_{CLDELAY}$  | CAPTURE rising edge to capture register latch time  | -   | -   | 4   | SYSCCLK |
| $t_{INTDELAY}$ | CAPTURE input interrupt latency time                | -   | -   | 4   | SYSCCLK |

**Table 20. CAPTURE AC Timing**

## 6.12 JTAG AC Timing

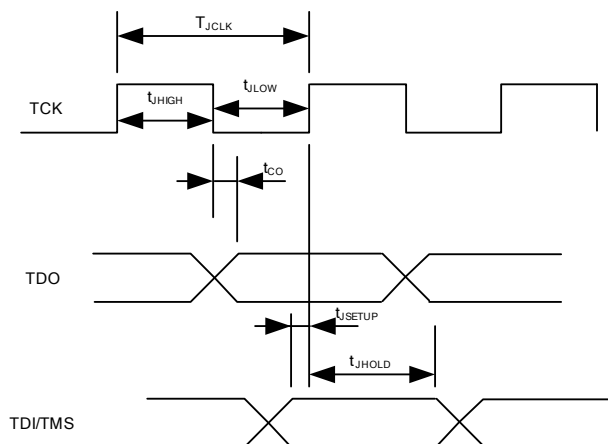


**Figure 18. JTAG timing**

Unless specified,  $T_a = 25^{\circ}\text{C}$ .

| Symbol       | Parameter                         | Min | Typ | Max | Unit |
|--------------|-----------------------------------|-----|-----|-----|------|
| $T_{JCLK}$   | TCK Period                        | -   | -   | 50  | MHz  |
| $t_{HIGH}$   | TCK High Period                   | 10  | -   | -   | nsec |
| $t_{LOW}$    | TCK Low Period                    | 10  | -   | -   | nsec |
| $t_{CO}$     | TCK to TDO propagation delay time | 0   | -   | 5   | nsec |
| $t_{JSETUP}$ | TDI/TMS setup time                | 4   | -   | -   | nsec |
| $t_{JHOLD}$  | TDI/TMS hold time                 | 0   | -   | -   | nsec |

**Table 21. JTAG AC Timing**

## 7 I/O Structure

The following figure shows the motor PWM output (PWMUH/PWMUL/PWMVH/PWMVL/PWMWH/PWMWL)

**Figure 19. PWMUL/PWMUH/PWMVL/PWMVH/PWMWL/PWMWH output**

The following figure shows the digital I/O structure except the motor PWM output

**Figure 20. All digital I/O except motor PWM output**

The following figure shows RESET and GATEKILL I/O structure.

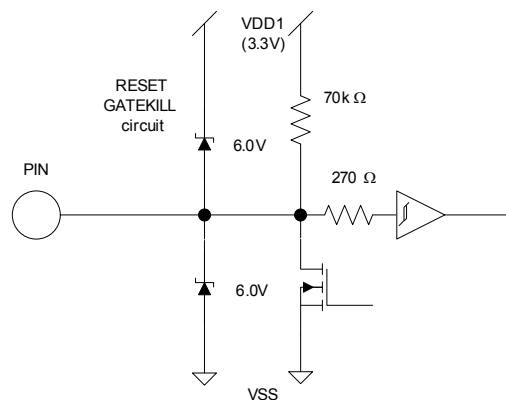


**Figure 21. RESET, GATEKILL I/O**

The following figure shows the analog input structure.

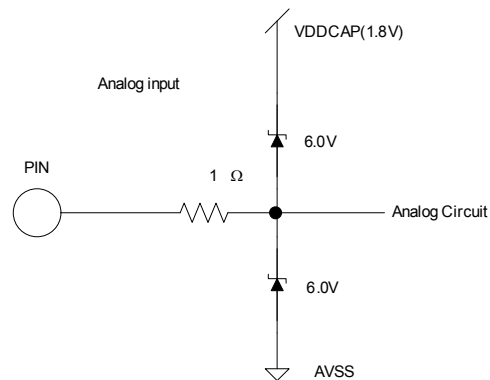


**Figure 22. Analog input**

The following figure shows all analog operational amplifier output pins and AREF pin I/O structure.

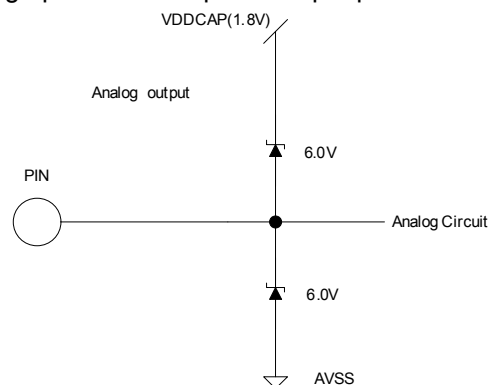


**Figure 23 Analog operational amplifier output and AREF I/O structure**

The following figure shows the VSS,AVSS pin I/O structure

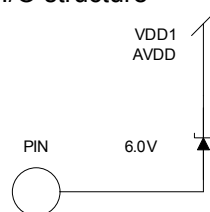


**Figure 24. VSS,AVSS pin I/O structure**

The following figure shows the VDD1,VDDCAP pin I/O structure

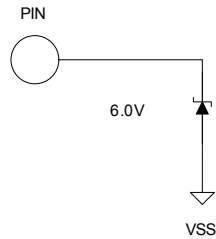


**Figure 25. VDD1,VDDCAP pin I/O structure**

The following figure shows the XTAL0 and XTAL1 pins structure

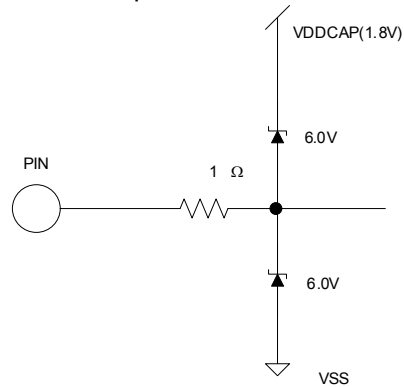


**Figure 26. XTAL0/XTAL1 pins structure**

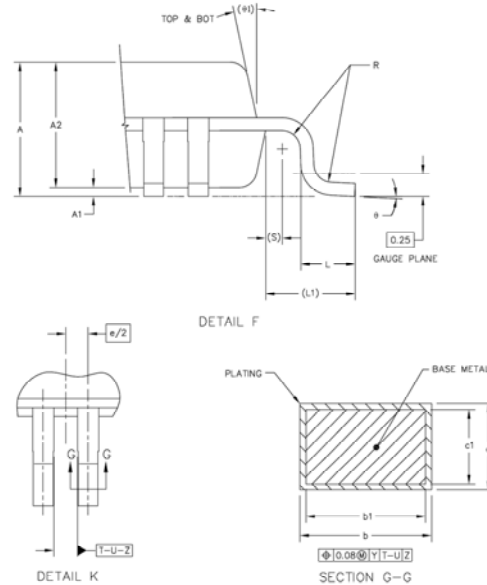
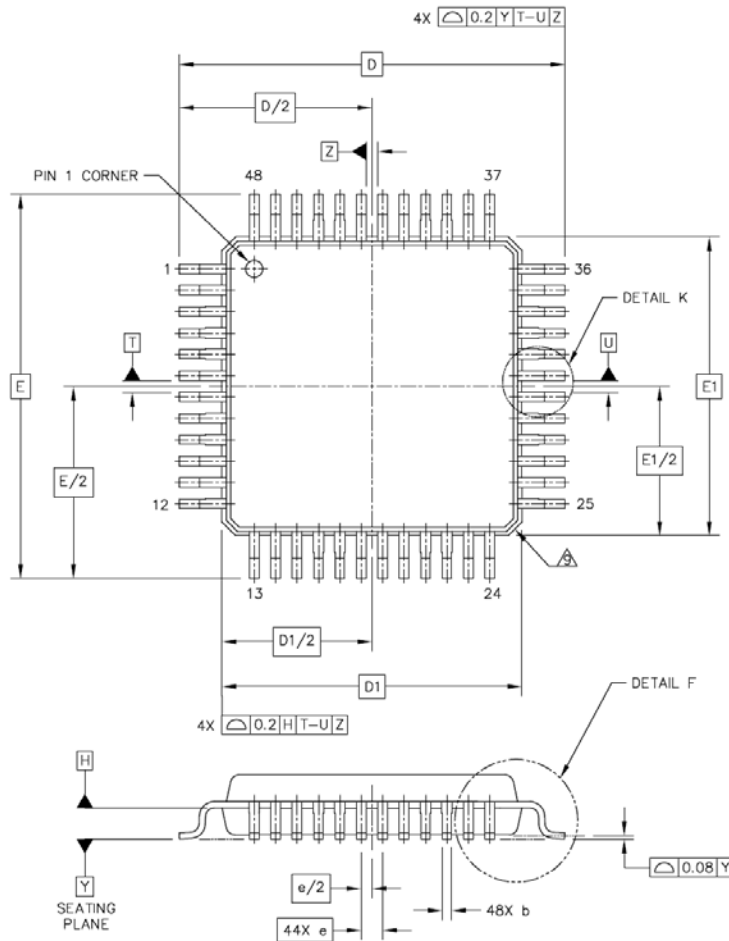
## 8 Pin List

| Pin Number | Pin Name      | Internal Pull-up /Pull-down | Pin Type | Description                                                                     |
|------------|---------------|-----------------------------|----------|---------------------------------------------------------------------------------|
| 1          | XTAL0         |                             | I        | Crystal input                                                                   |
| 2          | XTAL1         |                             | O        | Crystal output                                                                  |
| 3          | P1.0/T2       |                             | I/O      | Discrete programmable I/O or Timer/Counter 2 input                              |
| 4          | SCL/SO-SI     |                             | I/O      | I <sup>2</sup> C clock output (open drain, need pull up) or SPI data            |
| 5          | SDA/CS0       |                             | I/O      | I <sup>2</sup> C data (open drain, need pull up) or SPI Chip Select 0           |
| 6          | P1.3/SYNC/SCK |                             | I/O      | Discrete programmable I/O or SYNC output or SPI clock output                    |
| 7          | P1.4/CAP      |                             | I/O      | Discrete programmable I/O or Capture timer input                                |
| 8          | VDD1          |                             | P        | 3.3V digital power                                                              |
| 9          | VSS           |                             | P        | Digital common                                                                  |
| 10         | VDDCAP        |                             | P        | Internal 1.8V output, Capacitor(s) to be connected                              |
| 11         | P2.0/NMI      |                             | I/O      | Discrete programmable I/O or Non-maskable Interrupt input                       |
| 12         | P3.2/INT0     |                             | I/O      | Discrete programmable I/O or Interrupt 0 input                                  |
| 13         | P2.7/AOPWM1   |                             | I/O      | Discrete programmable I/O or PWM 1 digital output                               |
| 14         | AIN0          |                             | I        | Analog input channel 0, 0-1.2V range, needs to be pulled down to AVSS if unused |
| 15         | AIN1          |                             | I        | Analog input channel 1, 0-1.2V range, needs to be pulled down to AVSS if unused |
| 16         | AIN2          |                             | I        | Analog input channel 2, 0-1.2V range, needs to be pulled down to AVSS if unused |
| 17         | AIN3          |                             | I        | Analog input channel 3, 0-1.2V range, needs to be pulled down to AVSS if unused |
| 18         | AIN4          |                             | I        | Analog input channel 4, 0-1.2V range, needs to be pulled down to AVSS if unused |
| 19         | IFB-          |                             | I        | Single shunt current sensing OP amp input (-)                                   |
| 20         | IFB+          |                             | I        | Single shunt current sensing OP amp input (+)                                   |
| 21         | IFBO          |                             | O        | Single shunt current sensing OP amp output                                      |
| 22         | CMEXT         |                             | O        | Unbuffered 0.6V output. Capacitor needs to be connected.                        |
| 23         | AREF          |                             | O        | Analog reference voltage output (0.6V)                                          |
| 24         | AIN5-         |                             | I        | Analog input channel 5, 0-1.2V range, needs to be pulled down to AVSS if unused |
| 25         | AIN5+         |                             | I        | Analog input channel 5, 0-1.2V range, needs to be pulled down to AVSS if unused |
| 26         | AIN5O         |                             | O        | Analog output 5, 0-1.2V range,                                                  |
| 27         | AVSS          |                             | P        | Analog common                                                                   |
| 28         | VDDCAP        |                             | P        | Internal 1.8V output, Capacitor(s) to be connected                              |
| 29         | VDD1          |                             | P        | 3.3V digital power                                                              |
| 30         | VSS           |                             | P        | Digital common                                                                  |
| 31         | P3.1/AOPWM2   |                             | I/O      | Discrete programmable I/O or PWM 2 digital output                               |
| 32         | PWMWL         | 58 k $\Omega$ Pull down     | O        | PWM gate drive for phase W low side, configurable either high or low true.      |
| 33         | PWMVL         | 58 k $\Omega$ Pull down     | O        | PWM gate drive for phase V low side, configurable either high or low true       |

| Pin Number | Pin Name      | Internal Pull-up /Pull-down | Pin Type | Description                                                                  |
|------------|---------------|-----------------------------|----------|------------------------------------------------------------------------------|
| 34         | PWMUL         | 58 k $\Omega$ Pull down     | O        | PWM gate drive for phase U low side, configurable either high or low true    |
| 35         | PWMWH         | 58 k $\Omega$ Pull down     | O        | PWM gate drive for phase W high side, configurable either high or low true   |
| 36         | PWMVH         | 58 k $\Omega$ Pull down     | O        | PWM gate drive for phase V high side, configurable either high or low true   |
| 37         | PWMUH         | 58 k $\Omega$ Pull down     | O        | PWM gate drive for phase U high side, configurable either high or low true   |
| 38         | P1.5          |                             | I/O      | Discrete programmable I/O.                                                   |
| 39         | GATEKILL      | 70 k $\Omega$ Pull up       | I        | PWM shutdown input, configurable digital filter, active low input.           |
| 40         | P3.0/INT2/CS1 | 70 k $\Omega$ Pull up       | I/O      | Discrete programmable I/O or external interrupt 2 input or SPI Chip Select 1 |
| 41         | P5.2/TMS      |                             | I        | JTAG test mode input or input digital port                                   |
| 42         | TDO           |                             | O        | JTAG test data output                                                        |
| 43         | P5.1/TDI      |                             | I        | JTAG test data input or input digital port                                   |
| 44         | TCK           |                             | I        | JTAG test clock                                                              |
| 45         | RESET         |                             | I        | Reset, low true, Schmitt trigger input                                       |
| 46         | P1.1/RXD      |                             | I/O      | UART receiver input or Discrete programmable I/O                             |
| 47         | P1.2/RXD      |                             | I/O      | UART transmitter output or Discrete programmable I/O                         |
| 48         | P3.3/INT1     |                             | I/O      | Interrupt 1 input or Discrete I/O                                            |

**Table 22. Pin List**

## 9 Package Dimensions

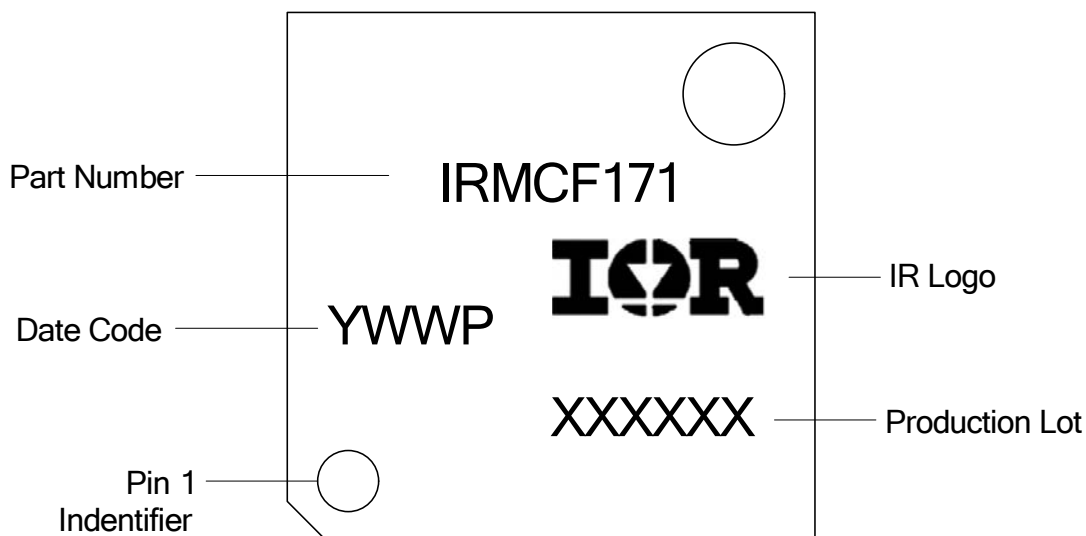


### NOTES:

- DIMENSIONS ARE IN MILLIMETERS.
- INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
- DATUM PLANE H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
- DATUM T, U AND Z TO BE DETERMINED AT DATUM PLANE H.
- DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE Y.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. DAM BAR PROTRUSION SHALL NOT CAUSE THE b DIMENSION TO EXCEED 0.35.
- MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
- EXACT SHAPE OF EACH CORNER IS OPTIONAL.

| DIM | MIN     | MAX  | DIM | MIN     | MAX  | DIM | MIN | MAX |
|-----|---------|------|-----|---------|------|-----|-----|-----|
| A   | 1.4     | 1.6  | L1  | 1 REF   |      |     |     |     |
| A1  | 0.05    | 0.15 | R   | 0.15    | 0.25 |     |     |     |
| A2  | 1.35    | 1.45 | S   | 0.2 REF |      |     |     |     |
| b   | 0.17    | 0.27 | θ   | 1°      | 5°   |     |     |     |
| b1  | 0.17    | 0.23 | θ1  | 12° REF |      |     |     |     |
| c   | 0.09    | 0.2  |     |         |      |     |     |     |
| c1  | 0.09    | 0.16 |     |         |      |     |     |     |
| D   | 9 BSC   |      |     |         |      |     |     |     |
| D1  | 7 BSC   |      |     |         |      |     |     |     |
| e   | 0.5 BSC |      |     |         |      |     |     |     |
| E   | 9 BSC   |      |     |         |      |     |     |     |
| E1  | 7 BSC   |      |     |         |      |     |     |     |
| L   | 0.5     | 0.7  |     |         |      |     |     |     |

## 10 Part Marking Information



## 11 Qualification Information †

|                                   |                         |                                                       |
|-----------------------------------|-------------------------|-------------------------------------------------------|
| <b>Qualification Level</b>        |                         | Industrial <sup>††</sup><br>(per JEDEC JESD 47E)      |
| <b>Moisture Sensitivity Level</b> |                         | MSL3 <sup>†††</sup><br>(per IPC/JEDEC J-STD-020C)     |
| <b>ESD</b>                        | <b>Machine Model</b>    | Class B<br>(per JEDEC standard JESD22-A114D)          |
|                                   | <b>Human Body Model</b> | Class 2<br>(per EIA/JEDEC standard EIA/JESD22-A115-A) |
| <b>RoHS Compliant</b>             |                         | Yes                                                   |

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

## Revision History

Rev A First Revision  
(March 10, 2013)

International  
 Rectifier

Data and Specifications are subject to change without notice

**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105

TAC Fax: (310) 252-7903

Visit us at [www.irf.com](http://www.irf.com) for sales contact information