LXT6282

Octal E1 Digital Interface with CRC-4 Monitoring and Jitter/Wander Suppression

Datasheet

LXT6282 is an eight-channel E1 digital interface. It integrates an E1 dejitter phase locked loop, an E1 retiming function and a CRC-4 monitor function for each E1 transmitter and a CRC-4 monitoring function for each E1 receiver. It is optimized for SDH applications and can used in conjunction with the LXT6251A (21 E1 mapper).

Applications

- SDH 21 or 63 E1 multiplexer
- STM-0 and STM1 SDH add/drop multiplexer
- PDH NxE1 multiplexer
- DCS
- Microwave radio
- Satellite
- Test equipment
- Protection Switch

Product Features

- Octal E1 transceiver digital interface
- Performs the jitter attenuation function on a gapped clock supplied by a PDH or SDH multiplexer
- Performs CRC4 performance monitoring on both transmit and receive sides
- Provides a retiming function on the transmit side for SDH applications (demapped E1 tributaries)
- Built-in HDB3 encoder/decoder
- Compatible with LXT6251A for STM-0/1 applications
- Compatible with LXT334 and the next generation octal LIU
- Microprocessor programmable
- Low power, 3.3 Volt operation, 5 V tolerant I/O
- IEEE 1149.1 (JTAG) compliant
- LQFP - 144 surface mount packaging
- Compatible with ITU G.703, G.704, G.706, G.707, G.775 (Draft 1996), G.783 and G.742
- Industrial temperature operating range -40°C to +85°C.

As of January 15, 2001, this document replaces the Level One document *LXT6282 Octal E1 Digital Interface with CRC-4 Monitoring and Jitter/Wander Suppression*. Order Number: 249279-001 January 2001

Datasheet

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Revision	Date	Description

Figure 1. LXT6282 Block Diagram

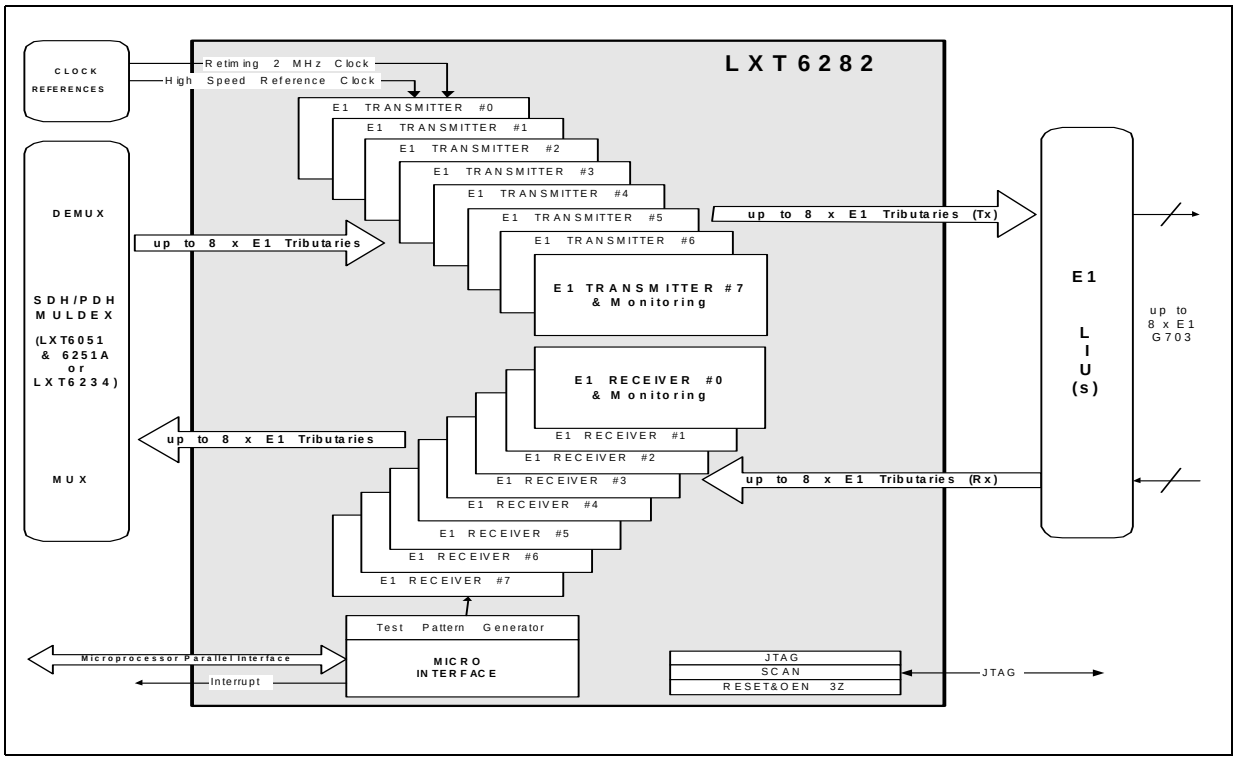


Figure 2. LXT6282 Block Diagram

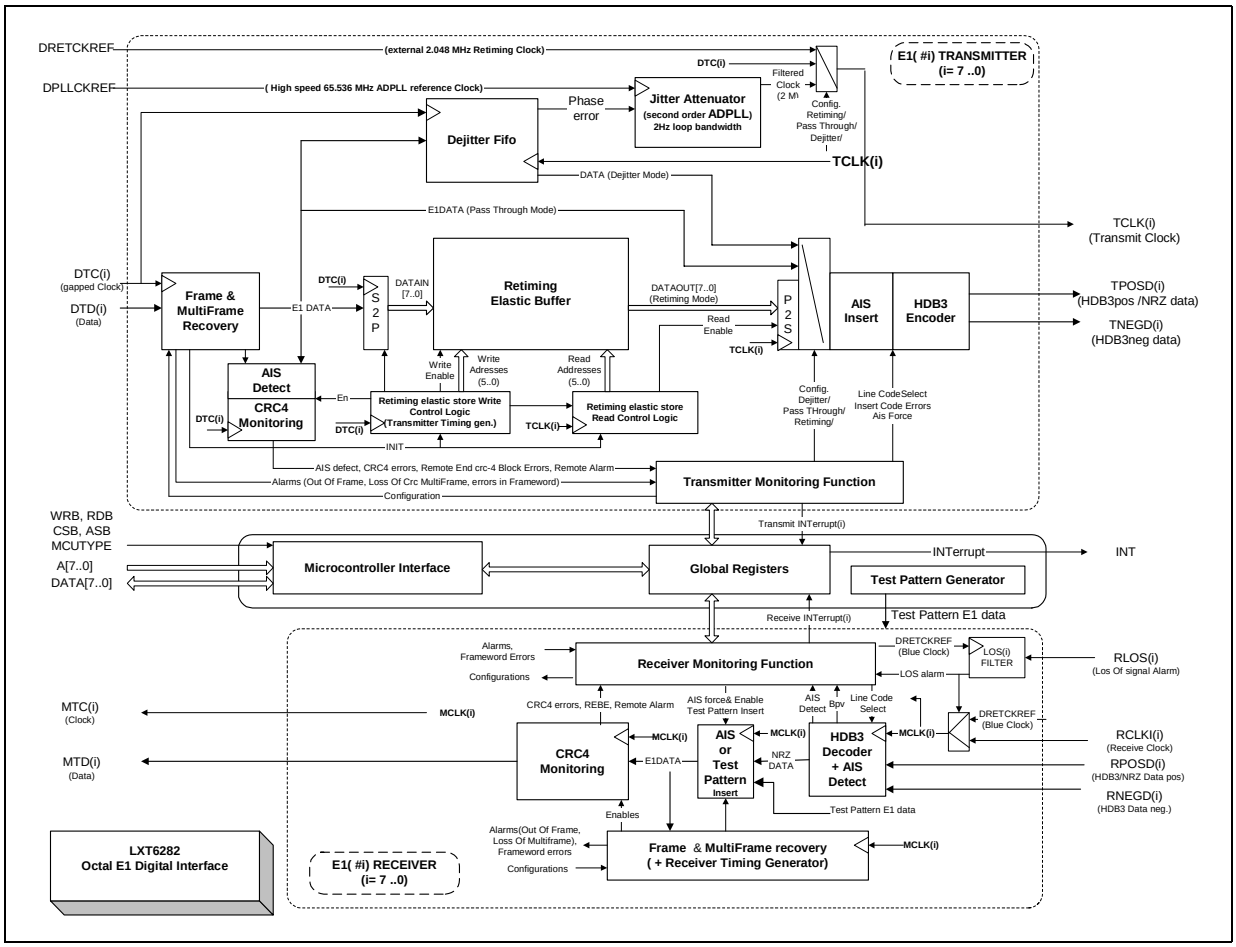
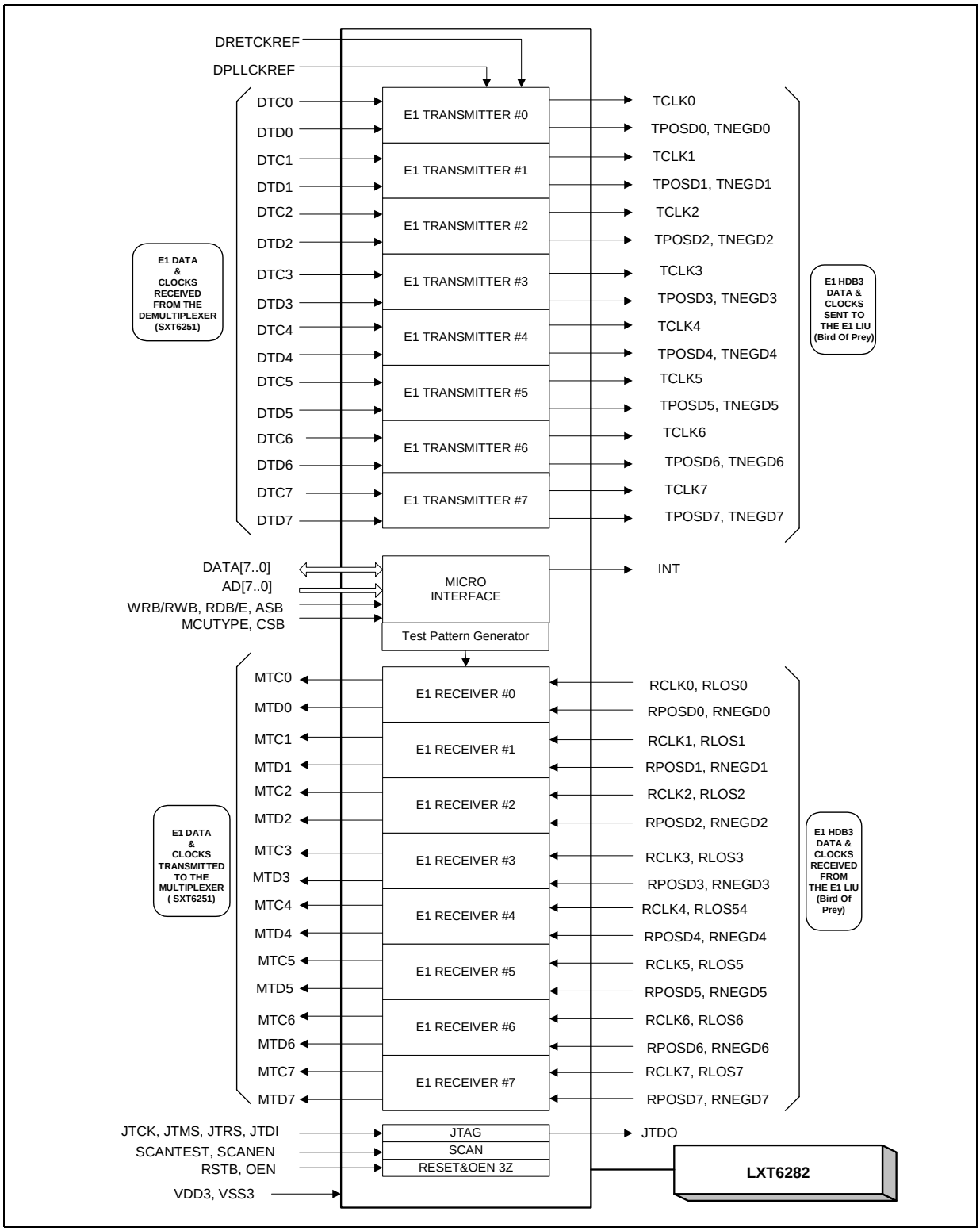
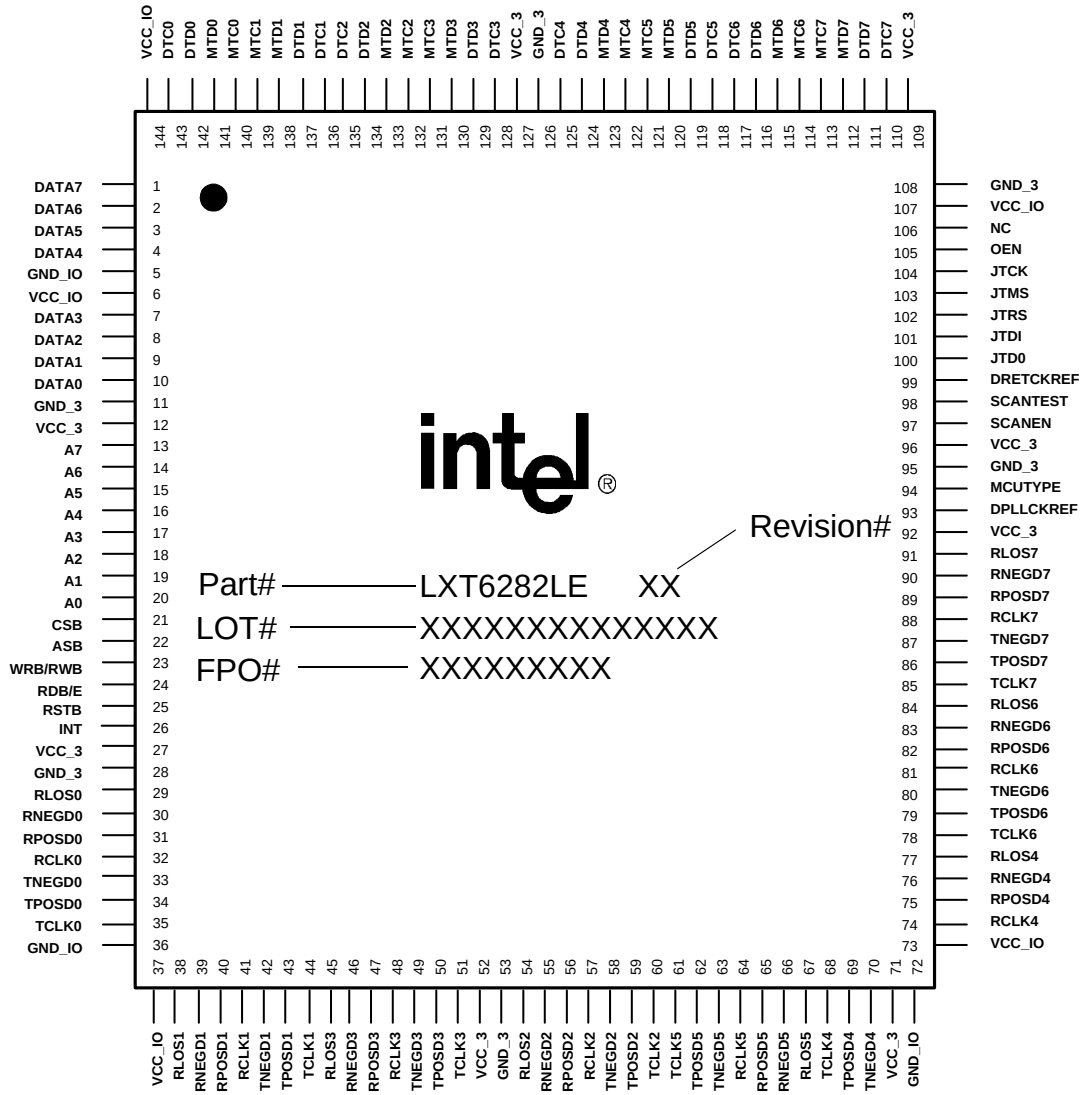


Figure 3. LXT6282 Block Diagram 2



1.0 Pin Assignments and Signal Descriptions

Figure 4. LXT6282 Pin Assignment



Package Topside Markings

Marking	Definition
Part #	LXT6282 is the unique identifier for this product family. LE indicates the family member.
Rev #	Identifies the particular silicon “stepping” — refer to the specification update for additional stepping information.
Lot #	Identifies the batch.
FPO #	Identifies the Finish Process Order.

Table 1. Signal Descriptions

Pin Name	Pin	PROP	I/O	Description
E1 Transmitters (receive side of demultiplexer)				
E1 data and clocks transmitted to the LIU				
TPOSD<7...0>	86 79 62 69 50 59 43 34	HiZ-4ma	O	**Positive HDB3 or NRZ Data Transmit outputs.** Eight E1 data channel outputs (channel<i>, i=<7..0>) at 2.048 Mbit/s, in either NRZ or HDB3 format.
TNEGD<7...0>	87 80 63 70 49 58 42 33	HiZ-4ma	O	**Negative HDB3 Data Transmit outputs.** Eight E1 data channel outputs (channel<i>, i=<7..0>) at 2.048 Mbit/s when HDB3 coding is used.
TCLK<7...0>	85 78 61 68 51 60 44 35	HiZ-8ma	O	**Transmit clock outputs.** The 2.048 MHz clock output of each of the eight independent transmitters (TCLK<i>, i=<7..0>) is to be used with the corresponding E1 data (TPOSD<i> and TNEGD<i>) signals when needed.
E1 data and clocks received from the demultiplexer				
DTD<7...0>	111 116 119 124 129 134 137 142	BUF-in	I	**Demultiplexed NRZ data inputs.** Eight E1 data channel inputs (transmitters, channel<i>, i=<7..0>) at 2.048 Mbit/s received from the demultiplexer.
DTC<7...0>	110 117 118 125 128 135 136 143	BUF-in	I	**Demultiplexed Clock inputs.** Eight E1 clock inputs (transmitters; channel <i>, i=<7..0>) at 2.048 MHz received from the demultiplexer. These clocks can be gapped due to the SDH frame structure and the justification process.
External Clock References				
DRETCKREF	99	BUF-in	I	**Demultiplexer Re-timing Clock**. This is an external **2.048 MHz reference** clock input that can be used in each E1 transmitter to retime the E1 data received from the demultiplexer (wander reduction if the E1 transmitter # i is configured in retiming mode). This clock is also used as a blue clock in each receiver to generate an AIS signal in case of RLOS.
1. Buf-in = CMOS Input buffer with switching threshold at 3.3V / 2 (V_{DD} / 2) 2. i = <7...0> which corresponds to the E1 channel number				

Table 1. Signal Descriptions

Pin Name	Pin	PROP	I/O	Description
DPLLCKREF	93	BUF-in	I	**High speed PLL clock reference**. This is an external **65.536 MHz** (+ /-50 ppm) **reference clock** that can be used in each E1 transmitter as the Digital Phase Locked Loop Clock input reference. Only needed if an E1 transmitter is configured in jitter attenuation mode.
E1 Receivers (Transmit side of multiplexer)				
E1 Data and Clocks received from the LIU				
RPOSD<7...0>	89 82 65 75 47 56 40 31	BUF-in	I	**Positive HDB3 or NRZ Data Receive.** Eight E1 data channel inputs (channel <i>, i=<7..0>) at 2.048 Mbit/s supplied by the E1 line interface unit(s), in either NRZ or HDB3 format.
RNEGD<7...0>	90 83 66 76 46 55 39 30	BUF-in	I	**Positive HDB3 Data Receive.** Eight E1 data channel inputs (channel<i>, i=<7..0>) at 2.048 Mbit/s supplied by the E1 line interface unit(s), when HDB3 coding is used. If HDB3 coding is not used, these inputs have to be grounded.
RLOS<7...0>	91 84 67 77 45 54 38 29	BUF-in	I	**Loss of Signal from the external line interface unit(s).** Eight input alarms from the E1 line interface circuits (channel<i>, i=<7..0>). RLOS alarm is active high.
RCLK<7...0>	88 81 64 74 48 57 41 32	BUF-in	I	**Receive clock inputs.** Eight receive E1 clocks at 2.048 MHz provided by the E1 line interface unit(s).
E1 Data and Clocks transmitted to the Multiplexer				
MTD<7...0>	112 115 120 123 130 133 138 141	HiZ-4ma	O	**NRZ Data outputs.** Eight E1 data channel outputs of the receivers (channel<i>, i=<7..0>) at 2.048 Mbit/s transmitted to the multiplexer.

1. Buf-in = CMOS Input buffer with switching threshold at 3.3V / 2 (V_{DD} / 2)
2. i = <7...0> which corresponds to the E1 channel number

Table 1. Signal Descriptions

Pin Name	Pin	PROP	I/O	Description
MTC<7...0>	113 114 121 122 131 132 139 140	HiZ-8ma	O	**Clock outputs.** Each one of these eight 2048 MHz clock outputs of the receivers is to be used with the corresponding E1 data (MTD<i>, i=<7..0>) signal transmitted to the multiplexer, if needed.
Microprocessor Bus				
A<7..0>	13-20	BUF-in	I	**Address Bus 8 bits.** Eight-bit address port for data, command and status addresses.
DATA<7..0>	1-4 7-10	BUF-in/ Hiz-10ma	I/O	**Data Bus 8 bits.** Eight bits I/O to read and write data, commands and status to and from the device.
WRB/RWB	23	BUF-in	I	Write-Bar Intel; Read/Write Bar Motorola
RDB/E	24	BUF-in	I	Read-bar Intel; Enable Motorola
INT	26	Hiz-4ma	O	Interrupt request. Active low
CSB	21	BUF-in	I	**Chip Select**. Active low
ASB	22	BUF-in	I	**Address Strobe Enable.** Indication that the address on the address bus is valid. Active high.
MCUTYPE	94	BUF-in	I	**Motorola/Intel Interface mode select**. A High indicates a Motorola and a Low an Intel Microprocessor.
RSTB	25	BUF-in (60K pull up)	I	**Chip Master Reset.** A low will reset all registers to default values.
OEN	105	BUF-in (60K pull up)	I	**Master chip output enable.** Active high (a low will set all outputs and bidirectionnal to 3Z)
JTAG and SCAN test ports				
JTCK	104	BUF-in	I	**JTAG Clock.** Clock for all boundary scan circuitry.
JTMS	103	BUF-in (60K pull up)	I	**JTAG Test Mode Select.** Determine state of TAP controller.
JTRS	102	BUF-in (60K pull down)	I	**JTAG Reset.** Active low.
JTDI	101	BUF-in (60K pull up)	I	**JTAG Data Input.** Input signal used to shift in instructions and data.
JTDO	100	2mA	O	**JTAG Data Output.** Output signal used to shift out instructions and data.
SCANTEST	98	BUF-in (60K pull up)	I	**Scan test mode** (active low)
SCANEN	97	BUF-in (60K pull up)	I	**Scan enable** (active low)

1. Buf-in = CMOS Input buffer with switching threshold at 3.3V / 2 (V_{DD} / 2)
2. i = <7...0> which corresponds to the E1 channel number

Table 1. Signal Descriptions

Pin Name	Pin	PROP	I/O	Description
Power Supply				
VCC_3	12, 27, 52, 71, 92, 96, 109, 127			**3.3 V Core supply.** (8 pins)
GND_3	11, 28, 53, 95, 108, 126			**GND-Core**. Ground for 3.3 V supply. (6 pins)
VCC_IO	6, 37, 73, 107, 144			**3.3V I/O ring supply.** (5 pins)
GND_IO	5, 36, 72			**GND-I/O Ring**. Ground for I/O supply. (3 pins)
NC	106			This pin should be left unconnected.

1. Buf-in = CMOS Input buffer with switching threshold at 3.3V / 2 (V_{DD} / 2)
2. i = <7...0> which corresponds to the E1 channel number

2.0 General Functional Description

2.1 Introduction

The LXT6282 integrates eight E1 transmitters and eight E1 receivers that can operate independently. It performs jitter/wander filtering, CRC-4 monitoring and HDB3 encoding/decoding. It also includes a Motorola/Intel compatible microcontroller interface for alarm and performance monitoring.

The following description follows the simplified block diagram (refer to Figure 2 and Figure 3).

2.2 Transmitter Description

The eight fully independent E1 transmitter blocks can be configured for different applications.

Each transmitter input interface accepts an NRZ encoded E1 signal input (DTDx) and clock input (DTCx). The transmission frame structure and the justification process allow the incoming clock (DTCx) to be gapped and jittered. The E1 signal (DTDx) may have a CRC-4 multiframe structure according to recommendation ITU G.704 (refer to Table 2).

The DTDx data is fed to the frame/multiframe recovery block. This block synchronizes the Transmitter Timing Generator to the incoming E1 data frame and provides Out Of Frame (OOF) and Loss Of Multiframe (LOMF) alarm indications. Remote End Block Errors (REBE) are also counted and stored in a set of microprocessor-accessible counters. The Remote alarm is monitored (but not inserted) for status changes.

Once frame synchronization is achieved, any errors in the frame word are detected, counted and stored in a set of microprocessor-accessible counters. A CRC-4 calculation is also performed over the multiframe and compared with the incoming CRC-4 value. Again, any errors are counted and stored in a set of microprocessor-accessible counters.

An AIS defect at the DTDx input is also detected and monitored. All framing, multiframing and CRC-4 monitoring functions can be bypassed if not needed.

The transmitter can be configured to operate in three different modes:

2.2.1 Dejitter Mode

In Dejitter mode, the transmitter filters jitter and eliminates gaps in the incoming E1 clock and data.

The incoming E1 data is fed into a 32-bit FIFO. The write clock of the FIFO is the gapped input clock (DTC), which is also fed to the jitter attenuator consisting of a second order All Digital Phase Locked Loop (ADPLL) having a 2.0 Hz loop bandwidth. The filtered clock output of the ADPLL is the read clock of the FIFO. The transmitter can be configured to insert an AIS signal (data “all one” + blue clock) automatically when the FIFO overflows, underflows or the PLL is unlocked.

The degapped E1 output is emitted as NRZ data on TPOSD, or as HDB3 encoded data on TPOSD and TNEGD. The dejittered and degapped output clock of each transmitter is emitted on TCLK at the same frequency as the DTC input clock (TCLK clock is the ADPLL output). This working mode is fully transparent - no data is lost or added in the transmission.

2.2.2 Retiming Mode

In the Retiming mode, the transmitter eliminates wander and jitter in the incoming clock (DTC).

Incoming E1 data is converted to a byte parallel format and fed into a two frame-wide elastic buffer. The write and read control logic of this elastic store are initialized by the E1 frame acquisition process. The data is read out of the elastic buffer using an external clock reference input (DRETCKREF). DRETCKREF may or may not be at the same frequency as the DTC clock input. If the read and write frequencies are different, the elastic store will periodically overflow or underflow. In either case, the read control logic will process a controlled slip of one complete frame in order to re-center the elastic buffer. This will result in the loss or repetition of one complete E1 frame.

The retiming FIFO may also operate on an un-framed 2.048 Mbit/s signal busy setting the transmitter to “Retiming Test Mode.” In this case, the read and write control logic of the elastic store is in full free running mode and independent of the framing algorithm. As the data is supposed to be un-framed in this test mode, CRC-4 error monitoring is not valid.

The output from the elastic buffer is converted to a serial format and emitted as NRZ data on TPOSD, or output as HDB3 encoded data on TPOSD and TNEGD, at the TCLK clock rate that is synchronous with the DRETCKREF clock input.

This working mode may be non-transparent. It can handle a maximum of 26 time slots (208 UI) of wander or low frequency jitter before a frame slip occurs. This controlled frame slip assures that the time-slot assignment is not lost at the output of the chip. All the jitter and wander due to the multiplexing/demultiplexing process in the transmission is eliminated.

2.2.3 Pass-Through Mode

In the Pass-through mode no dejitter or retiming is performed on the input data.

The input clock (DTC) is shunted to the output clock (TCLK). CRC-4 monitoring and HDB3 encoding can be performed if so configured.

2.3 Receive Data Flow Description

The Receiver consists in eight fully independent E1 receiver blocks.

Each receiver input interface includes an NRZ encoded E1 signal input on RPOSDx or HDB3 encoded data on RPOSDx and RNEGDx, a serial clock RCLKx, and a Loss Of Signal (RLOSx) alarm indication coming from the output of an E1 Line Interface Unit Receiver. The E1 input data RPOSD/RNEGD may have a CRC-4 multiframe structure according to recommendation ITU G.704 (refer to Figure 5). HDB3 code errors (Bipolar Violations) are detected and stored in a set of microprocessor-accessible counters.

An AIS defect is detected according to recommendation ITU G.775 for the E1 incoming signal after HDB3 decoding, and the corresponding alarm is accessible to the microprocessor.

If the Loss Of Signal alarm is active, the receiver may insert an AIS signal (all ones in the data), using the DRETCLK clock reference input as a blue clock.

Data is fed to the framing/multiframing block that synchronizes the Receiver Timing Generator to the incoming E1 data frame, and provides Out Of Frame (OOF) and Out Of Multiframe (OOMF) alarm indications. Once the frame synchronization is acquired, frame word errors are detected, counted and stored in a set of microprocessor accessible counters. Remote End Block Errors (REBE) are also counted and stored in a set of microprocessor-accessible counters. The Remote alarm is monitored (but not inserted) for status changes.

A CRC-4 calculation is also performed over the multiframe and compared to the incoming CRC-4 value. Again, any errors are counted and stored in a set of microprocessor- accessible counters.

The E1 signal is emitted as NRZ data on MTD and clock on MTC.

All the AIS, framing, multiframing and CRC-4 monitoring functions can be independently bypassed in each receiver if not needed.

For testing and maintenance purposes, the receiver can be set via the microprocessor as a sequence pattern generator on MTD and MTC data and clock output pins (framed or unframed PRBS sequence).

3.0 Functional Description Per E1 Channel

3.1 Transmitter Default Operation

3.1.1 Data Input Interface

The relative phase between E1 NRZ data (on DTDx pin) and clock (on DTCx pin) inputs can be configured via microprocessor (DTDx data input may be sampled in the transmitter by the rising or falling edge of the input clock DTCx: see global register AFH).

3.1.2 Frame Alignment

The framing method follows the rules set forth in CCITT/ITU recommendations G.704 and G.706.

The frame alignment circuit searches for the first frame alignment signal (“0011011” frameword, bit 2-8 in time slot 0) within the incoming E1 data (DTDx). Once detected, the frame acquisition counter is set to check bit 2 in the non-frame alignment signal (time slot 0) of the next frame. If bit 2 is one, a second un-errored frame alignment signal is checked one frame later. Next, the timing generator counters are set and frame synchronization is declared. If bit 2 in the non-frame alignment signal is not one, or the frame alignment signal is not found in the third frame, then a new search is initiated.

If CRC-4 multiframing is configured (see paragraph below and Figure 5), two correct multiframes within 8 ms are used for immunity against false framing.

Once the E1 frame is synchronized, the framer will go out of synchronization after three consecutive frame alignment signals containing single or multiple errors are received. In addition, it is possible to configure the framing algorithm via register 0FH, so that the framer will also go out of synchronization if three consecutive bit 2 of the non- frame alignment signal are not one. A 12-bit microprocessor-accessible counter can be configured (see global register 0FH) to count either the errored FAS, the errored NFAS, or the FAS *and* the NFAS with single or multiple errors.

If the CRC-4 multiframing is not configured, it is possible to strengthen the frame acquisition algorithm to five consecutive frames (three FAS and two NFAS with no error) by programming global register 0FH. This will minimize the probability of incorrect synchronization. In this case, the frame desynchronization algorithm is also strengthened to four consecutive frame alignment signals received that contain single or multiple errors, or four consecutive bit 2 of the non-frame alignment signal not one (if so configured).

The Out Of Frame (OOF) alarm status is accessible to the microprocessor via the status registers.

3.1.3 CRC-4 Multiframe Alignment

CRC-4 multiframe alignment is used for immunity against false framing and also provides non-intrusive error monitoring capabilities for the E1 payload.

When CRC-4 is selected as the E1 framing option the transmitter attempts to synchronize to a 16 frame multiframe structure illustrated in Table 1.

The multiframe consists of 16 basic E1 frames (eight double frames), numbered 0-15, that are further divided into two 8-frame sub-multiframes (SMF I and SMF II). Bit 1 of each frame is used to transport the Cyclic Redundancy Check bits, multiframe sync word and Remote End Block Errors (REBE) in the following manner:

- In the four frames of each SMF that include the FAS word, bit 1 contains the four CRC bits, numbered C1-C4.
- In the eight frames of the entire multiframe that include the NFAS word, bit 1 contains a 6-bit CRC-4 multiframe alignment signal as well as two REBE indication bits.

Table 2. Multiframe TimeSlot 0 Signaling Description

	Frame #	1	2	3	4	5	6	7	8
SMF I	0	C1	0	0	1	1	0	1	1
	1	0	F	A	Sa4	Sa5	Sa6	Sa7	Sa8
	2	C2	0	0	1	1	0	1	1
	3	0	F	A	Sa4	Sa5	Sa6	Sa7	Sa8
	4	C3	0	0	1	1	0	1	1
	5	1	F	A	Sa4	Sa5	Sa6	Sa7	Sa8
	6	C4	0	0	1	1	0	1	1
	7	0	F	A	Sa4	Sa5	Sa6	Sa7	Sa8

	Frame #	1	2	3	4	5	6	7	8
SMF II	8	C1	0	0	1	1	0	1	1
	9	1	F	A	Sa4	Sa5	Sa6	Sa7	Sa8
	10	C2	0	0	1	1	0	1	1
	11	1	F	A	Sa4	Sa5	Sa6	Sa7	Sa8
	12	C3	0	0	1	1	0	1	1
	13	RE1	F	A	Sa4	Sa5	Sa6	Sa7	Sa8
	14	C4	0	0	1	1	0	1	1
	15	RE2	F	A	Sa4	Sa5	Sa6	Sa7	Sa8

NOTES:
RE: Remote End CRC-4 Block Error indicator bits (REBE)
Sa4-Sa8: Spare bits for national use
C1-C4: CRC-4 Bits
A: Remote Alarm Indication
F: NFAS Framing Bit (normally = 1 to avoid spurious frame sync)

After FAS/NFAS frame synchronization is acquired, the CRC-4 multiframe alignment is declared when two correct CRC-4 MultiFrame Alignment signals are detected within 8 ms (one complete multiframe lasts two ms). If CRC-4 multiframe alignment is not achieved within 8 ms after frame alignment, a new search will be initiated for valid FAS/NFAS.

Once the CRC-4 Multiframe is acquired, a Loss Of CRC-4 Multiframe (LOMF) is declared when the frame synchronization is lost, or the CRC-4 error rate is greater or equal to 915 block/s. The Loss Of CRC-4 Multiframe alarm is accessible to the microprocessor via the status registers.

3.1.4 AIS Detection

An AIS defect is detected in the DTDx input data when the incoming signal has two or less ZEROs in each of two consecutive double frame periods (512 bits). This defect alarm is cleared when each of two consecutive double frame periods contain three or more ZEROs or when the frame alignment signal has been found.

The AIS defect alarm status is accessible to the microprocessor via the status registers.

3.1.5 CRC-4 Multiframe Monitoring

3.1.5.1 CRC-4 Block Errors Calculation

When the CRC-4 multiframe is synchronized, the CRC-4 bits are calculated internally based on a sub-multiframe (as specified in recommendation ITU G704) and compared to the incoming CRC-4 value in the next sub-multiframe. The block errors are stored in a 10-bit counter that can be read by the microprocessor. A maskable interrupt is provided for counter overflows.

3.1.5.2 Remote End Block Errors

Two bits per multiframe (RE1 and RE2) are allocated for the CRC-4 Remote End Block Errors (REBE) indication. These errors are counted and stored in a 10 bit counter that can be read by the microprocessor. A maskable interrupt is provided for counter overflows.

3.1.5.3 Remote Alarm

The Remote alarm bit (bit 3 in the NFAS) is used to tell the transmit end that the receive end has detected a loss of signal or loss of frame. The remote alarm is filtered for three consecutive frames before being declared a new value. Changes in its status is indicated to the microprocessor via a maskable interrupt.

3.1.6 Retiming Elastic Store Operation

This block is used to eliminate the wander and the jitter in the incoming clock and data (DTC and DTD). It may be non-transparent for the incoming data (see frame slips, below), but it keeps the time slot alignment in the E1 frame.

The incoming data is converted to a byte parallel format and clocked into a 2 frame wide elastic buffer. The write and read control logic of this elastic store are initialized by the frame synchronization process. Once the frame is acquired, the Elastic Store is centered and the data is read out of the elastic buffer and re-converted to a serial format using an external system clock reference input (DRETCKREF).

If the incoming clock DTC and the system clock DRETCKREF are synchronous and phase-locked (i.e., in the case of a synchronous network), the elastic buffer will never overflow or underflow.

If these two clocks, (DRETCKREF and DTC) do not have the same frequency, the elastic store will overflow or underflow repetitively, depending on the frequency offset.

If the read system clock (DRETCKREF) frequency is higher than the write incoming clock (DTC) frequency, then when the FIFO is close to underflowing, the read control logic will perform a slip of one complete frame. This results in the repetition of the last received frame (“positive slip”).

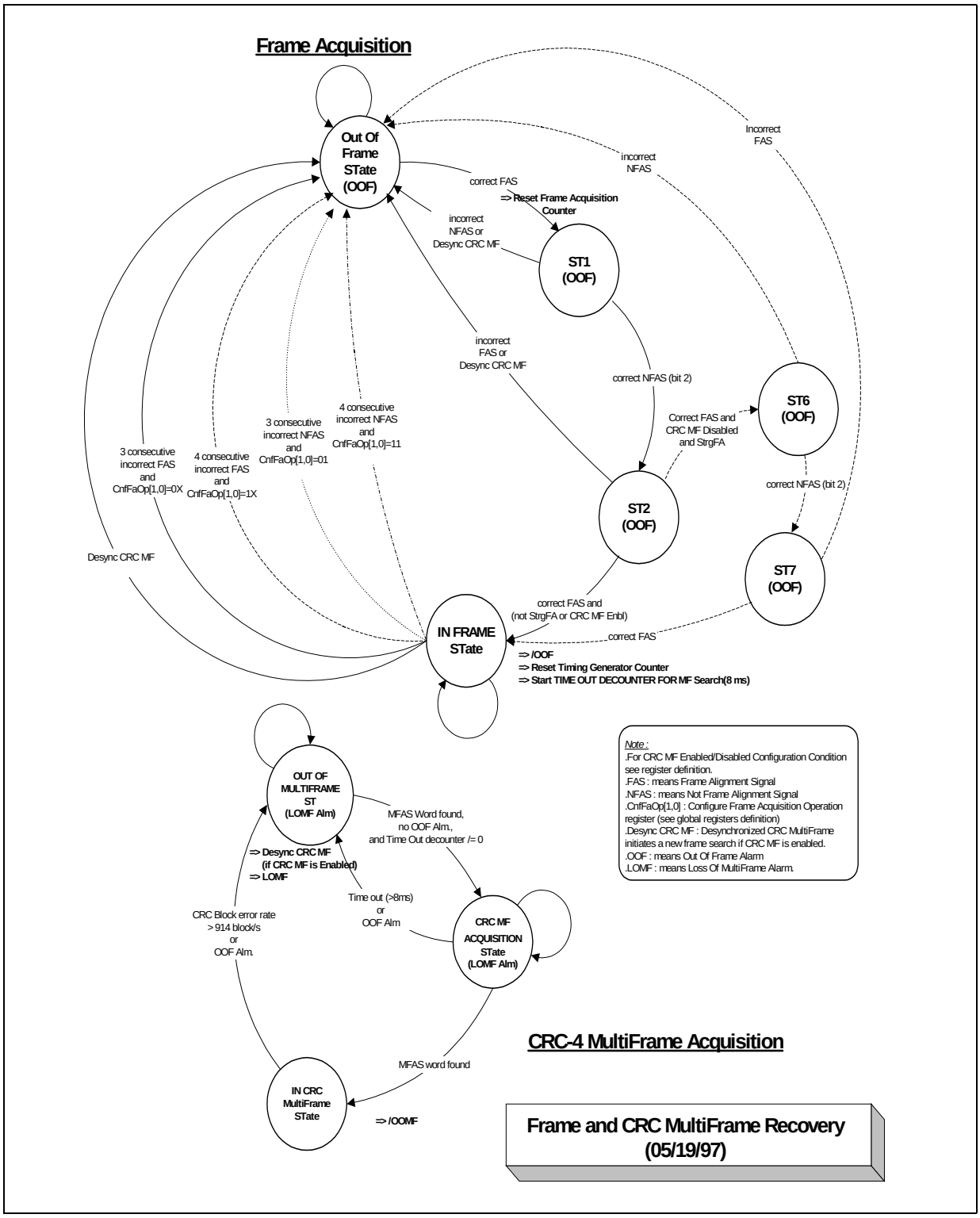
If the read system clock (DRETCKREF) frequency is lower than the write incoming clock (DTCx) frequency, then when the FIFO is close to overflow, the read control logic will perform a slip of one complete frame. This results in the loss of the last received frame (“negative slip”).

Positive and negative slips in the elastic store are indicated via two maskable interrupts, and counted in two different 4-bit counters accessible via the microprocessor. A maskable interrupt is provided to indicate counter overflows.

For FIFO and Wander monitoring, or delay calculation, the relative difference between FIFO write and read pointers is indicated in register iCH (6 bits used), accessible via the microprocessor.

For testing and debugging, this two-frame-wide elastic buffer may be reset via the microprocessor to its center point (see register iEH).

Figure 5. Frame and Multiframe Acquisition



A maskable interrupt is also provided to indicate the inoperability of the elastic store. This alarm indicates that the clock frequencies are so different that slippage is continual.

By setting a special configuration in register iEH, the transmit retiming 2 frame-wide elastic store (512 bits) may be used to retime an un-framed 2.048 Mbit/s signal for wander elimination. In this case, the read and write pointer of the FIFO are independent of the framing algorithm and operate in complete free running mode, but the CRC-4, REBE and remote alarm monitoring are un-valid, as the 2.048 Mbit/s input signal is considered un-framed.

The retiming elastic store can be bypassed by using the dejittering circuitry or configuring the data path in pass-through mode (see register iEH).

3.1.7 De-jittering Circuitry

The de-jittering circuitry consists of the dejitter FIFO and a jitter attenuator or phase lock loop. This function can be bypassed by using the retiming function or configuring the data path in pass-through mode (see register iEH).

The dejitter FIFO is a 32-bit asynchronous FIFO, whose write clock is the input gapped clock (DTCx) at 2.048MHz +/- 50 ppm average frequency, and whose read clock is the phase-locked and filtered output of the jitter attenuator (the ADPLL).

The jitter attenuator is a second order All Digital Phase Lock Loop with a 2.0 Hz loop bandwidth. The reference and sample clock of the digital PLL is provided by the high speed clock input pin DPLLCKREF at 65.536 MHz +/- 50 ppm. DPLLCKREF reference clock is provided by an external crystal oscillator. When the de-jittering circuitry is not selected in a transmitter, the high speed clock is shut down in this specific transmitter to save power consumption.

A maskable interrupt is provided to indicate dejitter FIFO overflows.

3.1.8 AIS Signal Insertion

An AIS signal (unframed all ones signal) can be generated using the external clock input DRETCKREF at 2.048 MHz +/- 50 ppm (if the transmitter is configured to operate in retiming or passed through mode) or using the high-speed ADPLL reference clock at 65.536 MHz +/- 50 ppm divided by 32 (if the transmitter is configured to operate in dejitter mode), as a blue clock on the E1 transmitter output.

When the transmitter is configured to operate in dejitter mode, an AIS signal may be automatically hardware inserted when enabled (see registers iEH and AFH), if the dejitter ADPLL is unlocked and the FIFO crashed. In this case, the AIS blue clock is derived from the high-speed PLL reference clock (+/- 50 ppm), and the transition from non-AIS clock to AIS blue clock (and the inverse) is always smooth. The AIS state is accessible to the microprocessor via the global status register 9FH.

3.1.9 Line Coding HDB3

The serial E1 output is a HDB3 signal output on TPOSD and TNEGD. The output clock is TCLK (2.048 MHz). For testing, it is possible to insert (microprocessor configurable) BPV errors on TPOSD and TNEGD output data. A single code error, one error every 1024 bits (BER 10-3), one error every multiframe, or one error every second may be inserted.

If the HDB3 encoder is not used, TPOSD is used as an NRZ output.

The relative phase between output data and clock can be configured via microprocessor (TPOSDx/ TNEGDx data outputs emitted on rising or falling edge of the output clock TCLKx: see global register AFH).

Depending on the transmitter configuration, TCLK transmit clock output may be provided by different sources:

Table 3. Transmitter clock output scheme

TCLK clock sources	Synchronous with	Clock source
Retiming Mode (No AIS or AIS)	DRETCKREF input	DRETCKREF
Dejitter Mode (No AIS)	DTC input	ADPLL filtered output
Dejitter Mode (AIS insert)	DPLLCKREF input/32	DPLLCKREF/32
Pass Through Mode (No AIS)	DTC input	DTC
Pass Through Mode (AIS insert)	DRETCKREF input	DRETCKREF

3.1.10 Receiver Operation

3.1.10.1 Line decoding HDB3

The HDB3 decoder is microprocessor selectable. When selected, this block accepts an HDB3 encoded E1 signal via data inputs RPOSDx and RNEGDx and clock RCLKx. A bipolar violation (or code error) detector is implemented in the HDB3 decoder. The Bipolar Violation (BPV) Errors Detector can be configured for all the E1 HDB3 receivers via the microprocessor. The detector can:

- be disabled
- detect two consecutive ‘1’s’ with the same polarity (*except when it is used as part of a valid HDB3 substitution*)
- detect BPV that do not alternate polarity (recommendation ITU O161)
- detect two consecutive ‘1’ with the same polarity, *or* BPV that do not alternate polarity, *or* four consecutive ‘0’ badly encoded.

BPV errors are accumulated in a 16-bit counter that can be read by the microprocessor. A maskable interrupt is provided to indicate counter overflows.

If the HDB3 decoder is not used, the E1 NRZ data is input on RPOSD. In this case, RNEGD input pin has to be grounded, and the BPV error detection is invalid.

The relative phase between E1 data (on RPOSDx/RNEGDx pins) and clock (on RCLKx pin) inputs can be configured via microprocessor (RPOSDx/RNEGDx data inputs may be sampled, in the transmitter, by rising or falling edge of the input clock RCLKx: see global register AFH).

3.1.10.2 AIS Detection

After HDB3 decoding, an AIS detection is performed on the incoming data according to recommendation ITU G.775.

AIS defect alarm is declared when each of two consecutive double frame periods (512 bits) has two or less ZEROs, and the alarm is cleared when three or more ZEROs or when the Frame Alignment Signal has been found in each of two consecutive double frame periods.

The AIS defect alarm status is accessible to the microprocessor via the status registers.

3.1.10.3 AIS Insert/LOS Alarm filtering

This block includes a filter for Loss Of Signal Alarm input on RLOS pin from the external LIU. The filtering on the LOS can be integrated over 128 clock cycles or disabled via microprocessor.

An AIS signal (unframed all ones in the data) can be inserted on the incoming data RPOSD and RNEGD after decoding in case of LOS alarm. DRETCKREF clock reference input (2.048 MHz +/- 50 ppm) may be used as a blue clock for AIS generation, if the receiver is so configured. The AIS insert can also be disabled or forced via microprocessor (see configuration register jEH). The AIS state for every receiver is reported in the global status registers.

3.1.10.4 Frame Alignment/Out Of Frame Alarm

The framing method follows the rules set forth in CCITT/ITU recommendations G.704 and G.706 and is the same as the one described in the transmitter. Refer to Section 3.1.2, “Frame Alignment” on page 18 and Figure 5 on page 22.

Out Of Frame status changes are indicated via a maskable interrupt, and errored FAS/NFAS (see global configuration register 0FH) are counted via a 13- bit microprocessor-accessible counter.

3.1.10.5 CRC-4 Multiframe Alignment/Out of CRC Multiframe Alarm

The multiframe acquisition is the same as in the transmitter. Refer to CRC-4 Multiframe Alignment on page 14.

Loss Of CRC-4 Multiframe status changes are indicated via a maskable interrupt.

3.1.10.6 CRC-4 Multiframe Monitoring

CRC-4 Block Errors Calculation

Once the CRC-4 multiframe is acquired, the CRC-4 bits are calculated internally based on a sub-multiframe (as specified in recommendation ITU G704) and compared to the incoming CRC-4 value in the next sub-multiframe. The block errors are accumulated in a 10-bit counter that can be read by the microprocessor. A maskable interrupt is provided to indicate counter overflows.

Remote End Block Errors

Two bits per multiframe (RE1 and RE2) are allocated for the CRC-4 Remote End Block Error (REBE) indication. REBEs are accumulated in a 10-bit counter that can be read by the microprocessor. A maskable interrupt is provided to indicate counter overflows.

Remote Alarm

The Remote alarm bit (bit 3 in the NFAS) is used to tell the transmit end that the received end has detected a loss of signal or loss of frame. The remote alarm is filtered for three consecutive frames before being declared a new value. A change in its status is indicated to the microprocessor via a maskable interrupt.

Output Interface

NRZ receive data and clock are emitted on MTDx and MTCx pins. MTCx clock is synchronous with an RCLKx input clock or DRETCKREF blue clock if AIS is inserted in the receiver or if in Autotest Mode. The relative phase between output data and clock can be configured via the microprocessor (MTDx data outputs emitted on the rising or falling edge of the output clock MTCx: see global register AFH).

3.1.10.7 Test Pattern Generator for Autotesting/Maintenance

CRC-4 E1 Framed Test Pattern

An internal E1 framed pattern generator may be enabled via the microprocessor for autotesting and maintenance purposes. The sequence consists of an E1 CRC-4 framed signal with the FAS, NFAS, MFAS and CRC-4 bits in the time slots 0 and a PRBS 2E15-1 sequence in the time slots 1 ->31.

If enabled (see registers 1FH and jEH), the E1 framed test pattern sequence is sent to the receiver input and then emitted on MTD data output pin, with the associated DRETCKREF blue clock emitted on MTC clock output pin. So, by looping back externally, the MTC/MTD output signals to the DTC/DTD input signals, the chip can be autotested without any external test equipment.

PRBS Unframed Test Pattern

If enabled (see registers 1FH and jEH), the internal test pattern generator can also generate the standard pseudo-random (2E15-1 sequence) unframed test signal used for E1 jitter analysis (Recommendation ITU-T O171) emitted on MTD data output pin, with the associated DRETCKREF blue clock emitted on MTC clock output pin.

3.1.11 MICROCONTROLLER INTERFACE

This section contains a description of the asynchronous microprocessor interface. A microprocessor should be connected to the LXT6282 for reading and writing data via the microprocessor interface pins.

The microprocessor interface is a generic asynchronous interface, including an address bus (A [7..0]), data bus (DATA [7..0]) and handshaking pins (WRB/RWB, RDB/E, CSB, and ALE). The MCUTYPE input pin indicates the type of microprocessor interface to be used – Intel or Motorola. There is also an INT output pin that indicates status changes to the microprocessor.

This interface has the same features as Intel’s LXT6051 and LXT6251A chips.

3.1.11.1 Intel Interface

The Intel interface is indicated by driving the MCUTYPE input pin LOW. It uses the WRB/RWB input pin as WRB and the RDB/E input pin as RDB.

A read cycle is indicated to the LXT6282 by the uP forcing a LOW on the RDB pin with the WRB pin held HIGH.

A write cycle is indicated to the LXT6282 by the uP forcing a LOW on the WRB pin with the RDB pin held HIGH.

Both cycles require the CSB pin to be LOW and the uP to drive the A[7..0] address pins. In the case of the write cycle, the uP is also required to drive the DATA [7..0] data pins. In the case of the read cycle, the LXT6282 drives the DATA [7..0] data pins.

When a multiplexed data/address bus is used, the falling edge of the ALE input latches the address provided on the muxed bus (the muxed bus will be connected to both the A[7..0] and DATA[7..0]). If the address and data are not multiplexed the ALE pin should be tied HIGH.

3.1.11.2 Motorola Interface

The Motorola interface is indicated by driving the MCUTYPE input pin HIGH. It uses the WRB/RWB input pin as RWB and the RDB/E input pin as E.

A read cycle is indicated to the LXT6282 by the uP forcing a HIGH on the RWB pin. A write cycle is indicated to the LXT6282 by the uP forcing a LOW on the RWR pin.

A LOW on the E input initiates both cycles. The E input is connected to the E output from the Motorola uP and is typically a 50% duty cycle waveform with a frequency derived from the uP clock.

Both cycles require the CSB pin to be LOW and the uP to drive the A[7..0] address pins. In the case of the write cycle, the uP is also required to drive the DATA [7..0] data pins. In the case of the read cycle, the LXT6282 drives the DATA [7..0] data pins.

When a multiplexed data/address bus is used, the falling edge of the ALE input latches the address provided on the muxed bus (the muxed bus will be connected to both the A[7..0] and DATA[7..0]). If the address and data are not multiplexed the ALE pin should be tied HIGH.

3.1.12 Iinterrupt Handling

3.1.12.1 Interrupt Sources

There are three types of interrupt sources:

- Status change of a monitoring process: For example, the LXT6282 monitors the incoming E1 frame for the correct framing pattern and updates the OofSt and LofSt status bits to indicate presence or absence of Out Of Frame and Loss Of Frame conditions. When the value of these status bits change an interrupt is generated if enabled.
- Event Occurrence: For example, positive and negative slips as well as FIFO overflows are considered “events” and can generate interrupts if enabled.
- Counter overflows: For example, the LXT6282 monitors the E1 frame structure for framing errors. These errors are recorded in a counter whose overflow can cause an interrupt if enabled.

3.1.12.2 Interrupt Enables

In order for an interrupt source to affect the state of the INT output pin its associated interrupt enable bit must be SET. The setting (whether it is 0 or 1) of the interrupt enables does not affect the updating of the status registers or counters.

Assuming the interrupt enable for a particular interrupt source is SET and the interrupt source is active, its interrupt bit will be SET. The primary difference between each interrupt type is the way its respective interrupt bit is cleared.

3.1.12.3 Interrupt Clearing

In the discussion below it is assumed that the example interrupt sources have their interrupt enable bits SET.

Status change interrupt sources have their interrupt bits cleared when their status is read. For example, say the OofSt bit changes from zero to one (in frame to out of frame). Its interrupt bit is SET by this event. When the microprocessor reads the register containing the OofSt bit its interrupt bit will be CLEARED. If the OofSt bit subsequently changes from one to zero (out of frame to in frame) again its interrupt bit is SET by this event and then CLEARED when the status is read.

The interrupt register can be read again only after three interval clock cycles (1.47) have completed since it has been cleared (by reading its associated status registers).

It should be noted that updates to status bits are not affected by the interrupt bit state. For example, the OofSt bit could change from a one to zero (generating an interrupt) and then before the microprocessor reads OofSt it could change back to one. This would have no affect on its interrupt bit since it would already be SET. When the microprocessor reads the OofSt bit it would read a one.

Both event interrupts and counter overflow interrupts are cleared when the interrupt register containing these bits is read (since event and counters do not have any associated status registers).

3.1.12.4 Status Registers Access

Due to the asynchronous nature of the microprocessor interface and timing differences during interrupt bit updates, it is possible that a status bit change can fail to SET its associated interrupt bit if the AlmUpdDsbl bit is not SET during a read of the status registers by the microprocessor. This situation is very difficult to achieve however, it can happen.

For this reason we encourage programmers to SET the AlmUpdDsbl bit before accessing the status registers during alarm processing. This effectively locks out internal processes that wish to access the status and interrupt bits during the time that the microprocessor is accessing these bits. After the microprocessor is done accessing the status registers it should CLEAR the AlmUpdDsbl bit so that internal processes may again update the status and interrupt bits.

3.1.12.5 Counter Reading

Counters are read by first buffering their contents and then reading the buffer. They can be individually buffered or group buffered. They are group buffered by writing to register BfrAllCntrs (5FH). They are individually buffered by writing to the most significant byte of a particular buffer. After buffering the counter, the contents of the buffer are read at the address specified in the register definition.

For example, to read the contents of the transmitter #1 FrameWord counter a write to register 07H will buffer only the contents of transmitter #1’s frame word counter. A read of registers 06H and 07H will give the counter value. Alternatively, all of the frame word counters for all 8 transmitters and receivers can be buffered by writing a 02H to register 5FH.

A counter can be read only after three interval clock cycles (1.47) have completed since it has been buffered (previous write operation. (JCC)

4.0 Microprocessor Register Description

The address mapping (8 address bits) is the following:

- addresses 0FH -> AFH: Global registers
- addresses i1H -> iEH: transmitter registers (i = {0 to 7} and i = E1 channel number)
- addresses j1H -> jEH: receiver registers (j = {8 to 15} and (j-8) = E1 channel number)

Address	Mnemonic	Register Name	Type	Page #
Global Registers				
0FH	GLOP_CONF0	Operational Configuration 0	R/W	25
0FH	GLOP_CONF1	Operational Configuration 1	R/W	26
2FH	IND_TRNSE1_CHN	Individual Transmit E1 Channel Interrupt	R	27
3FH	IND_RECE1_CHN	Individual Receive E1 Channel Interrupt	R	27
4FH	CHIP_ID_NMB	Chip ID Number	R	27
5FH	BUFF_ALLCNT	Buffer All Counters	W	28
8FH	E1_REC_AISTAT	E1 Receivers AIS Status	R	28
9FH	E1_TRNS_AISTAT	E1 Transmitters AIS Status	R	28
AFH	GLOP_CONF	Operational Configuration 3	R/W	29
Transmitter Alarm Status and Configuration Registers (E1 channel #i, i = {0 to 7})				
iEH	TRAMS_CONF	Transmitter Configuration	R/W	31
i1H	TRAN_ALRMIN0	Transmitter Alarm Interrupt 0	R	32
i2H	TRAN_ALRMIN1	Transmitter Alarm Interrupt 1	R	32
i3H	TRAN_ALRM_STAT	Transmitter Alarm Status	R	33
i4H	TRAN_ALRM_INTE0	Transmitter Alarm Interrupt Enable 0	R/W	33
i5H	TRAN_ALRM_INTE1	Transmitter Alarm Interrupt Enable 1	R/W	34
i7-i6H	TRAN_FRMWD_ERC	Transmitter FrameWord Error Counter	R	34
i9-i8H	TRAN_BLCK_ECR	Transmitter CRC-4 Block Errors Counter	R	34
iB-iAH	TRAN_RMT_ERC	Transmitter Remote CRC-4 Block Errors Counter	R	35
iCH	TRAN-RETMBUF	Transmitter Retiming Buffer Pos. & Neg. Slip Counters	R	35
iDH	TRAN_RTMBUF_STAT	Transmitter Retiming Buffer Status	R	36
Receivers Alarm Status and Configuration Registers (E1 channel #i = j - 8, j = {8 to 15})				
jEH	REC_CONF	Receiver Configuration	R/W	37
j1H	REC_ALRMIN0	Receiver Alarm Interrupt 0	R	38
j2H	REC_ALRMIN1	Receiver Alarm Interrupt 1	R	38
j3H	REC_ALRMS	Receiver Alarm Status	R	39
j4H	REC_ALRM_INTEREG0	Receiver Alarm Interrupt Enable Register 0	R/W	39
j5H	REC_ALRM_INTEREG1	Receiver Alarm Interrupt Enable Register 1	R/W	40
j7-j6H	REC_FRMWD_ERC	Receiver FrameWord Error Counter	R	40

Address	Mnemonic	Register Name	Type	Page #
j9-j8H	REC_BLCK_ERC	Receiver CRC-4 Block Error Counter	R	40
jB-jAH	REC_RMT_BLCK_ERC	Receiver Remote CRC-4 Block Error Counter	R	41
jD-jCH	REC-CD_ERC	Receiver Code Errors Counter	R	41

4.1 Global Registers

The registers described in this section are related to global configuration, tests and alarms.

4.1.1 GLOB_CONF0 - Global Operational Configuration 0 (0FH)

Configures high level operational characteristics of the chip.

Bit	Name	Label	Type	Default
Bit <7:6>	CnfBpvIns[1..0]	These bits configure the code errors (Bipolar Violation) inserted in all the E1 HDB3 transmitter outputs (TPOSD and TNEGD, to the LIU) when the BpvInsert is enabled (see register iEH) - (used for testing) 00 - Insert a single code error 01 - Insert one code error per second (used for testing) 10 - Insert one code error per multiframe (used for testing) 11 - Insert one code error per 1000 bits (BER 10-3) (used for testing)	R/W	0

Bit	Name	Label	Type	Default
Bit <5:4>	CnfBpvDet[1..0]	These bits configure the Bipolar Violation Errors Detection in all the E1 HDB3 receivers (on RPOSD and RNEGD inputs, from the LIU). 00 - Disable Bpv Detection 01 - 2 consecutive '1' with the same polarity 10 - BPV do not alternate polarity (recommendation ITU O161) 11 - two consecutive '1' with the same polarity, BPV do not alternate polarity, or four consecutive'0' badly encoded	R/W	11
Bit <3:2>	CnfFeCnt[1..0]	These bits configure the FrameWord (FAS/NFAS) error counters in all the E1 transmitters and receivers. 00 - Disable FrameWord error counter 01 - Count only FAS with single or multiple errors 10 - Count only errored NFAS (bit 2) 11 - Count both errored FAS *and* NFAS	R/W	0
Bit <1:0>	CnfFaOp[1..0]	These bits configure the Frame Acquisition Algorithm in all transmitters and receivers. The robust acquisition modes are only relevant if CRC-4 multiframing is disabled (see registers iEH and jEH). CRC-4 Multiframing selected always uses normal acquisition modes. 00 - Normal Acquisition: During acquisition, check three consecutive frames with two correct FAS and one correct NFAS. De-synchronization caused by three consecutive incorrect FAS. 01 - Normal Acquisition/de-synchronization using both FAS/NFAS: During acquisition, check three consecutive frames with two correct FAS and one correct NFAS. De-synchronization caused by three consecutive incorrect FAS or by three consecutive bit 2 of NFAS, not 1. 10 - Robust Acquisition: During acquisition, check five consecutive frames with three correct FAS and two correct NFAS. De-synchronization caused by four consecutive incorrect FAS. 11 - Robust Acquisition/de-synchronization using both FAS/NFAS: During acquisition, check five consecutive frames with three correct NFAS. De-synchronization caused by four consecutive incorrect FAS or by four consecutive incorrect NFAS.	R/W	0

4.1.2 GLOB_CONF1- Global Operational Configuration 1 (1FH)

Bit	Name	Label	Type	Default
Bit 7	AlmUpdDsbl	This bit enables/disables updates to status registers. 0 - Enable status updates when alarm interrupt is active 1 - Disable status updates when alarm interrupt is active	R/W	0
Bit 6	MastIntEn	Enables/disables the chip interrupt pin. 0 - Disable 1 - Enable	R/W	0
Bit <5:4>	Unused			
Bit 3	TestTBR	Test Bit: **has to be set to 0** 0 - Normal operation 1 - Test Only - non-working mode	R/W	0

Bit	Name	Label	Type	Default
Bit 2	AutotestCnfg	This bit configures the generation of the test pattern sequence as framed or unframed (both test pattern sequences are described in 0.151) 0 - Unframed (PBRS2E15-1 sequence). 1 - CRC-4 framed sequence. The PRBS2E15-1 sequence is transmitted in time slot 1 to 31 (and stopped during timeslot 0.)	R/W	1
Bit 1	ADPLLTest	This bit **should always be set to 0** during normal operation. It allows faster testing of the eight digital PLLs during simulation. 0 - Normal operation 1 - Very fast tracking PLLs	R/W	0
Bit 0	CntrTest	This bit **should always be set to 0** during normal operation. It allows faster testing of the overflow interrupt functionality during simulation. 0 - Normal operation 1 - set overflow count: error counter 4; retiming slip counters: 2	R/W	0

These next two registers (2FH and 3FH) indicate which channel (receiver or transmitter) has caused an interrupt.

For example, when a channel incurs a receive LOS alarm event, if the interrupt is enabled, the LosInt bit in the interrupt register will be set and causing the device interrupt pin to become active. The microcontroller would then read the Receive E1 Channel interrupt register 3FH to determine the channel in alarm. Next the Channel Interrupt Registers Receive j1H would be read to identify the alarm. Finally, the status register j3H is read to determine the current alarm state. This last read would also clear the corresponding interrupt register.

4.1.3 IND_XMTE1_CHN - Individual Transmit E1 Channel Interrupt (2FH)

Bit	Name	Label	Type	Default
Bit <7:0>	XmtChannel XMTINT <7:0>	This register indicates which E1 channel transmitter has caused an interrupt.	RO	0

4.1.4 IND_RCVE1_CHN - Individual Receive E1 Channel Interrupt (3FH)

Bit	Name	Label	Type	Default
Bit <7:0>	RcvChannel RCVINT <7:0>	This register indicates which E1 channel receiver has caused an interrupt.	RO	0

4.1.5 CHIP_ID_NMB - Chip ID Number (4FH)

This register can only be read. It is used to identify the version of the chip.

Bit	Name	Label	Type	Default
Bit <7:0>	ChipID [7:0]	This field contains the chip identification value	RO	01H

4.1.6 BUFF_ALLCNT - Buffer All Counters (5FH)

A write to this location causes all of the counters of the same type to be loaded into buffers and then cleared. This operation assumes that those counters can be monitored in the same second. The contents of an individual counter buffer can then be read at the addresses specified for the counters in this document. Counters can be individually buffered by writing to the specified MSByt of the counter of interest.

Bit	Name	Label	Type	Default
Bit <7:2>	Unused			
Bit <1:0>	BfrAllCntrs[1:0]	A write to these bits selects the counters to be loaded at the same time. 00 - all CRC-4 Block Error counters both transmit and receive (16 x 10-bit counters) plus all Positive and Negative Frame Slip Counters (transmit side: 16 x 4-bit counters) 01 - all REBE Counters both transmit and receive (16x 10-bit counters) plus all Retiming FIFO Status Bits (transmit side: 8 x 6-bits, 8 registers iDH) 10 - all FrameWord Error Counters both receive and transmit (16 x 13-bit counters) 11 - all Code Errors counters (receive side) (8 x 16-bit counters)	WO	0

4.1.7 E1_RCV_AISTAT - E1 Receivers AIS Status (8FH)

This register indicates the status of internal chip logic for AIS generation processes in each of the eight E1 receivers.

Bit	Name	Label	Type	Default
Bit <7:0>	GenRcvAISCh<7:0>	Present status of E1 receiver #n (n= <7..0>) AIS generator. 0 - No AIS 1 - AIS	RO	0

4.1.8 EI_XMT_AISTAT - E1 Transmitters AIS Status (9FH)

This register indicates the status of internal chip logic for AIS generation processes in each of the eight E1 transmitters.

Bit	Name	Label	Type	Default
Bit <7:0>	GenXmtAISCh<7:0>	Present status of E1 transmitter #n (n=<7..0>) AIS generator. 0 - No AIS 1 - AIS	RO	0

4.1.9 GLOB_CONF - Global Operational Configuration 3 (AFH)

Bit	Name	Label	Type	Default
Bit 7	CnfTxClkIn	Clock Edges specification at the data interfaces: This bit Configures the phase relation between clock and data at the transmitter inputs (DTCx and DTDx input pins). 0 - DTDx input data is sampled in the chip by the falling edge of DTCx clock. 1 - DTDx input data is sampled in the chip by the rising edge of DTCx clock.	R/W	0
Bit 6	CnfTxClkOut	This bit configures the phase relation between clock and data at the transmitters outputs (TCLKx and TPOSDx/TNEGDx output pins). 0 - TPOSDx/TNEGDx output data are sampled by the rising edge of TCLKx clock. 1- TPOSDx/TNEGDx output data are sampled by the falling edge of TCLKx clock.	R/W	0
Bit 5	CnfRxClkIn	This bit configures the phase relation between clock and data at the receivers inputs (RCLKx and RPOSDx/RNEGDx input pins). 0 - RPOSDx/RNEGDx input data are sampled in the chip by the rising edge of RCLKx clock. 1 - RPOSDx/RNEGDx input data is sampled in the chip by the falling edge of RCLKx clock.	R/W	0
Bit 4	CnfRxClkOut	This bit configures the phase relation between clock and data at the receivers outputs (MTCx and MTDx output pins). 0 - MTDx output data are sampled by the falling edge of MTCx clock. 1- MTDx output data are sampled by the rising edge of MTCx clock.	R/W	0
Bit <3:0>	DjtAisSetWinNum[3:0]	Consecutive windows for setting AIS in the transmitters (dejitter mode): These bits are only relevant in dejitter mode (Transmitter) and are common for the eight transmitters when hardware AIS is enabled (see register iEH). Number of consecutive 200 ms windows that must detect dejitter ADPLL unlocked and dejitter FIFO crash to insert AIS and switch to the blue clock on the transmitter output. (Detection time = DjtAisSetWinNum *200 ms.) (Note: DjtAisSetWineNum = 0 => immediate insertion of AIS after detection of dejitter FIFO crash alarm)	R/W	0

4.2 Transmit Side Registers

The registers described in this section are related to the E1 transmitters alarm status and configuration.

There are eight E1 transmitters in the chip, and 14 registers per E1 transmitter. The 4 MSB bits of the register addresses indicate the E1 channel number (from 0 to 7). The eight transmitters are each capable of generating 12 alarm types. Any one of these alarms (if enabled) can cause the device interrupt pin to become active.

Each E1 transmitter alarm has three registers associated with it:

- Interrupt source: This register set will identify the alarm(s) that triggered the interrupt.
- Alarm status: This register contains the current status of the alarm. When this register is read, the corresponding interrupt will be cleared.
- Interrupt Enable: This register contains the interrupt enable for all alarms.

Status alarms will generate an interrupt when the alarm changes from inactive to active *or* active to inactive. The event and overflow alarms generate an interrupt when detected.

Updating the status register is controlled by the AlmUp-dateDsbl configuration bit in global register 0FH. When low, status register are updated once every frame, regardless of the interrupt state. When high, status alarm memory updates will be disabled. When accessing status alarm memory, the microprocessor should SET AlmUpdateDsbl so that the microprocessor will have uncontested access to this memory.

4.2.1 XMT_CONF - Transmitter Configuration (iEH)

(i = [0 to 7] and corresponds to the eight different E1 channel numbers)

This register configures a particular E1 channel transmitter's parameters.

Bit	Name	Label	Type	Default
Bit 7	CenterRetFifo	A transition from 0 to 1 in this bit sets the two frame-wide retiming elastic store to its center point (only relevant in retiming mode).	W	0
Bit 6	XmtDjtAisEn	Enable/disable hardware AIS generation on the transmit data and clock outputs (to the LIU) via software (only relevant in dejitter mode). This bit should be set to 0 before changing the mode from dejitter. 0 - Disable AIS generation because of unlocked PLL 1 - Enable AIS generation because of unlocked PLL	R/W	0
Bit 5	InsBpv	Inserts a code error (Bipolar Violation) in the transmitter HDB3 output (TPOSD and TNEGD, to the LIU). See CnfBpvIns[1..0] configuration bits in global register 0FH for the error repetition. 0 - Normal operation 1 - Insert Bpv errors (see register 0FH)	R/W	0
Bit 4	XmtAisFrc	Forces AIS generation on the transmit data and clock outputs (to the LIU). 0 - Disable 1 - Enable	R/W	0

Bit	Name	Label	Type	Default
Bit 3	XmtCrc-4En	Enable/disable G704 CRC-4 monitoring and multiframing in the E1 transmitter (on DTD data input). 0 - Disable. In this case, the E1 transmitter checks the errors in the E1 frameword (every two frames) and counts them in the XmtErrCnt errors counter. No CRC multiframing 1 - Enable. The chip performs a CRC-4 check on the incoming E1. The blocks in error is counted in the XmtErrCnt errors counter	R/W	0
Bit <2:1>	OpCnf <1..0>	Each E1 Transmitter can be configured for the following operational modes. 00 - Passed through mode: no dejitter, no retiming in the transmitter 01 - Dejitter mode 10 - Retiming mode: normal configuration (operates on an E1 framed signal) 11 - Retiming mode: test configuration (operates on a 2.048 Mbit/s un-framed signal; in this mode the CRC-4, REBE and remote alarm monitoring functions are irrelevant since the incoming data is supposed to be un-framed.) (Note: When not in dejitter mode, the High Speed ADPLL reference Clock is shut down in the transmitter to save power consumption.)	R/W	01
Bit 0	XmtLnCodeSel	Line Interface coding (on TPOSD/TNEGD transmit data). 0 - HDB3 1 - NRZ	R/W	0

4.2.2 XMT_ALRM_INTO - Transmitter Alarm Interrupt 0 (i1H)

(i = [0 to 7] and corresponds to the E1 channel number)

This register identifies the interrupt source for a particular E1 Channel Transmitter. Each of these bits can cause the chip interrupt pin to become active if enabled via the bits in the Transmit Interrupt Enable Register 0 (i4H).

Bit	Name	Label	Type	Default
Bit <7:5>	Unused			
Bit 4	XmtRmtAlm	This bit is set when there is a change in the XmtRmtAlmSt bit (i3H). It is cleared when status register (i3H) is read.	RO	0
Bit 3	XmtLomf	This bit is set when there is a change in the XmtLomfSt bit (i3H). It is cleared when status register (i3H) is read.	RO	0
Bit 2	XmtOof	This bit is set when there is a change in the XmtOofSt bit (i3H). It is cleared when status register (i3H) is read.	RO	0
Bit 1	XmtAisDet	This bit is set when there is a change in the XmtAisDetSt bit (i3H). It is cleared when status register (i3H) is read.	RO	0
Bit 0	Unused			

4.2.3 XMT_ALRM_INT1 - Transmitter Alarm Interrupt 1(i2H)

(i = [0 to 7] and corresponds to the E1 channel number)

This register identifies the interrupt source for a particular E1 Channel Transmitter. Each of these bits can cause the chip interrupt pin to become active if enabled via the bits in the Transmit Interrupt Enable Register 1 (i5H).

Bit	Name	Label	Type	Default
Bit 7	XmtPosSlip	Indicates that a positive frame slip has occurred in the retiming elastic buffer. It is cleared when this register is read.	RO	0
Bit 6	XmtNegSlip	Indicates that a negative frame slip has occurred in the retiming elastic buffer. It is cleared when this register is read.	RO	0
Bit 5	XmtFifofAlm	Indicates that the transmit FIFO has overflowed (depending on the OpCnf bits setting, this can be either the dejitter FIFO, or the retiming elastic buffer). It is cleared when register is read.	RO	0
Bit 4	XmtRetNegOvrFlw	This bit is set when the RetNegCnt[] retiming positive slip counter rollover occurs. It is cleared when this register is read.	RO	0
Bit 3	XmtRetPosOvrFlw	This bit is set when the RetPosCnt[] retiming positive slip counter rollover occurs. It is cleared when this register is read.	RO	0
Bit 2	XmtRbeOvrFlw	This bit is set when the RbeCnt[] Remote Block error counter rollover occurs. It is cleared when this register is read.	RO	0
Bit 1	XmtCrc4ErrOvrFlw	This bit is set when the Crc4ErrCnt[] error counter rollover occurs. It is cleared when this register is read.	RO	0
Bit 0	XmtFasErrOvrFlw	This bit is set when the FasErrCnt[] Frame Alignment Signal error counter rollover occurs. It is cleared when this register is read.	RO	0

4.2.4 XMT_ALM_STAT - Transmitter Alarm Status (i3H)

(i = [0 to 7] and corresponds to the E1 channel number)

This register gives the present status of each alarm source for a particular E1 channel transmitter.

These registers are associated with the interrupt source registers. Status the interrupt source bits have an associated status bit. Generally, when an interrupt is being acknowledged, the status bit will be checked to see the present status of the interrupt-generating source. Overflow event interrupt sources do not have status bits.

Bit	Name	Label	Type	Default
Bit <7:5>	Unused			
Bit 4	XmtRmAlmSt	Present status of Remote Alarm detect on DTDx input data. 0 - No Remote Alarm 1 - Remote Alarm	RO	0
Bit 3	XmtLomfSt	Present status of Out Of E1 CRC-4 MultiFrame detect on DTDx input data. 0 - No LOMF 1 - LOMF	RO	0
Bit 2	XmtOofSt	Present status of Out Of E1 Frame detect on DTDx input data. 0 - No OOF 1 - OOF	RO	0
Bit 1	XmtAisDetSt	Present status of AIS defect detect on DTDx input data. 0 - No AIS defect 1 - AIS defect detected	RO	0
Bit 0	Unused			

4.2.5 XMT_ALM_INTE0 - Transmitter Alarm Interrupt Enable 0 (i4H)

(i = [0 to 7] and corresponds to the E1 channel number)

This register can be used to enable an interrupt source for a particular E1 channel interrupt source. The reset default is disabled (‘0’). All of the interrupt registers in the above section are capable of activating the chip interrupt pin if their corresponding interrupt enable bits are set to 1.

Bit	Name	Label	Type	Default
Bit 7:5	Unused			
Bit 4	XmtRmtAlmIntEn		R/W	0
Bit 3	XmtLomfIntEn		R/W	0
Bit 2	XmtOofIntEn		R/W	0
Bit 1	XmtAisDetIntEn		R/W	0
Bit 0	Unused			

4.2.6 XMT_ALM_INTE1 - Transmitter Alarm Interrupt Enable 1 (i5H)

(i = [0 to 7] and corresponds to the E1 channel number)

This register can be used to enable an interrupt source for a particular E1 channel interrupt source. The reset default is disabled (‘0’). All of the interrupt registers in the above section are capable of activating the chip interrupt pin if their corresponding interrupt enable bits are set to 1.

Bit	Name	Label	Type	Default
Bit 7	XmtPosSlipEn		R/W	0
Bit 6	XmtNegSlipEn		R/W	0
Bit 5	XmtFifofAlmIntEn		R/W	0
Bit 4	XmtRetNOvrFlwEn		R/W	0
Bit 3	XmtRetPOvrFlwEn		R/W	0
Bit 2	XmtRbeOvrFlwEn		R/W	0
Bit 1	XmtCrcErrOvrFlwEn		R/W	0
Bit 0	XmtFasErrOvrFlwEn		R/W	0

4.2.7 XMT_FRMWD_ERC - Transmitter FrameWord Error Counter (i7- i6H)

(i = [0 to 7] and corresponds to the E1 channel number)

(i7H = bits <15:8>, i6H = bits <7:0>

This counter increments each time an errored E1 frameword (FAS and/or NFAS: see global configuration register 0FH: bits CnfFeCnt[1..0]) is detected. A write to the MSByte of the counter (register i7H) causes the entire counter to be buffered and then cleared. The contents of the buffer can then be read.

Bit	Name	Label	Type	Default
Bit <15:13>	Unused			
Bit <12:0>	XmtFasErrCnt[12:0]		RO	00H

4.2.8 XMT_BLCK_ERC - Transmitter CRC-4 Block Errors Counter (i9H - i8H)

(i = [0 to 7] and corresponds to the E1 channel number)

(i9H = bits<15:8>, i6H = bits<7:0>

This counter increments each time a CRC-4 Block error is detected. A write to the MSByte of the counter (register i9H) causes the entire counter to be buffered and then cleared. The contents of the buffer can then be read.

Bit	Name	Label	Type	Default
Bit <15:10>	Unused			
Bit <9:0>	XmtCrc4ErrCnt[9:0]		RO	00H

4.2.9 XMT_RMT_ERC - Transmitter Remote CRC-4 Block Errors Counter (iB - iAH)

(i = [0 to 7] and corresponds to the E1 channel number)

(iBH = bits<15:8>, iAH = bits<7:0>)

This counter increments each time a Remote CRC-4 Block error is detected. A write to the MSByte of the counter (register iBH) causes the entire counter to be buffered and then cleared. The contents of the buffer can then be read.

Bit	Name	Label	Type	Default
Bit < 15:10>	Unused			
Bit <9:0>	XmtRbeCnt[9:0]		RO	0

4.2.10 XMT_RETMBUF - Transmitter Retiming Buffer Positive & Negative Slip Counters (iCH)

(i = [0 to 7] and corresponds to the E1 channel number)

A write to the register (register iC) causes both counters to be buffered and then cleared. The contents of the buffer can then be read.

Bit	Name	Label	Type	Default
Bit <7:4>	RetNegCnt[3:0]	The RetNegCnt[3..0] counter (4 MSB bits of register iCH) counter increments each time a negative slip is detected in the retiming elastic buffer (one complete frame is lost).	RO	0
Bit <3:0>	RetPosCnt[3:0]	The RetPosCnt[3..0] counter (4 LSB bits of register iCH) increments each time a positive slip is detected in the retiming elastic buffer (one complete frame is repeated).	RO	0

4.2.11 XMT_RTMBUF_STAT - Transmitter Retiming Buffer Status (iDH)

(i = [0 to 7] and corresponds to the E1 channel number)

A write to the register (register iDH) causes the Retiming elastic store status bits to be buffered. The contents of the buffer can then be read.

Bit	Name	Label	Type	Default
Bit <7:6>	Unused			
Bit <5:0>	RetFifoStatus<5:0>	The RetFifoStatus[5..0] bits make an indication of the content of the Retiming 2 frame-wide elastic store. This value, coded on 6 bits, corresponds to the difference between the read and the write pointer of the FIFO and may be used for wander monitoring and delay calculation.	RO	<0, 1, 0, 1, 0, 0>

If WritePointerValue < ReadPointerValue then

$$RetFifoStatus[5..0] = 64 + WritePointerValue - ReadPointerValue$$

else

$$RetFifoStatus[5..0] = WritePointerValue - ReadPointerValue$$

4.3 Receive Side Registers

The registers described in this section are related to the E1 receivers alarm status and configuration.

There are eight E1 receivers in the chip, and 14 registers per E1 receiver. The 4 MSB bits of the register addresses indicate the E1 channel number (4 MSB bits [from 8 to 15] minus 8 correspond to the E1 channel number: from 0 to 7)

The eight receivers are each capable of generating nine alarm types. Any one of these alarms (if enabled) can cause the device interrupt pin to become active.

Each E1 receiver alarm has three registers associated with it:

- Interrupt source: This register set will identify the alarm(s) that triggered the interrupt
- Alarm status: This register contains the current status of the alarms. When this register is read, the corresponding interrupts will be cleared

- Interrupt Enable: This register contains the interrupt enables for all alarms

Status alarms will generate an interrupt both when the alarm changes from inactive to active *or* active to inactive. The overflow alarms generate an interrupt when detected.

Updating the status register is controlled with the AlmUpdsbl bit in global register 0FH. When low, the status registers are updated once every frame, regardless of the interrupt state. When high, status alarm memory updates will be disabled. When accessing status alarm memory, the microprocessor should SET AlmUpdateDsbl so that the microprocessor will have uncontested access to this memory.

4.3.1 RCV_CONF- Receiver Configuration (jEH)

(j =[8 to F] and corresponds to the eight different E1 channel numbers)

This register configures a particular E1 channel receiver parameters.

Bit	Name	Label	Type	Default
Bit 7	Unused			
Bit 6	AutoTestEn	Enable/disable test pattern generator (the contents of the sequence is configured in global register 1FH). 0 - Normal mode (disable autotest) 1 - Enable autotest	R/W	0
Bit 5	RcvBclkEn	Enable/disable hardware switches to blue clock during Loss Of Signal condition. 0 - Disable hardware clock switch because of LOS 1 - Enable hardware clock switch because of LOS	R/W	0
Bit 4	RcvCrc-4En	Enable/disable CRC-4 monitoring and multiframing in the E1 receiver (on RPOSD/RNEGD data input from the LIU). 0 - Disable. In this case, the receiver checks the errors in the receive E1 frameword (every two frames) and counts them in the RxErrCnt error counter. CRC multiframing is also disabled 1 - Enable. The chip performs a CRC-4 check on the incoming E1. The blocks in error are counted in the RxErrCnt errors counter. CRC multiframing is also enabled.	R/W	0
Bit 3	RcvLosFlt	Configure LOS alarm filtering (on RLOS input signal). 0 - No filtering 1 - LOS filtering. The LOS condition must be maintained for 128 clock cycles	R/W	0
Bit 2	RcvAisFrc	Force AIS generation from the receive data and clock inputs (from the LIU) to the receiver output (to the multiplexer) via software. 0 - Disable 1 - Enable	R/W	0
Bit 1	RcvAisEn	Enable/disable hardware AIS generation from the receive data and clock inputs (from the LIU) to the receiver output (to the PDH/SDH multiplexer). 0 - Disable AIS generation because of LOS 1 - Enable AIS generation because of LOS	R/W	0
Bit 0	RcvLnCodeSel	Line interface coding (on RPOSD/RNEGD receive data) 0 - HDB3 1 - NRZ	R/W	0

4.3.2 RCV_ALRM_INT0 - Receiver Alarm Interrupt 0 (j1H)

(j =[8 to F] and corresponds to the E1 channel number)

This register identifies the interrupt source for a particular E1 channel receiver. Each of these bits can cause the chip interrupt pin to become active if enabled via the bits in the Receive Interrupt Enable Register j4H.

Bit	Name	Label	Type	Default
Bit <7:5>	Unused			
Bit 4	RcvRmtAlm	This bit is set when there is a change in the RcvRmAlmSt Receive Remote Alarm bit (j3H). It is cleared when status register (j3H) is read.	RO	0
Bit 3	RcvLomf	This bit is set when there is a change in the RcvLomfSt bit (j3H). It is cleared when status register (j3H) is read.	RO	0
Bit 2	RcvOof	This bit is set when there is a change in the RcvOofSt bit (j3H). It is cleared when status register (j3H) is read.	RO	0
Bit 1	RcvAisDet	This bit is set when there is a change in the RcvAisDetSt bit (j3H). It is cleared when status register (j3H) is read.	RO	0
Bit 0	Los	This bit is set when there is a change in the LosSt bit (j3H). It is cleared when status register (i3H) is read.	RO	0

4.3.3 RCV_ALRM_INT1 - Receiver Alarm Interrupt 1 (j2H)

(j =[8 to F] and corresponds to the E1 channel number)

This register identifies the interrupt source for a particular E1 channel receiver. Each of these bits can cause the chip interrupt pin to become active if enabled via the bits in the Receive Interrupt Enable Register j5H.

Bit	Name	Label	Type	Default
Bit <7:4>	Unused			
Bit 3	BpvOvrFlw	This bit is set when the BpvCnt[] Code error counter rollover occurs. It is cleared when this register is read.	RO	0
Bit 2	RcvRbeOvrFlw	This bit is set when the RbeCnt[] Remote Block error counter rollover occurs. It is cleared when this register is read.	RO	0
Bit 1	RcvCrc4ErrOvrFlw	This bit is set when the RcvCrc4ErrCnt[] Receive CRC-4 block error counter rollover occurs. It is cleared when this register is read.	RO	0
Bit 0	RcvFasErrOvrFlw	This bit is set when the RcvFasErrCnt[] Receive Frame Alignment Signal error counter rollover occurs. It is cleared when this register is read.	RO	0

4.3.4 REC_ALRMS - Receiver Alarm Status (j3H)

(j =[8 to F] and corresponds to the E1 channel number)

This register gives the present status of each alarm source for a particular E1 channel receiver.

These registers are associated with the interrupt source registers. Status interrupt source bits have an associated status bit. Generally, when an interrupt is being acknowledged, the status bit will be checked to see the present status of the interrupt-generating source. Overflow interrupt sources do not have status bits associated with them since the counter value fulfills this purpose.

Bit	Name	Label	Type	Default
Bit <7:5>	Unused			
Bit 4	RcvRmtAlmSt	Present status of Receive Remote Alarm detect. 0 - No Remote Alarm 1 - Remote Alarm	RO	0
Bit 3	RcvLomfSt	Present status of Out Of E1 CRC-4 MultiFrame detect. 0 - No LOMF 1 - LOMF	RO	0
Bit 2	RcvOofSt	Present status of Out Of E1 Frame detect. 0 - No OOF 1 - OOF	RO	0
Bit 1	RcvAisDetSt	Present status of AIS defect detect on the incoming E1 data (ITU G.775). 0 - No AIS 1 - AIS defect detected	RO	0
Bit 0	LosSt	Present status of Loss of Signal detect. 0 - No LOS 1 - LOS	RO	0

4.3.5 RCE_ALM_INTE0 - Receiver Alarm Interrupt Enable Register 0 (j4H)

(j =[8 to F] and corresponds to the E1 channel number)

This register can be used to enable an interrupt source for a particular E1 channel. The reset default is not enabled (‘0’). All of the interrupt registers in the above section are capable of activating the chip interrupt pin if their corresponding interrupt enable bits are set to 1.

Bit	Name	Label	Type	Default
Bit <7:5>	Unused			
Bit 4	RcvRmtAlmEn		R/W	0
Bit 3	RcvLomfIntEn		R/W	0
Bit 2	RcvOofIntEn		R/W	0
Bit 1	RcvAisDetIntEn		R/W	0
Bit 0	LosIntEn		R/W	0

4.3.6 RCV_ALM_INTE1 - Receiver Alarm Interrupt Enable Register 1 (j5H)

(j =[8 to F] and corresponds to the E1 channel number)

This register can be used to enable an interrupt source for a particular E1 channel. The reset default is disabled (‘0’). All of the interrupt registers in the above section are capable of activating the chip interrupt pin if their corresponding interrupt enable bits are set to 1.

Bit	Name	Label	Type	Default
Bit <7:4>	Unused			
Bit 3	BpvOvrFlwIntEn		R/W	0
Bit 2	RcvRbeOvrFlwEn		R/W	0
Bit 1	RcvCrcOvrFlwIntEn		R/W	0
Bit 0	RcvFasErrOvrFlwEn		R/W	0

4.3.7 RCV_FRMWD_ERC - Receiver FrameWord Error Counter (j7 - j6H)

(j =[8 to F] and corresponds to the E1 channel number)

(j7H = bits <15:8>, j6H = bits <7:0>)

This counter increments each time an errored E1 frameword (FAS and/or NFAS: see global configuration register 0FH: bits CnfFeCnt[1..0]) is detected. A write to the MSByte of the counter (Register j7H) causes the entire counter to be buffered and then cleared. The contents of the buffer can then be read.

Bit	Name	Label	Type	Default
Bit <15:13>	Unused			
Bit <12:0>	RcvFasErrCnt[12:0]		RO	0

4.3.8 RCV_BLCK_ERC - Receiver CRC-4 Block Error Counter (j9 - j8H)

(j =[8 to F] and corresponds to the E1 channel number)

(j9H = bits<15:8>, j8H = bits <7:0>

This counter increments each time either a CRC Block error event is selected. A write to the MSByte of the counter (Register j9H) causes the entire counter to be buffered and then cleared. The contents of the buffer can then be read.

Bit	Name	Label	Type	Default
Bit <15:10>	Unused			
Bit <9:0>	RcvCrc4ErrCnt[9:0]		RO	0

4.3.9 RCV_RMT_BLCK_ERC - Receiver Remote CRC-4 Block Error Counter (jB - jAH)

(j =[8 to F] and corresponds to the E1 channel number)

(jBH = bits<15:8>, jAH = bits<7:0>)

This counter increments each time a remote CRC-4 block error is detected. A write to the MSByte of the counter (Register jBH) causes the entire counter to be buffered and then cleared. The contents of the buffer can then be read.

Bit	Name	Label	Type	Default
Bit <15:10>	Unused			
Bit <9:0>	RcvRbeCnt[9:0]		RO	0

4.3.10 RCV_CD_ERC - Receiver Code Errors Counter (jDH)

(j =[8 to F] and corresponds to the E1 channel number)

(jDH = bits <15:8>, jCH = bits<7:0>)

This counter increments each time a code error (Bipolar Violation) is detected, according to cnfBpvDet[1,0] configuration bits in global register 0FH. A write to the MSByte of the counter (register jDH) causes the entire counter to be buffered and then cleared. The contents of the buffer can then be read.

Bit	Name	Label	Type	Default
Bit <15:0>	BpvCnt[15:0]		RO	0

5.0 Test Specifications

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	VDD		3.6	V
DC Voltage on any pin[1]	VIN	-1.0	5.5	V
Ambient operating temperature	TOP	-40	+85	C
Storage temperature range	TST	-65	+150	C
1. Minimum voltage is -0.6V dc which may undershoot to -1.0 V for pulses of less than 20 ns				
Caution: Exceeding these values may cause permanent damage. ***Caution:*** Functional operation under these conditions is not implied ***Caution:*** Exposure to maximum rating conditions for extended periods may affect device reliability				

Table 5. Operating Conditions

Parameter	Symbol	Min	Typ[1]	Max	Unit
Recommended Operating Temperature	TOP	-40	-	+85	C
Supply Voltage - I/O Ring and Core	VDDr	3.0	3.3	3.6	V
Supply Current [3] (8 channels in jitter attenuation mode)	IDDrja	-	65	-	mA
Supply Current - Core [3] (8 channels in retiming mode)	IDDrret	-	15	-	mA
1. Typical values are at 25C and nominal voltage and are provided for design aid only; not guaranteed nor subject to production testing 2. Voltages with respect to ground unless otherwise specified 3. Core +I/O (outputs loaded with 30pF).					

Table 6. 5 V Tolerant Digital I/O Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Input Low Voltage	VIL			0.5	V	
Input High Voltage	VIH	2.0	5.0	5.5	V	
Switching Threshold	VT		1.4		V	VDD=3.3V, 25C
Input Leakage High	IIH			5	uA	VIN=VDD=3.6V
Output Low Voltage	VOL			0.4	V	VDD=3.0V
Output High Voltage	VOH	VDD-0.6V			V	
Output Leakage (no pull up)	IOZ	-10		10	uA	Vin=VDD or VSS, VDD= 3.6V, No pull up
1. All values applicable over recommended Voltage and Temperature operating range unless otherwise noted						

Figure 6. E1 outputs, transmitted to the LIUs, Timing

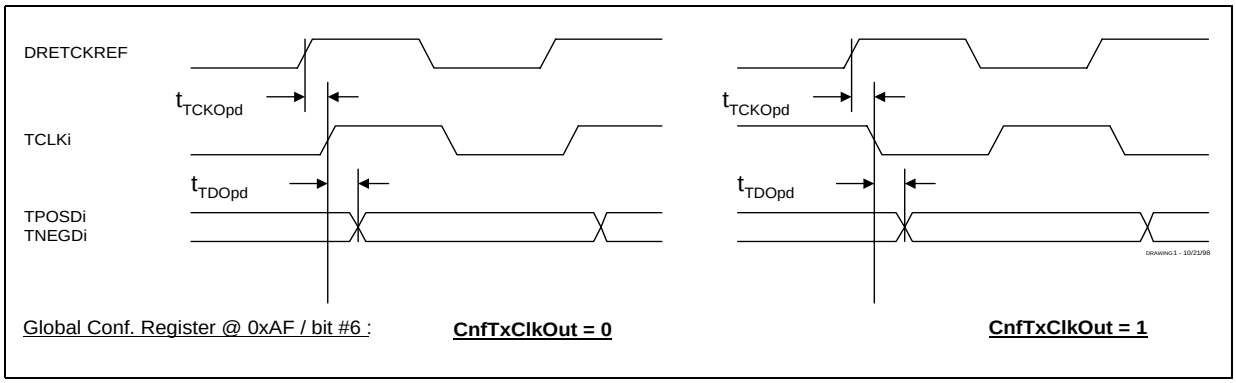


Table 7. E1 outputs, transmitted to the LIUs, Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
DRETCKREF rising edge to TCLKi rising/falling edge	t_{TCKOpd}[2]	3		11	ns
TCLKi rising/falling edge to TPOSDi and TNEGDi[1]	t_{TDOpd}[2]	1		8	ns

1. i = [0 to 7] and corresponds to the eight different E1 channel numbers
2. Considering outputs with a 25pF load

Figure 7. E1 inputs, received from the LIUs, Timing

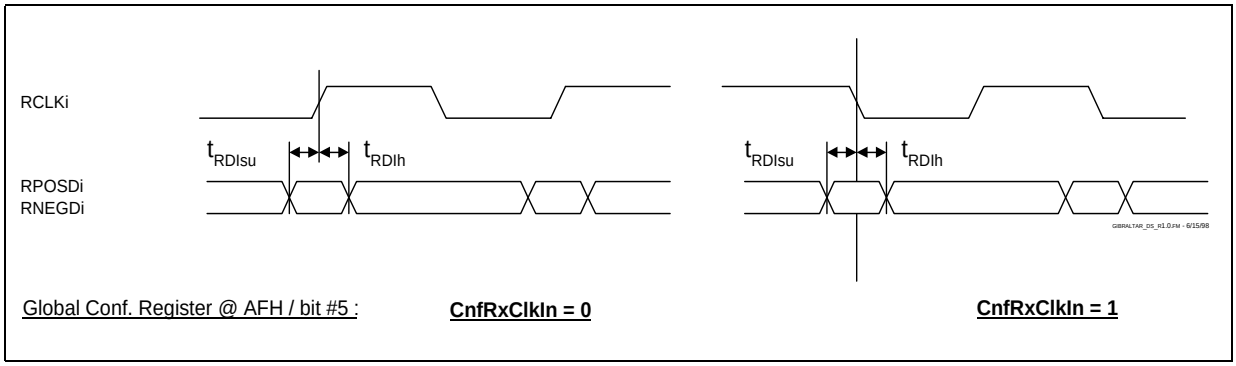


Table 8. E1 inputs, received from the LIUs,Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
RPOSDi and RNEGDi setup time to RCLKi rising/falling edge	t_{RDIsu}	1			ns
RPOSDi and RNEGDi hold time from RCLKi rising/falling edge	t_{RDIh}	4			ns

1. i = [0 to 7] and corresponds to the eight different E1 channel numbers

Figure 8. E1 inputs, received from the demultiplexer, Timing

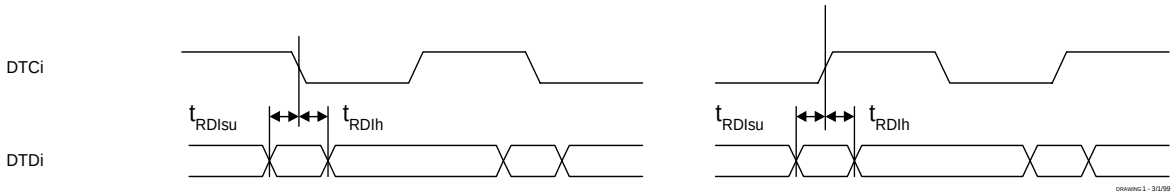


Table 9. E1 inputs, received from the demultiplexer, Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
DTDi setup time to DTCi falling/rising edge	t_{RDIsu}	1			ns
DTDi hold time from DTCi falling/rising edge	t_{RDIh}	3			ns

1. i = [0 to 7] and corresponds to the eight different E1 channel numbers
2. Considering outputs with a 25pF load

Figure 9. E1 outputs, transmitted to the multiplexer, Timing

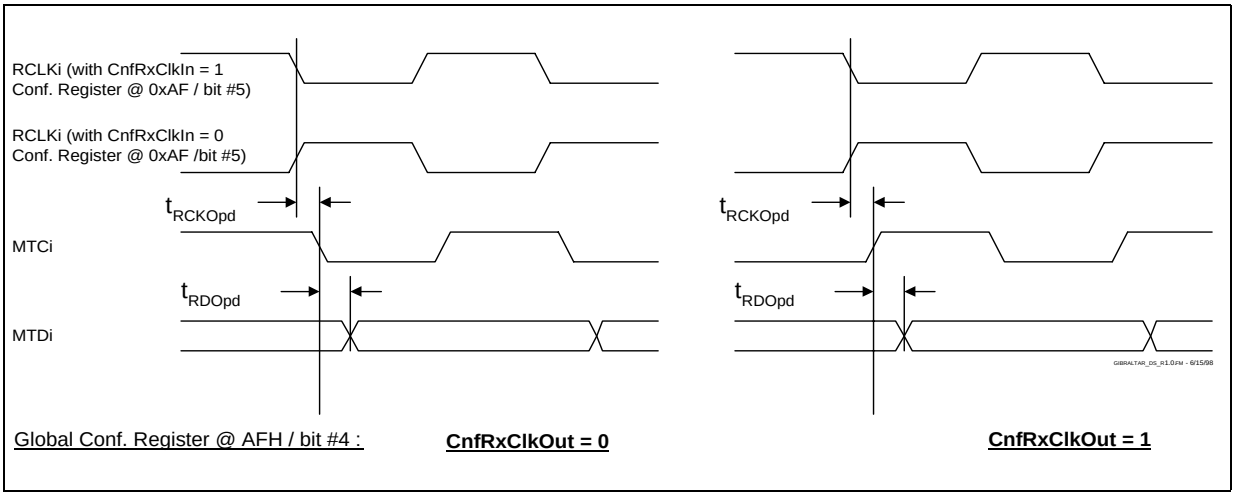


Table 10. E1 outputs, transmitted to the multiplexer, Timing

Parameter	Symbol	Min	Typ	Max	Unit
RCLKi rising/falling edge to MTCi rising/falling edge	t_{RCKOpd}	3		12	ns
MTCi falling/rising edge to MTDi	t_{RDOpd}	1		7	ns

1. i = [0 to 7] and corresponds to the eight different E1 channel numbers
2. Considering outputs with a 25pF load

Figure 10. Microprocessor Read Timing

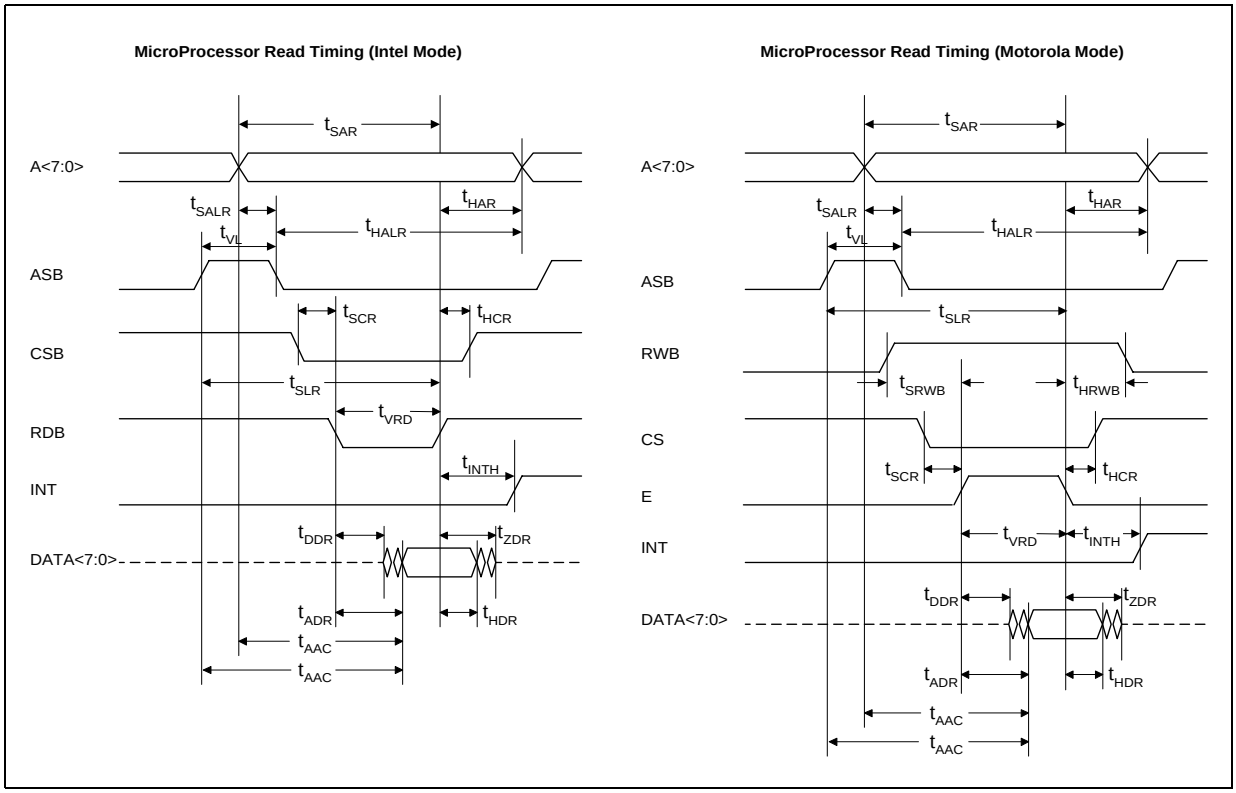


Table 11. Microprocessor Data Read Timing Parameters (considering outputs with a 50pF load)

Parameter	Symbol	Min	Typ	Max	Unit
A<7:0> setup time to read cycle end	t_{SAR}	5			ns
A<7:0> hold time from inactive read	t_{HAR} [1]	1			ns
A<7:0> setup time to latch	t_{SALR} [2]	4			ns
A<7:0> hold time from latch	t_{HALR} [2]	2			ns
Valid latch pulse width	t_{VL} [2]	5			ns
AS rising edge to read cycle end setup	t_{SLR} [2]	6			ns
RWB setup to active read	t_{SRWB}	1			ns
RWB hold from inactive read	t_{HRWB}	1			ns
CSB setup to active read	t_{SCR}	1			ns
CSB hold from inactive read	t_{HCR}	1			ns
DATA<7:0> access time from valid address (or ASB whichever comes last for muxed AD bus)	t_{AAC}			20	ns
DATA<7:0> bus driven from active read	t_{DDR}	5			ns

1. For non-multiplexed Address and Data bus (ASB tied high)
2. For multiplexed Address and Data bus (ASB used as address latch enable)
3. T is the minimum cycle time of either DTCi, either, DRETCKREF, or MTCi (typically 488 ns for E1)

Table 11. Microprocessor Data Read Timing Parameters (considering outputs with a 50pF load)

Parameter	Symbol	Min	Typ	Max	Unit
DATA<7:0> access time from active read	t_{ADR}			15	ns
DATA<7:0> hold from inactive read	t_{HDR}	4			ns
DATA<7:0> High impedance from inactive read	t_{ZDR}			13	ns
Valid read pulse width	t_{VRD}	20			ns
Inactive read to inactive INT (due to reset on read feature)	t_{INTH} [3]	T + 6		2*T + 21	ns

1. For non-multiplexed Address and Data bus (ASB tied high)
2. For multiplexed Address and Data bus (ASB used as address latch enable)
3. T is the minimum cycle time of either DTCi, either, DRETCKREF, or MTCi (typically 488 ns for E1)

Figure 11. Microprocessor Write Timing

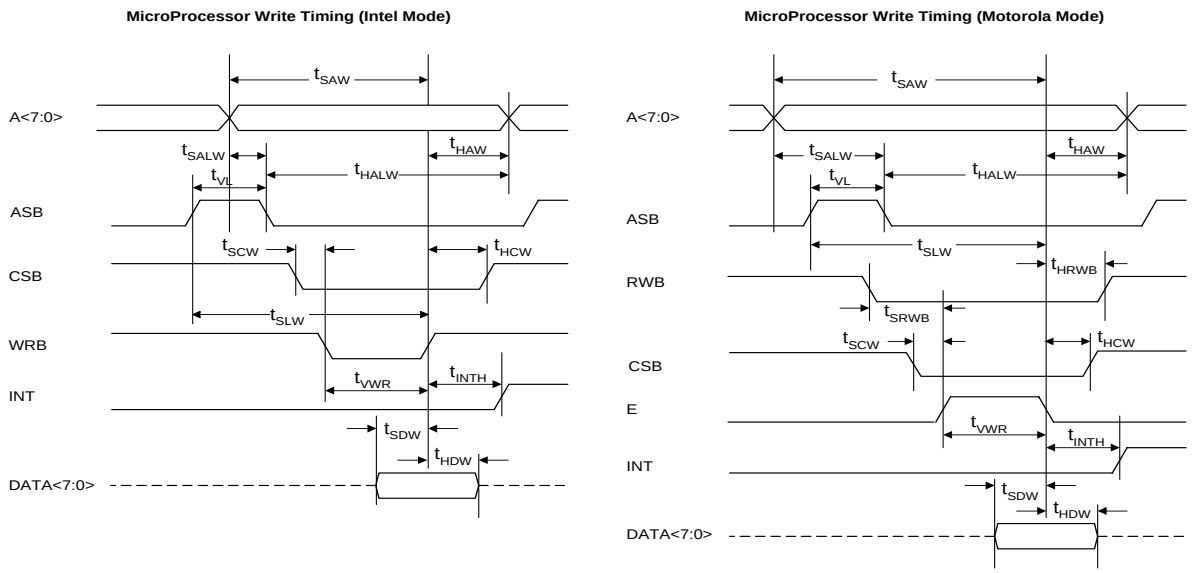


Table 12. Microprocessor Data Write Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
A<7:0> setup time to write cycle end	t_{SAW}	6			ns
A<7:0> hold time from inactive write	t_{HAW} [1]	2			ns
A<7:0> setup time to latch	t_{SALW} [2]	4			ns
A<7:0> hold time from latch	t_{HALW} [2]	2			ns
Valid latch pulse width	t_{VL} [2]	5			ns
ASB rising edge to write cycle end setup	t_{SLW} [2]	7			ns

1. For non-multiplexed Address and Data bus (AS tied high)
2. For multiplexed Address and Data bus (AS used as address latch enable)
3. T is the minimum cycle time of either DTCi, either, DRETCKREF, or MTCi (typically 488 ns for E1)

Table 12. Microprocessor Data Write Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
RWB setup to active write	t_{SRWB}	0			ns
RWB hold from inactive write	t_{HRWB}	1			ns
CSB setup to active write	t_{SCW}	1			ns
CSB hold from inactive write	t_{HCW}	1			ns
DATA<7:0> setup to inactive write	t_{SDW}	2			ns
DATA<7:0> hold from inactive write	t_{HDW}	2			ns
Valid write pulse width	t_{VWR}	20			ns
Inactive write to inactive INT (due to interrupt masking)	t_{VWR} [3]	T + 6		2*T + 21	ns

1. For non-multiplexed Address and Data bus (AS tied high)
2. For multiplexed Address and Data bus (AS used as address latch enable)
3. T is the minimum cycle time of either DTCi, either, DRETCKREF, or MTCi (typically 488 ns for E1)

6.0 Testability

The LXT6282 provides a method for enhancing testability: IEEE1149.1 Boundary Scan (JTAG) is used for testing of the interconnect.

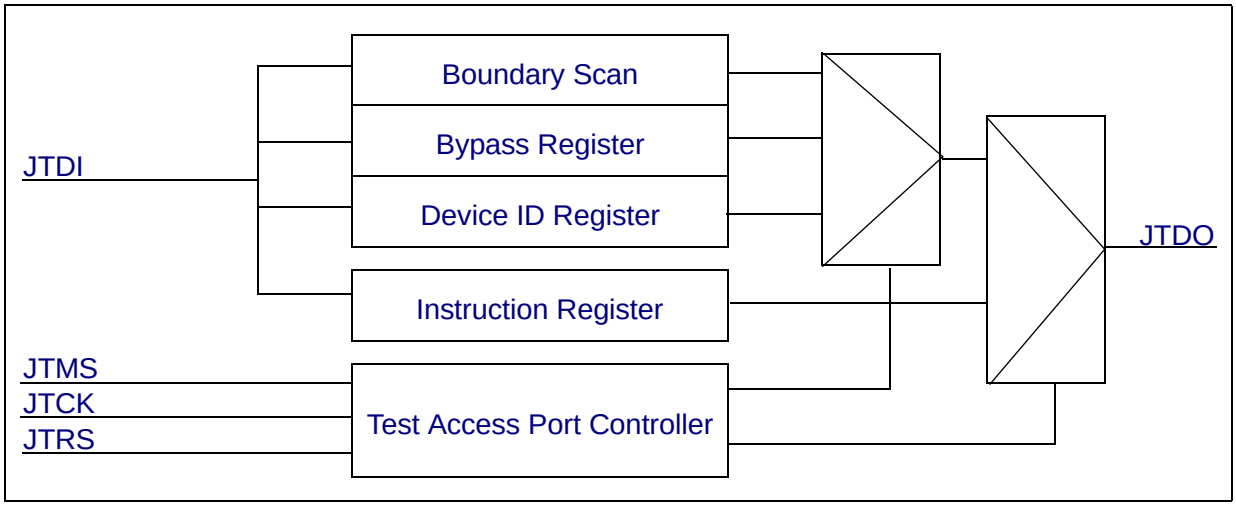
6.1 IEEE 1149.1 Boundary Scan Description

The boundary scan circuitry allows the user to test the interconnection between the LXT6282 and the circuit board. The boundary scan port consists of 5 pins as shown in Table 13. The heart of the scan circuitry is the Test Access Port controller (TAP). The TAP controller is a 16 state machine that controls the function of the boundary scan circuitry. Inputs of the TAP controller are the Test Mode Select (JTMS) and the Test Clock (JTCK) signals. Data and instructions are shifted into the LXT6282 through the Test Data In pin (JTDI). Data and instructions are shifted out through the Test Data Out pin (JTDO). An asynchronous reset pin (JTRS) allows to reset the boundary scan circuitry

Table 13. JTAG Pin Description

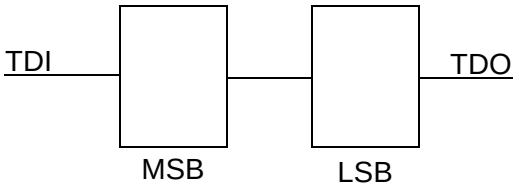
Pin #	Name	I/O	Function
103	JTMS_P	I	Test Mode Select: Determines state of TAP Controller. Pull up 48k
104	JTCK_P	I	Test Clock: Clock for all boundary scan circuitry
102	JTRS_P	I	Test Reset: Active low asynchronous signal that causes the TAP controller to reset. Pull down 35k
101	JTDI_P	I	Test Data In: Input signal used to shift in instructions and data. Pull up 48k
100	JTDO_P	O	Test data Out: Output signal used to shift out instructions and data.

Figure 12. Test Access Port



6.1.1 Instruction Register and Definitions

The LXT6282 supports the following instructions IEEE1149.1: EXTEST, SAMPLE/PRELOAD, BYPASS and IDCODE. Instructions are shifted into the instruction register during the SHIFT-IR state and become active upon exiting the UPDATE-IR state. The instruction register definition is shown in the following figure.



6.1.1.1 EXTEST (‘b00)

This instruction allows the testing of circuitry external to the package, typically the board interconnect, to be tested. While the instruction is active, the boundary scan register is connected between TDI and TDO for any data shifts. Boundary scan cells at the output pins are used to apply test stimuli, while those at input pins capture test results. Signals present on input pins are loaded into the BSR inputs cells on the rising edge of JTCK during CAPTURE-DR state. BSR contains are shifted one bit location on each rising edge of JTCK during the SHIFT-DR state. BSR output cell contents appear at output pins on the falling edge of JTCK during the UPDATE-IR state.

One test cycle is:

1. A test stimuli pattern is shifted into the BSR during SHIFT-DR state
2. This pattern is applied to output pins during the UPDATE-DR state
3. The response is loaded into input BSR cells during the CAPTURE-DR state
4. The results are shifted out and next test stimuli shifted in to the BSR

6.1.1.2 SAMPLE/PRELOAD (‘b01)

This instruction allows a snapshot of the normal operation of the LXT6282. The boundary scan register is connected between the TDI and TDO for any data shifts while this instruction is active. All BSR cells capture data present at their inputs on the rising edge of JTCK during the CAPTURE-DR state. No action is taken during the UPDATE-DR state.

6.1.1.3 BYPASS (‘b11)

This instruction allows a device to be effectively removed from the scan chain by inserting a one-bit shift register stage between TDI and TDO during data shifts. When the instruction is active, the test logic has no impact upon the system logic performing its system function. When selected, the shift-register is set to a logic zero on the rising edge of the JTCK during the CAPTURE-DR state.

6.1.1.4 IDCODE (‘b10)

This instruction allows the reading of component types via the scan chain. During this instruction, the 32-bit Device Identification Register (ID-Register) is placed between TDI and TDO. The ID Register captures a fixed value of (‘h 1188A0FD) on the rising edge of JTCK during the CAPTURE-DR state. The Device Identification Register contains the following information: Manufacturer ID: ‘d126; Design Part Number: ‘d LXT6282; Design Version Number: ‘d1.

6.1.2 Boundary Scan Register

The Boundary Scan Register is a 126 bit shift register, made of two types of 4 types of shift-register cells. According to the Boundary Scan Description Language (BSDL) JTAG_BSRINBOTH, JTAG_BSROUTBOTH and JTAG_BSRCTL are designated TYPE2, JTAG_BSRINCLKOBS are designated TYPE1.

Description

- Length: 126 BSR cells
- JTCK_P Jtag Test Clock
- JTDI_P Jtag Test Data Input
- JTDO_C Jtag Test Data Output Control enable
- JTDO_P Jtag Test Data Output
- JTMS_P Jtag Test Mode Select
- JTRS_P Jtag Test Reset

Figure 13. Boundary Scan Cell

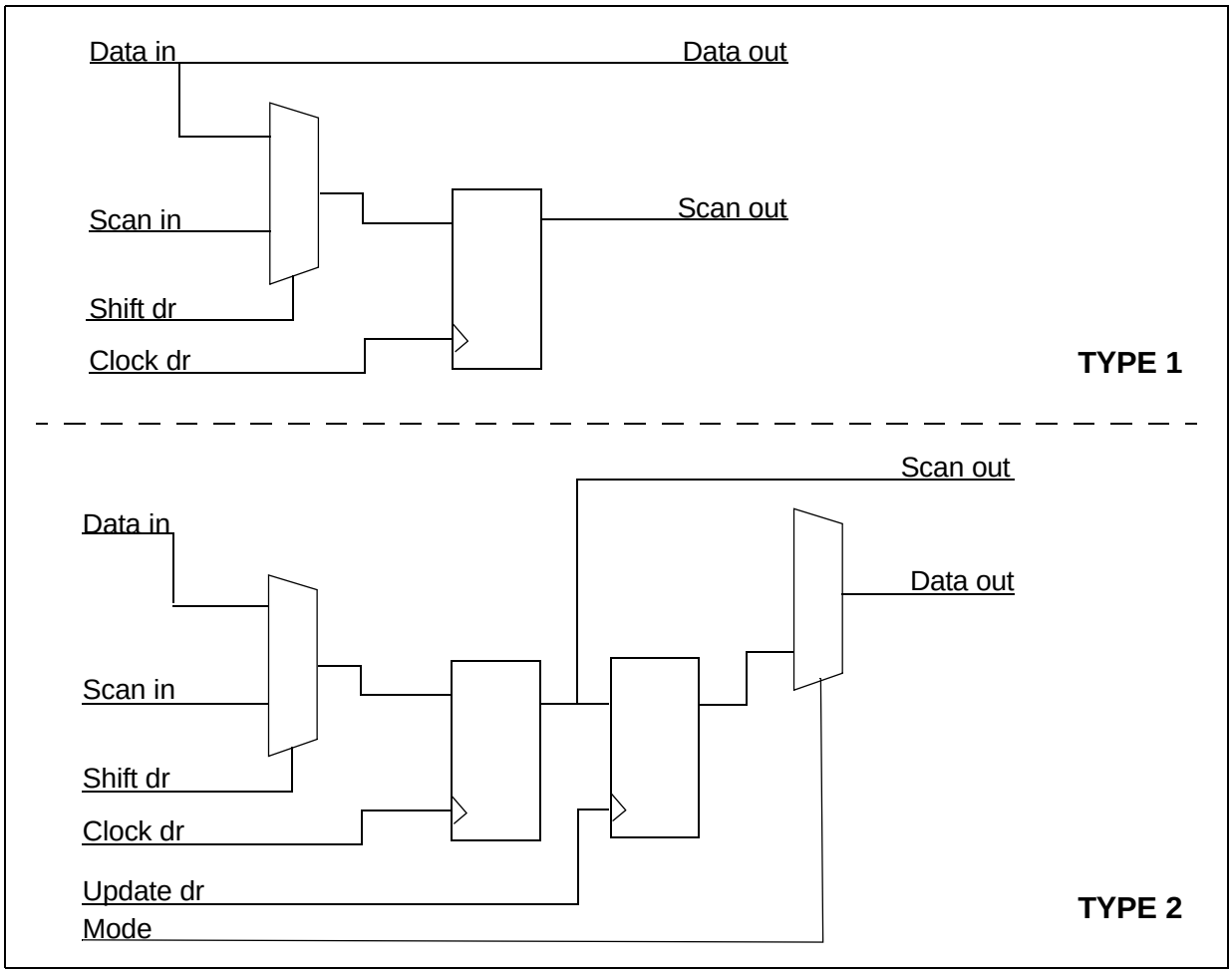


Table 14. Boundary Scan Order

dpllckref	Clock	1	JTAG_BSRINCLKOBS	
mcutype	Data	2	JTAG_BSRINBOTH	
scanen	Data	3	JTAG_BSRINBOTH	
scantest	Data	4	JTAG_BSRINBOTH	
dretckref	Clock	5	JTAG_BSRINCLKOBS	
oen	Data	6	JTAG_BSRINBOTH	
dtc[7]	Data	7	JTAG_BSRINBOTH	
dtd[7]	Data	8	JTAG_BSRINBOTH	
mtd[7]	Data	9	JTAG_BSROUTBOTH	
mtc[7]	Data	10	JTAG_BSROUTBOTH	oen_c
mtc[6]	Data	11	JTAG_BSROUTBOTH	oen_c
mtd[6]	Data	12	JTAG_BSROUTBOTH	oen_c

Table 14. Boundary Scan Order

dtd[6]	Data	13	JTAG_BSRINBOTH	
dtc[6]	Data	14	JTAG_BSRINBOTH	
dtc[5]	Data	15	JTAG_BSRINBOTH	
dtd[5]	Data	16	JTAG_BSRINBOTH	
mtd[5]	Data	17	JTAG_BSROUTBOTH	oen_c
mtc[5]	Data	18	JTAG_BSROUTBOTH	oen_c
mtc[4]	Data	19	JTAG_BSROUTBOTH	oen_c
mtd[4]	Data	20	JTAG_BSROUTBOTH	oen_c
dtd[4]	Data	21	JTAG_BSRINBOTH	
dtc[4]	Data	22	JTAG_BSRINBOTH	
dtc[3]	Data	23	JTAG_BSRINBOTH	
dtd[3]	Data	24	JTAG_BSRINBOTH	
mtd[3]	Data	25	JTAG_BSROUTBOTH	oen_c
mtc[3]	Data	26	JTAG_BSROUTBOTH	oen_c
mtc[2]	Data	27	JTAG_BSROUTBOTH	oen_c
mtd[2]	Data	28	JTAG_BSROUTBOTH	oen_c
dtd[2]	Data	29	JTAG_BSRINBOTH	
dtc[2]	Data	30	JTAG_BSRINBOTH	
dtc[1]	Data	31	JTAG_BSRINBOTH	
dtd[1]	Data	32	JTAG_BSRINBOTH	
mtd[1]	Data	33	JTAG_BSROUTBOTH	oen_c
mtc[1]	Data	34	JTAG_BSROUTBOTH	oen_c
mtc[0]	Data	35	JTAG_BSROUTBOTH	oen_c
mtd[0]	Data	36	JTAG_BSROUTBOTH	oen_c
dtd[0]	Data	37	JTAG_BSRINBOTH	
dtc[0]	Data	38	JTAG_BSRINBOTH	
data/i[7]	Data	39	JTAG_BSRINBOTH	
data/o[7]	Data	40	JTAG_BSROUTBOTH	rdb_c
data/i[6]	Data	41	JTAG_BSRINBOTH	
data/o[6]	Data	42	JTAG_BSROUTBOTH	rdb_c
data/i[5]	Data	43	JTAG_BSRINBOTH	
data/o[5]	Data	44	JTAG_BSROUTBOTH	rdb_c
data/i[4]	Data	45	JTAG_BSRINBOTH	
data/o[4]	Data	46	JTAG_BSROUTBOTH	rdb_c
data/i[3]	Data	47	JTAG_BSRINBOTH	
data/o[3]	Data	48	JTAG_BSROUTBOTH	rdb_c
data/i[2]	Data	49	JTAG_BSRINBOTH	
data/o[2]	Data	50	JTAG_BSROUTBOTH	rdb_c
data/i[1]	Data	51	JTAG_BSRINBOTH	

Table 14. Boundary Scan Order

data/o[1]	Data	52	JTAG_BSROUTBOTH	rdb_c
data/i[0]	Data	53	JTAG_BSRINBOTH	
data/o[0]	Data	54	JTAG_BSROUTBOTH	rdb_c
oen_c	Enble	55	JTAG_BSRCTL	
rdb_c	Enble	56	JTAG_BSRCTL	
a[7]	Data	57	JTAG_BSRINBOTH	
a[6]	Data	58	JTAG_BSRINBOTH	
a[5]	Data	59	JTAG_BSRINBOTH	
a[4]	Data	60	JTAG_BSRINBOTH	
a[3]	Data	61	JTAG_BSRINBOTH	
a[2]	Data	62	JTAG_BSRINBOTH	
a[1]	Data	63	JTAG_BSRINBOTH	
a[0]	Data	64	JTAG_BSRINBOTH	
csb	Data	65	JTAG_BSRINBOTH	
asb	Data	66	JTAG_BSRINBOTH	
wrb	Data	67	JTAG_BSRINBOTH	
rdb	Data	68	JTAG_BSRINBOTH	
reset	Data	69	JTAG_BSRINBOTH	
int	Enble	70	JTAG_BSRCTL	int
rlos[0]	Data	71	JTAG_BSRINBOTH	
rnegd[0]	Data	72	JTAG_BSRINBOTH	
rposd[0]	Data	73	JTAG_BSRINBOTH	
rclk[0]	Data	74	JTAG_BSRINBOTH	
tnegd[0]	Data	75	JTAG_BSROUTBOTH	oen_c
tposd[0]	Data	76	JTAG_BSROUTBOTH	oen_c
tclk[0]	Data	77	JTAG_BSROUTBOTH	oen_c
rlos[1]	Data	78	JTAG_BSRINBOTH	
rnegd[1]	Data	79	JTAG_BSRINBOTH	
rposd[1]	Data	80	JTAG_BSRINBOTH	
rclk[1]	Data	81	JTAG_BSRINBOTH	
tnegd[1]	Data	82	JTAG_BSROUTBOTH	oen_c
tposd[1]	Data	83	JTAG_BSROUTBOTH	oen_c
tclk[1]	Data	84	JTAG_BSROUTBOTH	oen_c
rlos[3]	Data	85	JTAG_BSRINBOTH	
rnegd[3]	Data	86	JTAG_BSRINBOTH	
rposd[3]	Data	87	JTAG_BSRINBOTH	
rclk[3]	Data	88	JTAG_BSRINBOTH	
tnegd[3]	Data	89	JTAG_BSROUTBOTH	oen_c
tposd[3]	Data	90	JTAG_BSROUTBOTH	oen_c

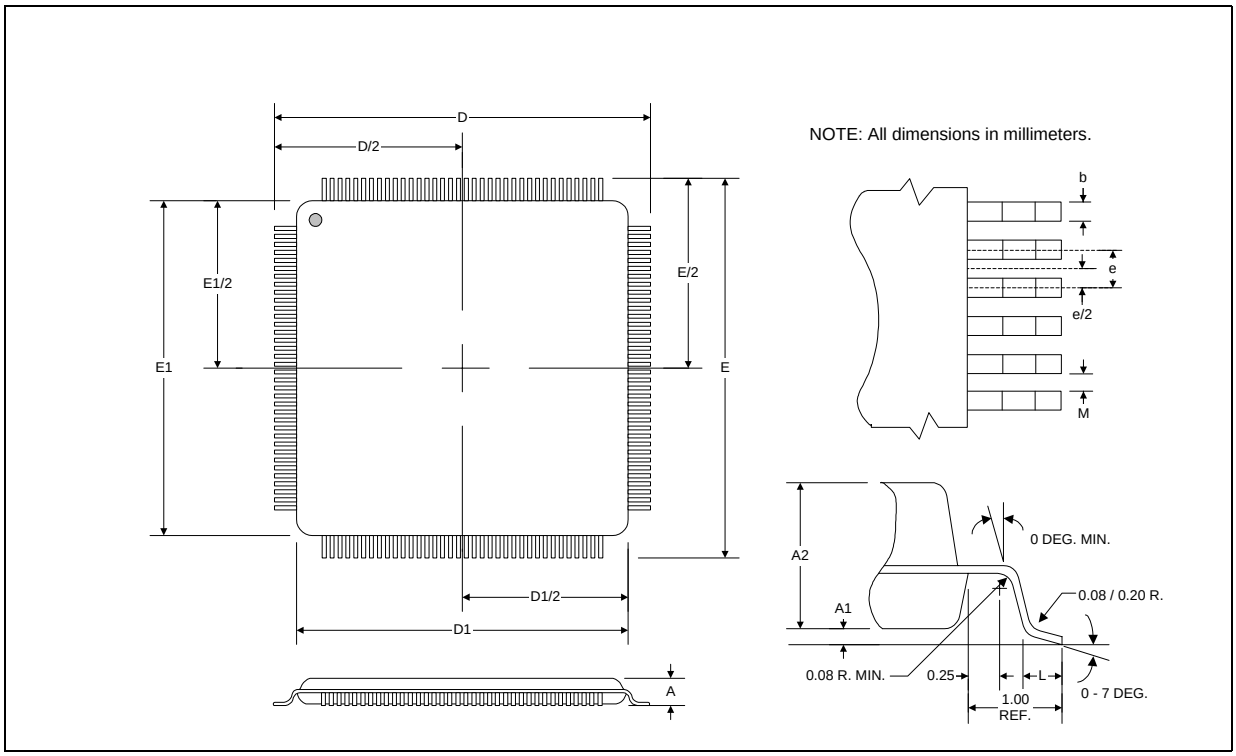
Table 14. Boundary Scan Order

tclk[3]	Data	91	JTAG_BSROUTBOTH	oen_c
rlos[2]	Data	92	JTAG_BSRINBOTH	
rnegd[2]	Data	93	JTAG_BSRINBOTH	
rposd[2]	Data	94	JTAG_BSRINBOTH	
rclk[2]	Data	95	JTAG_BSRINBOTH	
tnegd[2]	Data	96	JTAG_BSROUTBOTH	oen_c
tposd[2]	Data	97	JTAG_BSROUTBOTH	oen_c
tclk[2]	Data	98	JTAG_BSROUTBOTH	oen_c
tclk[5]	Data	99	JTAG_BSROUTBOTH	oen_c
tposd[5]	Data	100	JTAG_BSROUTBOTH	oen_c
tnegd[5]	Data	101	JTAG_BSROUTBOTH	oen_c
rclk[5]	Data	102	JTAG_BSRINBOTH	
rposd[5]	Data	103	JTAG_BSRINBOTH	
rnegd[5]	Data	104	JTAG_BSRINBOTH	
rlos[5]	Data	105	JTAG_BSRINBOTH	
tclk[4]	Data	106	JTAG_BSROUTBOTH	oen_c
tposd[4]	Data	107	JTAG_BSROUTBOTH	oen_c
tnegd[4]	Data	108	JTAG_BSROUTBOTH	oen_c
rclk[4]	Data	109	JTAG_BSRINBOTH	
rposd[4]	Data	110	JTAG_BSRINBOTH	
rnegd[4]	Data	111	JTAG_BSRINBOTH	
rlos[4]	Data	112	JTAG_BSRINBOTH	
tclk[6]	Data	113	JTAG_BSROUTBOTH	oen_c
tposd[6]	Data	114	JTAG_BSROUTBOTH	oen_c
tnegd[6]	Data	115	JTAG_BSROUTBOTH	oen_c
rclk[6]	Data	116	JTAG_BSRINBOTH	
rposd[6]	Data	117	JTAG_BSRINBOTH	
rnegd[6]	Data	118	JTAG_BSRINBOTH	
rlos[6]	Data	119	JTAG_BSRINBOTH	
tclk[7]	Data	120	JTAG_BSROUTBOTH	oen_c
tposd[7]	Data	121	JTAG_BSROUTBOTH	oen_c
tnegd[7]	Data	122	JTAG_BSROUTBOTH	oen_c
rclk[7]	Data	123	JTAG_BSRINBOTH	
rposd[7]	Data	124	JTAG_BSRINBOTH	
rnegd[7]	Data	125	JTAG_BSRINBOTH	
rlos[7]	Data	126	JTAG_BSRINBOTH	

7.0 Glossary

AIS	Alarm Indication Signal
FAS	E-1 Frame Alignment Signal
FIFO	First in/First Out Memory
MFAS	E1 CRC-4 Multiframe Alignment Signal
NFAS	E1 Non-Frame Alignment Signal
PDH	Synchronous Digital Hierarchy
SDH	Synchronous Digital Hierarchy

8.0 Package Information



144-pin L Quad Flat Pack package (1.40 mm body thickness)

Dimension[1]	Millimeters		
	Minimum	Nominal	Maximum
A	-	-	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
D	22.00 B.S.C.		
D1	20.00 B.S.C.		
E	22.00 B.S.C.		
E1	20.00 B.S.C.		
e	0.50 B.S.C.		
L	0.45	0.60	0.75
M	0.14	-	-
1. See JEDEC Publication for additional specifications.			