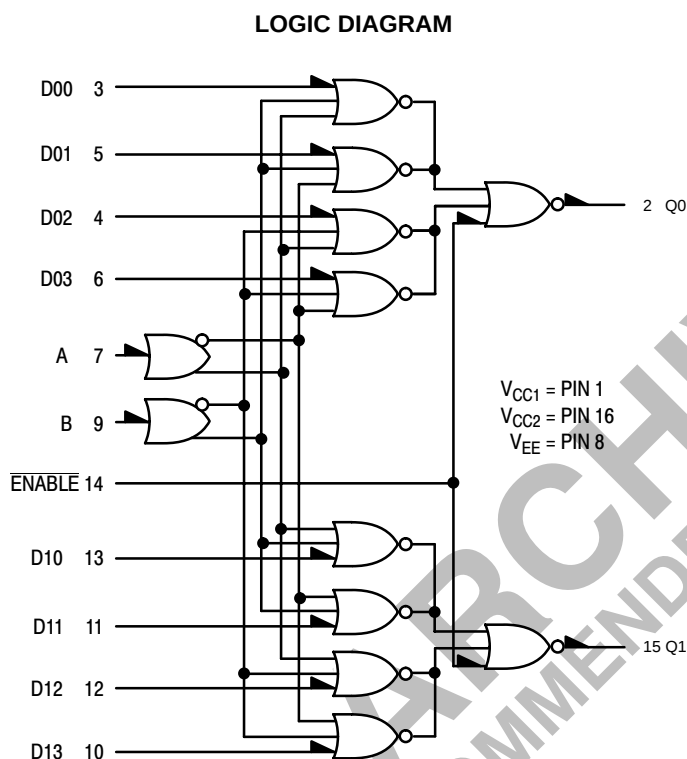


MC10174

Dual 4 to 1 Multiplexer

The MC10174 is a high speed dual channel multiplexer with output enable capability. The select inputs determine one of four active data inputs for each multiplexer. An output enable forces both outputs low when in the high state.

- $P_D = 305 \text{ mW typ/pkg (No Load)}$
- $t_{pd} = 3.5 \text{ ns typ (Dta to output)}$
- $t_r, t_f = 2.0 \text{ ns typ (20\%–80\%)}$



TRUTH TABLE

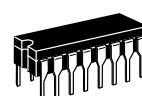
ENABLE	ADDRESS INPUTS		OUTPUTS	
$\bar{E}$	B	A	Q0	Q1
H	X	X	L	L
L	L	L	D00	D10
L	L	H	D01	D11
L	H	L	D02	D12
L	H	H	D03	D13



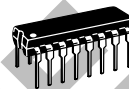
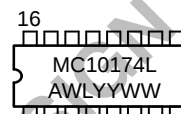
ON Semiconductor

<http://onsemi.com>

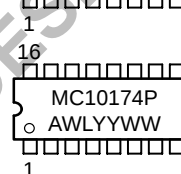
MARKING DIAGRAMS



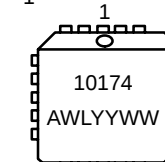
CDIP-16
L SUFFIX
CASE 620



PDIP-16
P SUFFIX
CASE 648

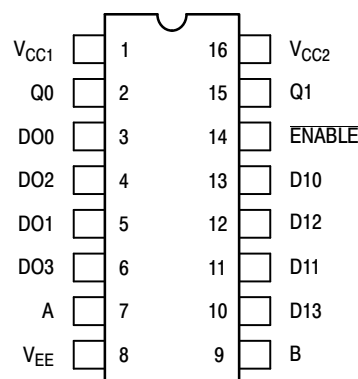


PLCC-20
FN SUFFIX
CASE 775



A = Assembly Location
 WL = Wafer Lot
 YY = Year
 WW = Work Week

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package.
 For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).

ORDERING INFORMATION

Device	Package	Shipping
MC10174L	CDIP-16	25 Units / Rail
MC10174P	PDIP-16	25 Units / Rail
MC10174FN	PLCC-20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			-30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I _E	8		80		58	73	80		mAdc
Input Current	I _{inH}	4 14		350 525			220 330		220 330	μAdc
	I _{inL}	4	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	V _{OH}	15	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc
Output Voltage Logic 0	V _{OL}	15	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc
Threshold Voltage Logic 1	V _{OHA}	15	-1.080		-0.980			-0.910		Vdc
Threshold Voltage Logic 0	V _{OLA}	15		-1.655			-1.630		-1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t ₁₃₊₁₅₊	15	1.4	5.0	1.5	3.5	4.7	1.4	5.0	
	t ₁₃₋₁₅₋	15	1.4	5.0	1.5	3.5	4.7	1.4	5.0	
	t ₇₊₁₅₋	15	1.9	6.6	2.0	5.0	6.2	2.1	6.6	
	t ₇₋₁₅₊	15	1.9	6.6	2.0	5.0	6.2	2.1	6.6	
	t ₁₄₊₁₅₋	15	1.0	3.3	1.0	2.0	3.1	0.9	3.4	
	t ₁₄₋₁₅₊	15	1.0	3.3	1.0	2.0	3.1	0.9	3.4	
Rise Time (20 to 80%)	t ₊	15	1.0	3.4	1.1	2.0	3.3	1.1	3.6	
Fall Time (20 to 80%)	t ₋	15	1.0	3.4	1.1	2.0	3.3	1.1	3.6	

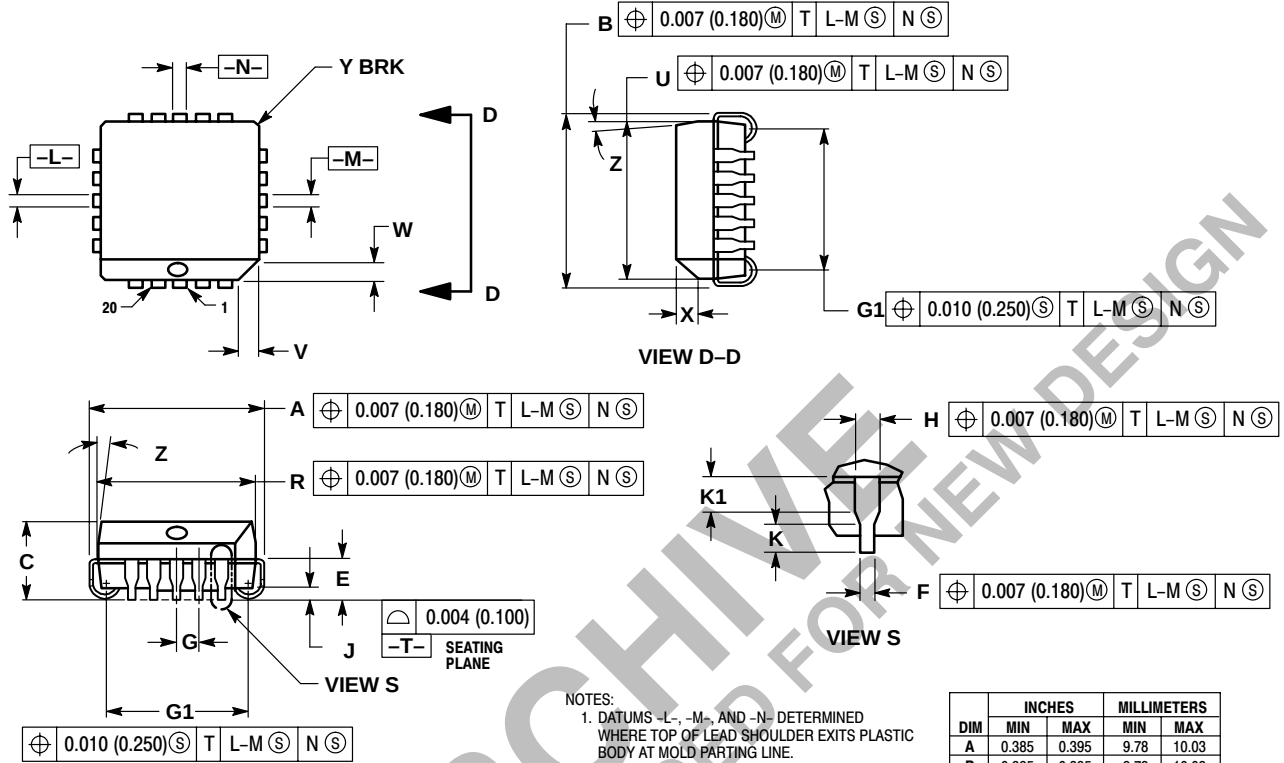
ELECTRICAL CHARACTERISTICS (continued)

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.			TEST VOLTAGE VALUES (Volts)					(V _{CC}) Gnd
			@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHmin}	V_{ILmax}	V_{EE}
			-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
			+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
			+85°C	-0.700	-1.825	-1.035	-1.440	-5.2
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V _{CC}) Gnd
			V_{IHmax}	V_{ILmin}	V_{IHmin}	V_{ILmax}	V_{EE}	
Power Supply Drain Current	I_E	8					8	1, 16
Input Current	I_{inH}	4 14	4 14				8 8	1, 16 1, 16
	I_{inL}	4		4			8	1, 16
Output Voltage Logic 1	V_{OH}	15	13				8	1, 16
Output Voltage Logic 0	V_{OL}	15	14				8	1, 16
Threshold Voltage Logic 1	V_{OHA}	15			13		8	1, 16
Threshold Voltage Logic 0	V_{OLA}	15			14		8	1, 16
Switching Times (50 Ω Load)			+1.11V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{13+15+}	15			13	15	8	1, 16
	t_{13-15-}	15			13	15	8	1, 16
	t_{7+15-}	15	11		7	15	8	1, 16
	t_{7-15+}	15	11		7	15	8	1, 16
	t_{14+15-}	15	13		14	15	8	1, 16
	t_{14-15+}	15	13		14	15	8	1, 16
Rise Time (20 to 80%)	t_+	15	13		14	15	8	1, 16
Fall Time (20 to 80%)	t_-	15	13		14	15	8	1, 16

MC10174

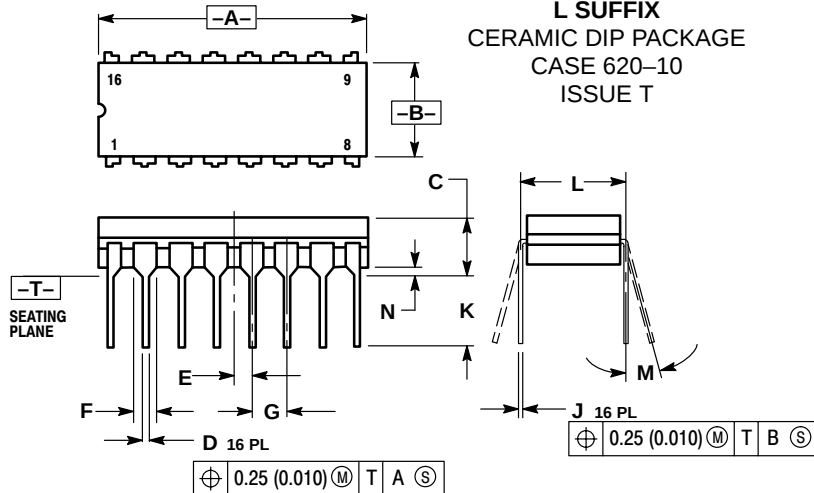
PACKAGE DIMENSIONS

PLCC-20
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775-02
ISSUE C



MC10174

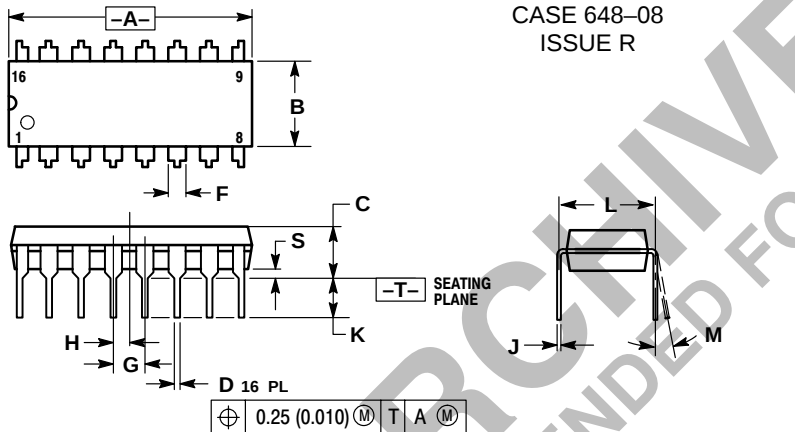
CDIP-16 L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE T



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	---	0.200	---	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

PDIP-16 P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

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