

SN54ALS169B, SN54AS169A, SN74ALS169B, SN74AS169A SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

SDAS125B – MARCH 1984 – REVISED DECEMBER 1994

- Fully Synchronous Operation for Counting and Programming
- Internal Carry Look-Ahead Circuitry for Fast Counting
- Carry Output for n-Bit Cascading
- Fully Independent Clock Circuit
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

These synchronous 4-bit up/down binary presettable counters feature an internal carry look-ahead circuitry for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable (\overline{ENP} , \overline{ENT}) inputs and internal gating. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

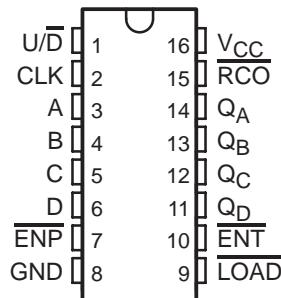
These counters are fully programmable; that is, they may be preset to either level. The load-input circuitry allows loading with the carry-enable output of cascaded counters. Because loading is synchronous, setting up a low level at the load (LOAD) input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The internal carry look-ahead circuitry provides for cascading counters for n-bit synchronous application without additional gating. \overline{ENP} and \overline{ENT} inputs and a ripple-carry output (RCO) are instrumental in accomplishing this function. Both \overline{ENP} and \overline{ENT} must be low to count. The direction of the count is determined by the level of the up/down (U/D) input. When U/D is high, the counter counts up; when low, it counts down. \overline{ENT} is fed forward to enable RCO. RCO, thus enabled, produces a low-level pulse while the count is zero (all inputs low) counting down or maximum (15) counting up. This low-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at \overline{ENP} or \overline{ENT} are allowed regardless of the level of the clock input. All inputs are diode clamped to minimize transmission-line effects, thereby simplifying system design.

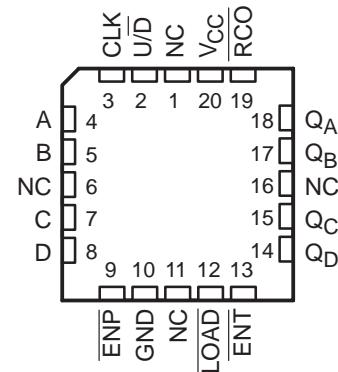
These counters feature a fully independent clock circuit. Changes at control inputs (\overline{ENP} , \overline{ENT} , \overline{LOAD} , or U/D) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

The SN54ALS169B and SN54AS169A are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS169B and SN74AS169A are characterized for operation from 0°C to 70°C .

SN54ALS169B, SN54AS169A . . . J PACKAGE
SN74ALS169B, SN74AS169A . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS169B, SN54AS169A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

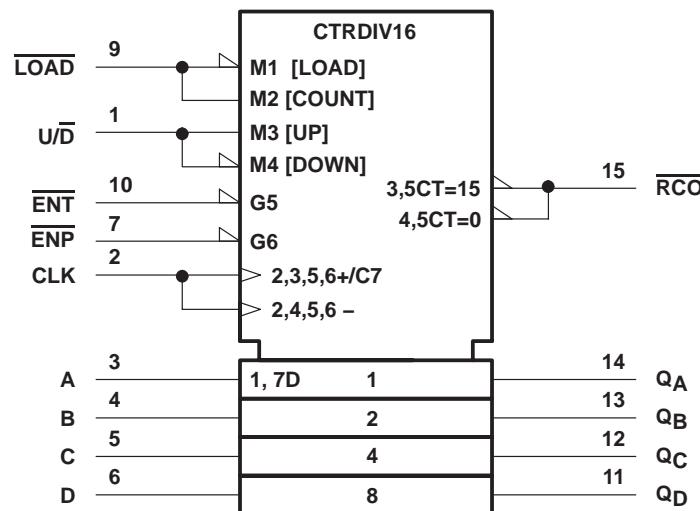


Copyright © 1994, Texas Instruments Incorporated

SN54ALS169B, SN54AS169A, SN74ALS169B, SN74AS169A SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

SDAS125B – MARCH 1984 – REVISED DECEMBER 1994

logic symbol†

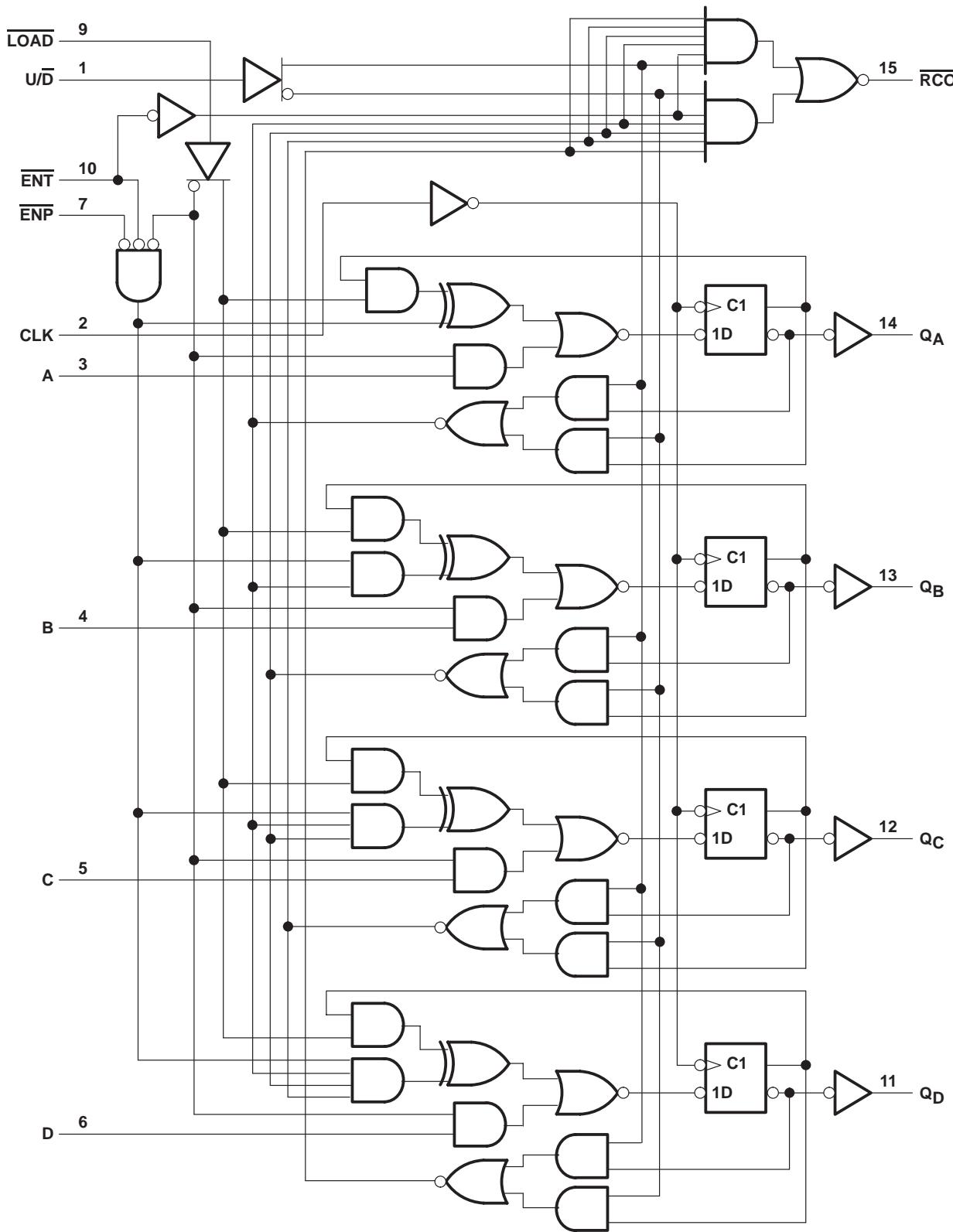


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

SN54ALS169B, SN54AS169A, SN74ALS169B, SN74AS169A SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

SDAS125B – MARCH 1984 – REVISED DECEMBER 1994

logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251-1443

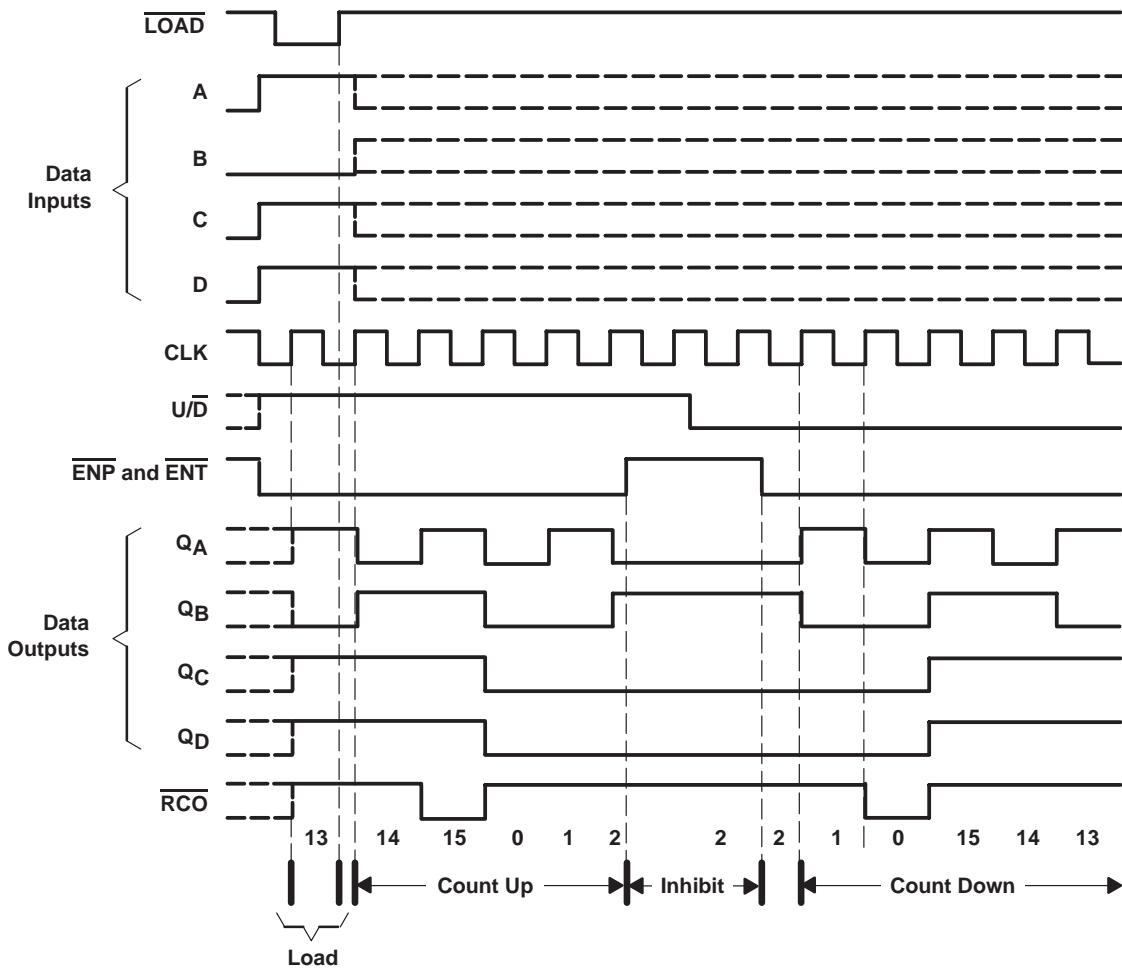
SN54ALS169B, SN54AS169A, SN74ALS169B, SN74AS169A SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

SDAS125B – MARCH 1984 – REVISED DECEMBER 1994

typical load, count, and inhibit sequences

The following sequence is illustrated below:

1. Load (preset) to binary 13
2. Count up to 14, 15 (maximum), 0, 1, and 2
3. Inhibit
4. Count down to 1, 0 (minimum), 15, 14, and 13



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SN54ALS169B, SN54AS169A, SN74ALS169B, SN74AS169A SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

SDAS125B – MARCH 1984 – REVISED DECEMBER 1994

recommended operating conditions

		SN54ALS169B			SN74ALS169B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current			-0.4			-0.4	mA
I _{OL}	Low-level output current			4			8	mA
f _{clock}	Clock frequency	0	22	0	0	40	40	MHz
t _w	Pulse duration, CLK high or low	14			12.5			ns
t _{su}	Setup time before CLK↑	A, B, C, or D	20		15			ns
		ENP or ENT	25		15			
		LOAD	20		15			
		U/D	28		15			
t _h	Hold time, data after CLK↑	0			0			ns
T _A	Operating free-air temperature	-55		125	0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS169B			SN74ALS169B			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA	V _{CC} - 2			V _{CC} - 2			V
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 4 mA	0.25	0.4	0.25	0.4		V
		I _{OL} = 8 mA			0.35	0.5		
I _I	V _{CC} = 5.5 V, V _I = 7 V			0.1			0.1	mA
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V			20			20	µA
I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V			-0.2			-0.2	mA
I _O ‡	V _{CC} = 5.5 V, V _O = 2.25 V	-20	-112		-30	-112		mA
I _{CC}	V _{CC} = 5.5 V	15	25		15	25		mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251-1443

SN54ALS169B, SN54AS169A, SN74ALS169B, SN74AS169A SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

SDAS125B – MARCH 1984 – REVISED DECEMBER 1994

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $C_L = 50 \text{ pF}$, $R_L = 500 \Omega$, $T_A = \text{MIN to MAX}^\dagger$				UNIT	
			SN54ALS169B		SN74ALS169B			
			MIN	MAX	MIN	MAX		
f_{max}			22	40			MHz	
t_{PLH}	CLK	$\overline{\text{RCO}}$	3	20	3	20	ns	
t_{PHL}			6	25	6	20		
t_{PLH}	CLK	Any Q	2	20	2	15	ns	
t_{PHL}			5	23	5	20		
t_{PLH}	$\overline{\text{ENT}}$	$\overline{\text{RCO}}$	2	16	2	13	ns	
t_{PHL}			3	24	3	16		
t_{PLH}	U/D	$\overline{\text{RCO}}$	4	22	5	19	ns	
t_{PHL}			5	26	5	19		

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Operating free-air temperature range, T_A : SN54AS169A	-55°C to 125°C
SN74AS169A	0°C to 70°C
Storage temperature range	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54AS169A			SN74AS169A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-2			-2	mA
I_{OL}	Low-level output current			20			20	mA
f_{clock}^*	Clock frequency	0	60	0	0	75		MHz
t_{w^*}	Pulse duration, CLK high or low	7.7			6.7			ns
t_{su}^*	Setup time before CLK^\uparrow	A, B, C, or D	10		8			ns
		ENP or ENT	10		8			
		LOAD	10		8			
		U/D	14		11			
t_h^*	Hold time, data after CLK^\uparrow	2			0			ns
T_A	Operating free-air temperature	-55		125	0		70	°C

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251-1443

SN54ALS169B, SN54AS169A, SN74ALS169B, SN74AS169A SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

SDAS125B – MARCH 1984 – REVISED DECEMBER 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS169A			SN74AS169A			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $I_{OH} = -2 \text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V
V_{OL}	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 20 \text{ mA}$		0.25	0.5		0.25	0.5	V
I_I	LOAD, ENT, U/D	$V_{CC} = 5.5 \text{ V}$, $V_I = 7 \text{ V}$		0.2		0.2		mA
	All others			0.1		0.1		
I_{IH}	LOAD, ENT, U/D	$V_{CC} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$		40		40		μA
	All others			20		20		
I_{IL}	LOAD, ENT, U/D	$V_{CC} = 5.5 \text{ V}$, $V_I = 0.4 \text{ V}$		-1		-1		mA
	All others			-0.5		-0.5		
I_O^\ddagger	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.25 \text{ V}$	-30	-112	-30	-112	-30	-112	mA
I_{CC}	$V_{CC} = 5.5 \text{ V}$		41	63		41	63	mA

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $C_L = 50 \text{ pF}$, $R_L = 500 \Omega$, $T_A = \text{MIN to MAX}^\S$				UNIT	
			SN54AS169A		SN74AS169A			
			MIN	MAX	MIN	MAX		
f_{max}^*			60		75		MHz	
t_{PLH}	CLK	\overline{RCO} (LOAD high or low)	3	17.5	3	16.5	ns	
			2	14	2	13		
t_{PHL}	CLK	Any Q	1	7.5	1	7	ns	
			2	14	2	13		
t_{PLH}	\overline{ENT}	\overline{RCO}	1.5	10	1.5	9	ns	
			1.5	10	1.5	9		
t_{PHL}	U/\overline{D}	\overline{RCO}	2	14	2	12	ns	
			2	14.5	2	13		

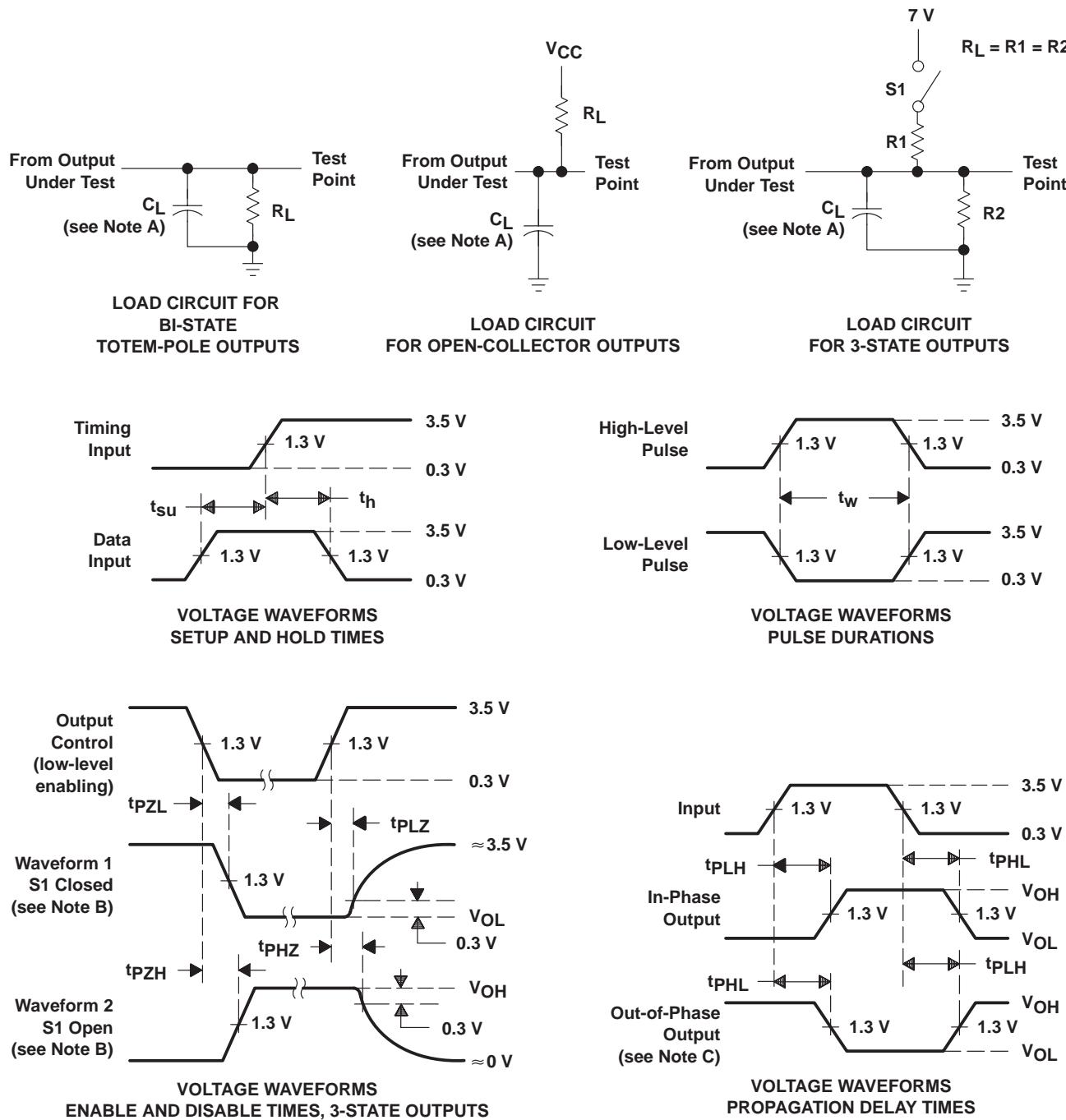
* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN54ALS169B, SN54AS169A, SN74ALS169B, SN74AS169A SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

SDAS125B – MARCH 1984 – REVISED DECEMBER 1994

PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1 \text{ MHz}$, $t_r = t_f = 2 \text{ ns}$, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
83025012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	83025012A SNJ54ALS 169BFK	Samples
8302501EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8302501EA SNJ54ALS169BJ	Samples
8302501FA	OBsolete	CFP	W	16		TBD	Call TI	Call TI	-55 to 125		
JM38510/38003B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 38003B2A	Samples
JM38510/38003BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 38003BEA	Samples
M38510/38003B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 38003B2A	Samples
M38510/38003BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 38003BEA	Samples
SN54ALS169BJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54ALS169BJ	Samples
SN54AS169AJ	OBsolete	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
SN74ALS169BD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS169B	Samples
SN74ALS169BDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS169B	Samples
SN74ALS169BN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS169BN	Samples
SN74ALS169BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS169B	Samples
SN74AS169AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74AS169AN	Samples
SNJ54ALS169BFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	83025012A SNJ54ALS 169BFK	Samples
SNJ54ALS169BJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8302501EA SNJ54ALS169BJ	Samples
SNJ54AS169AFK	OBsolete	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
SNJ54AS169AJ	OBsolete	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54ALS169B, SN54AS169A, SN74ALS169B, SN74AS169A :

• Catalog: [SN74ALS169B](#), [SN74AS169A](#)

• Military: [SN54ALS169B](#), [SN54AS169A](#)



www.ti.com

PACKAGE OPTION ADDENDUM

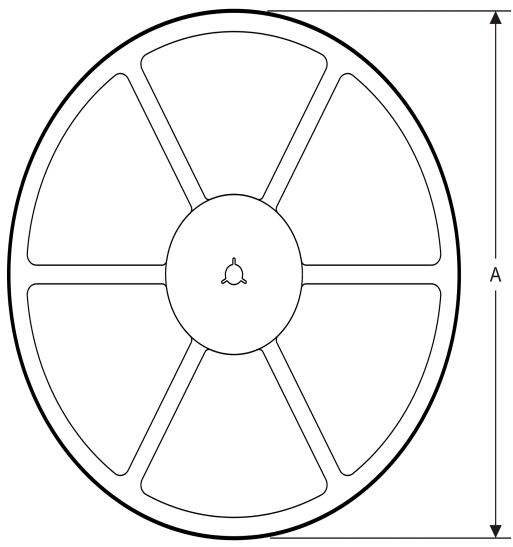
10-Jun-2014

NOTE: Qualified Version Definitions:

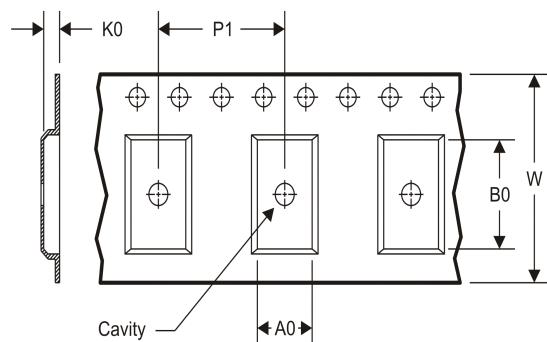
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

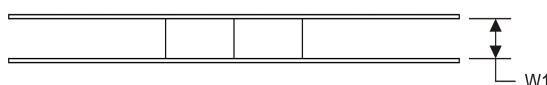
REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS169BDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74ALS169BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

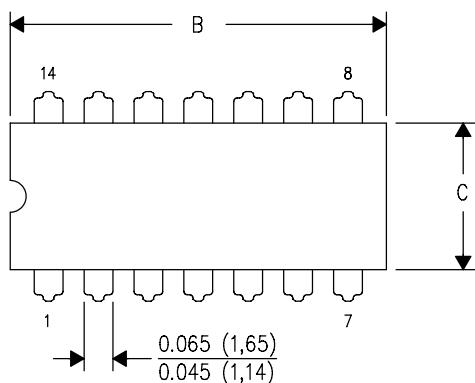

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS169BDR	SOIC	D	16	2500	333.2	345.9	28.6
SN74ALS169BNSR	SO	NS	16	2000	367.0	367.0	38.0

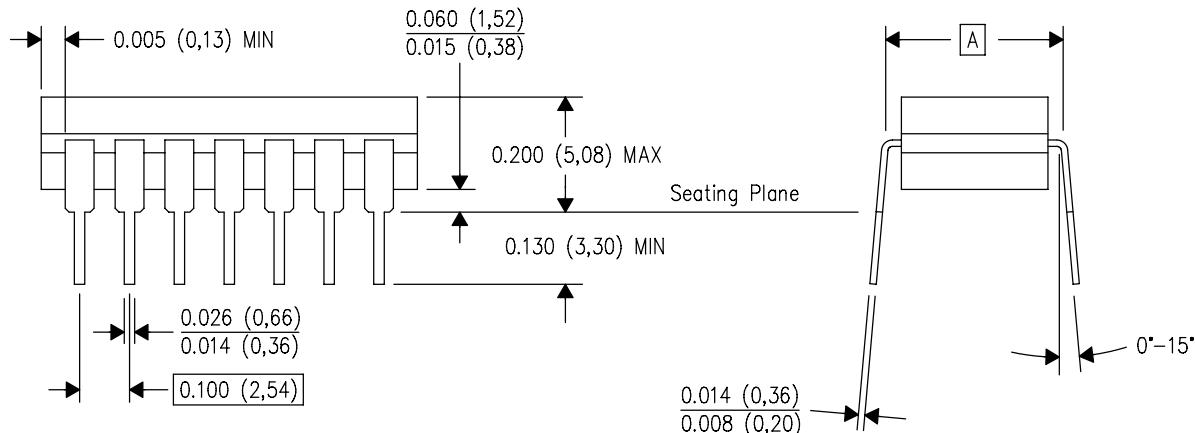
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

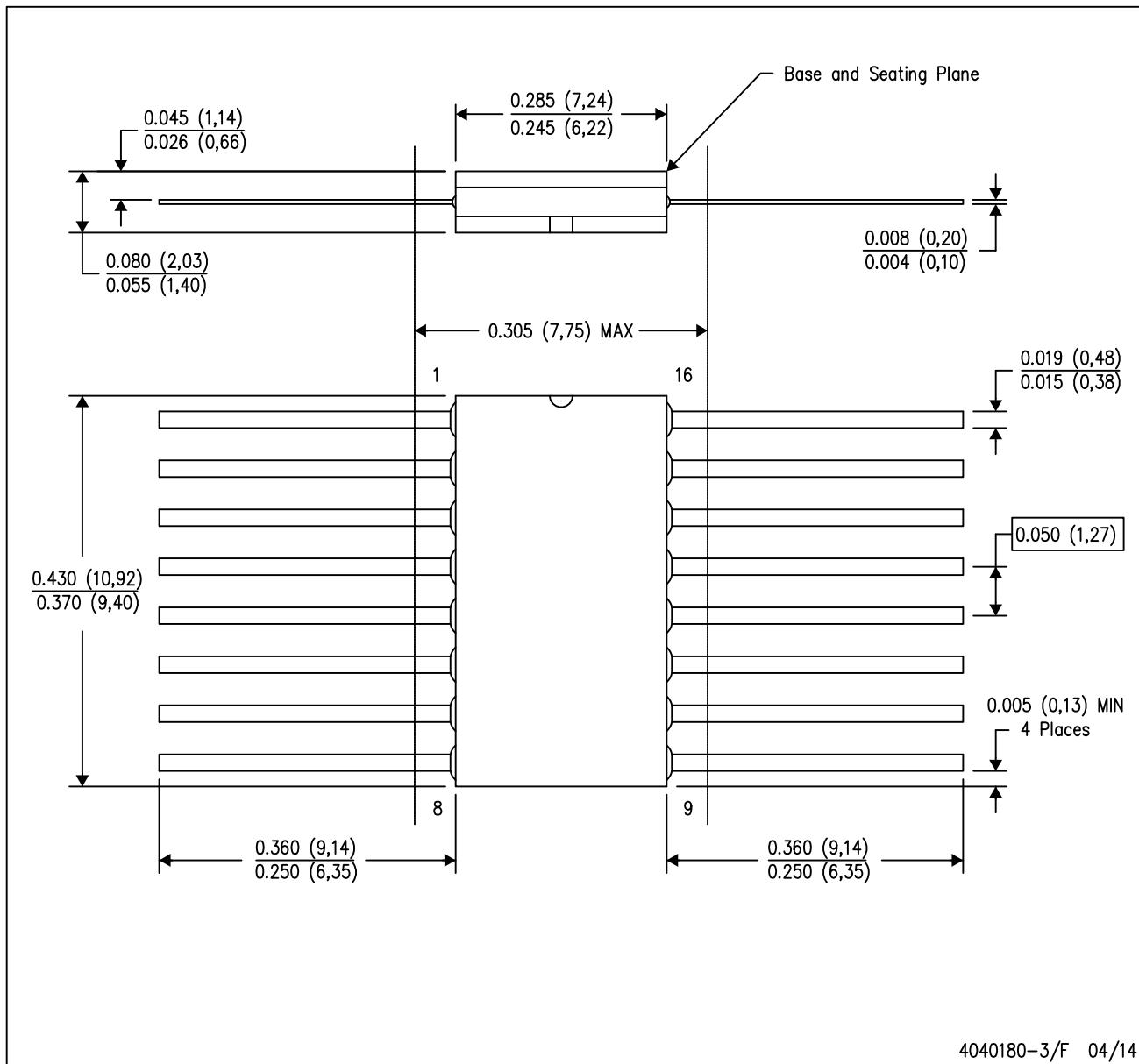


4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



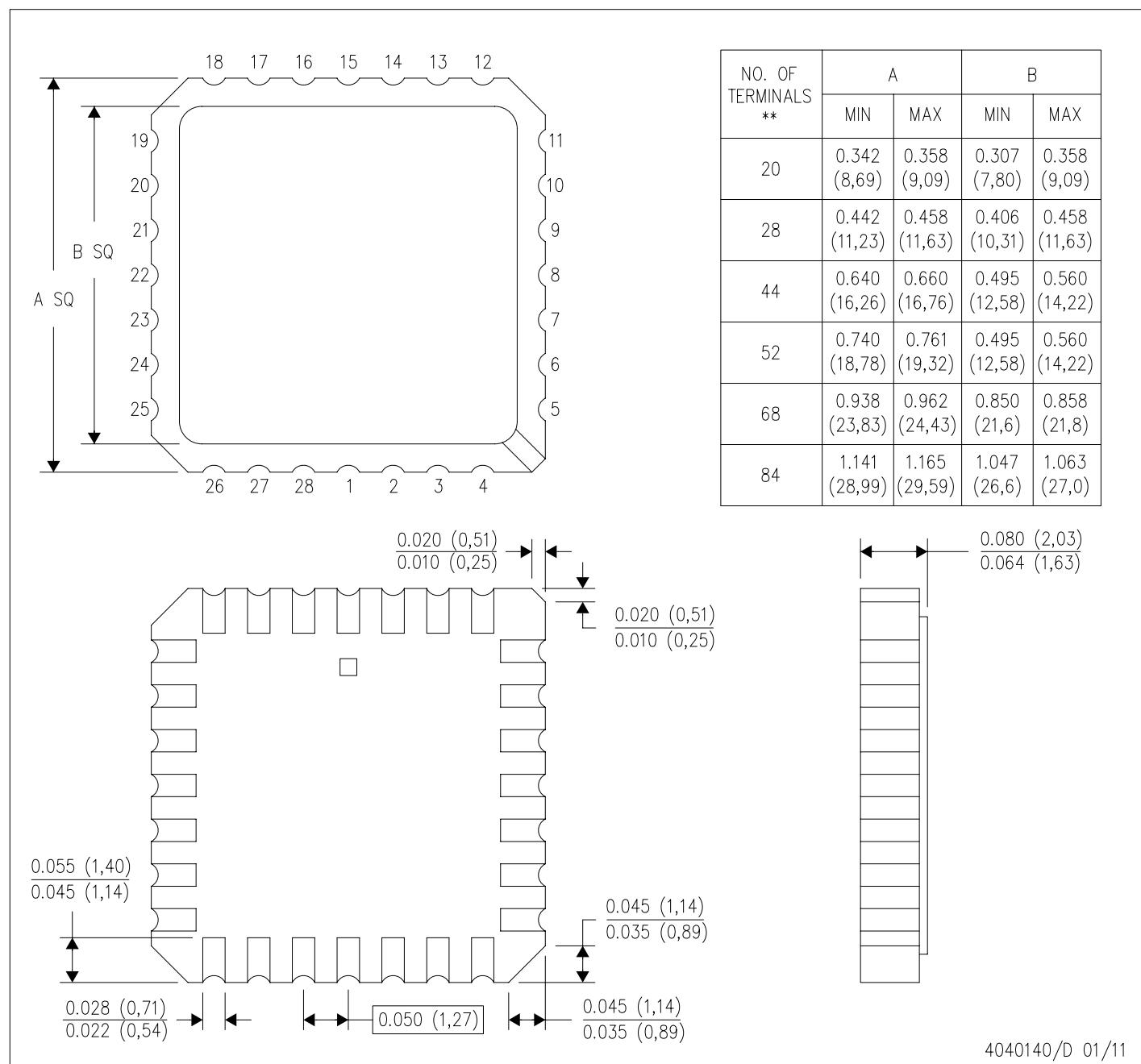
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL-STD 1835 GDFP2-F16

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES:

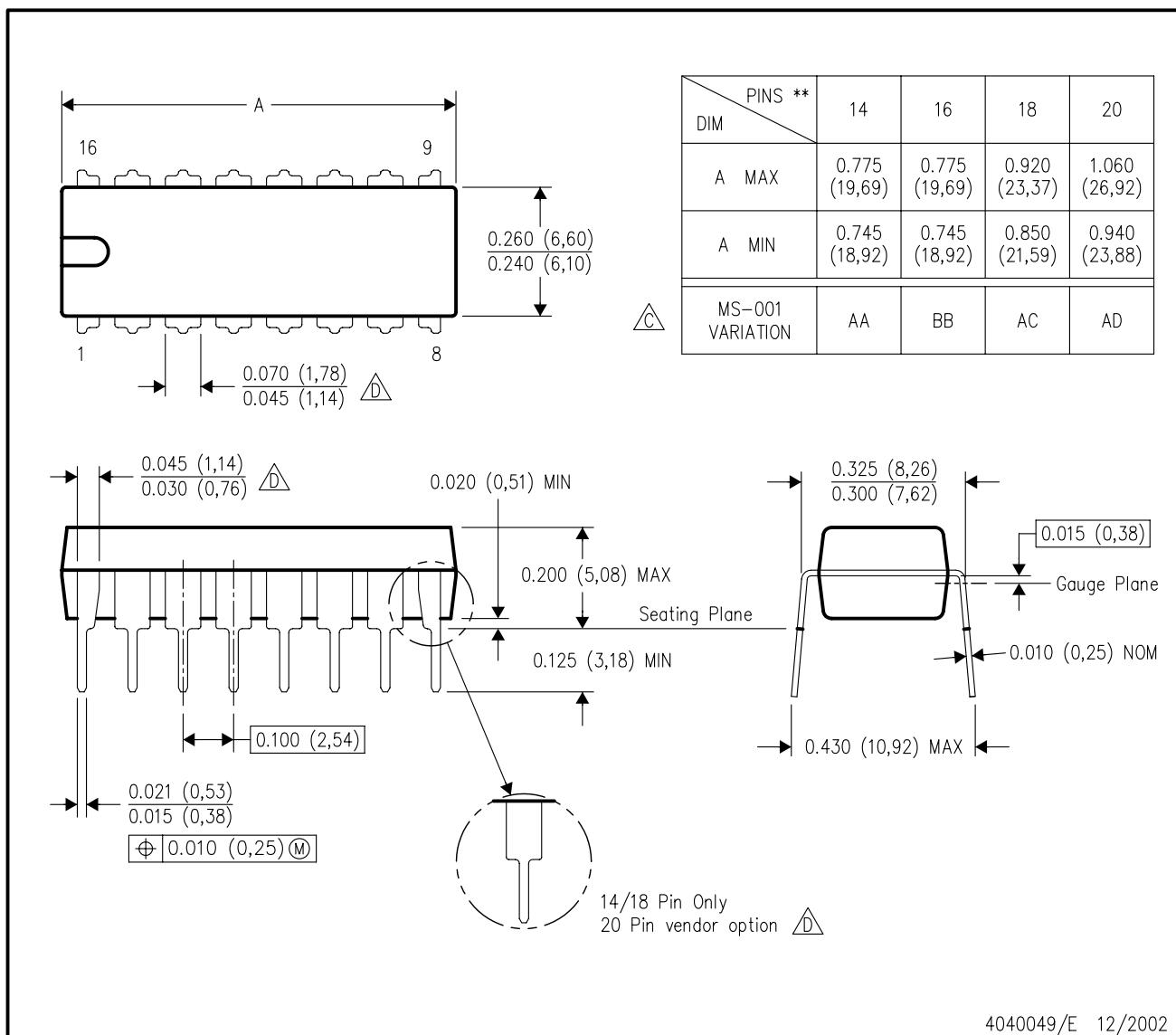
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

4040140/D 01/11

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



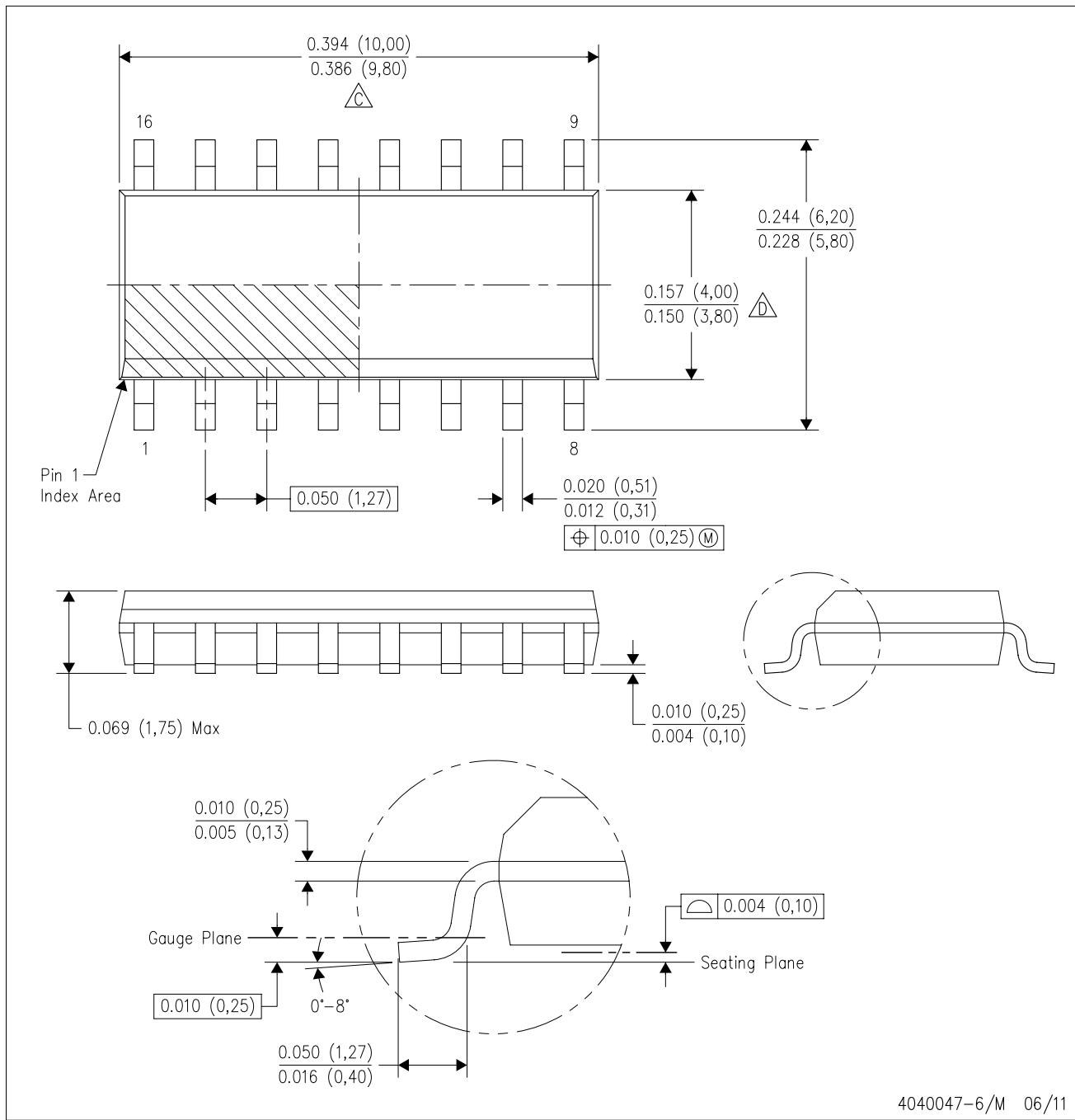
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

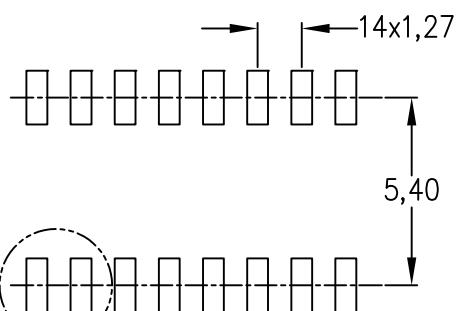
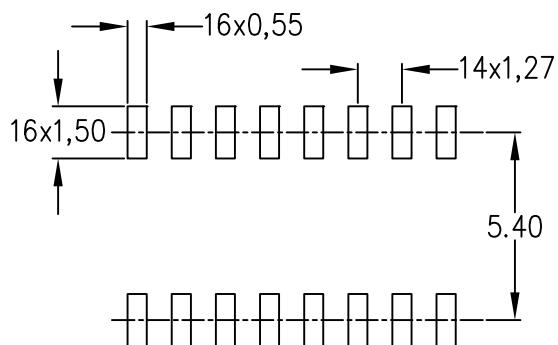
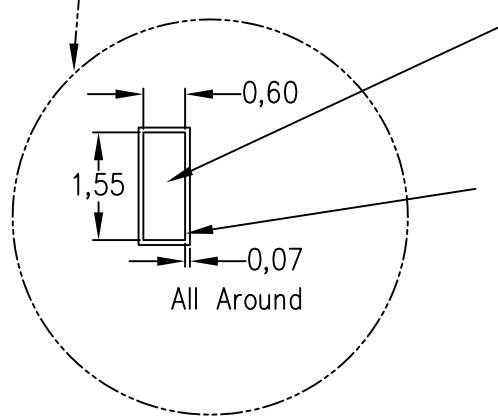
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

4211283-4/E 08/12

NOTES:

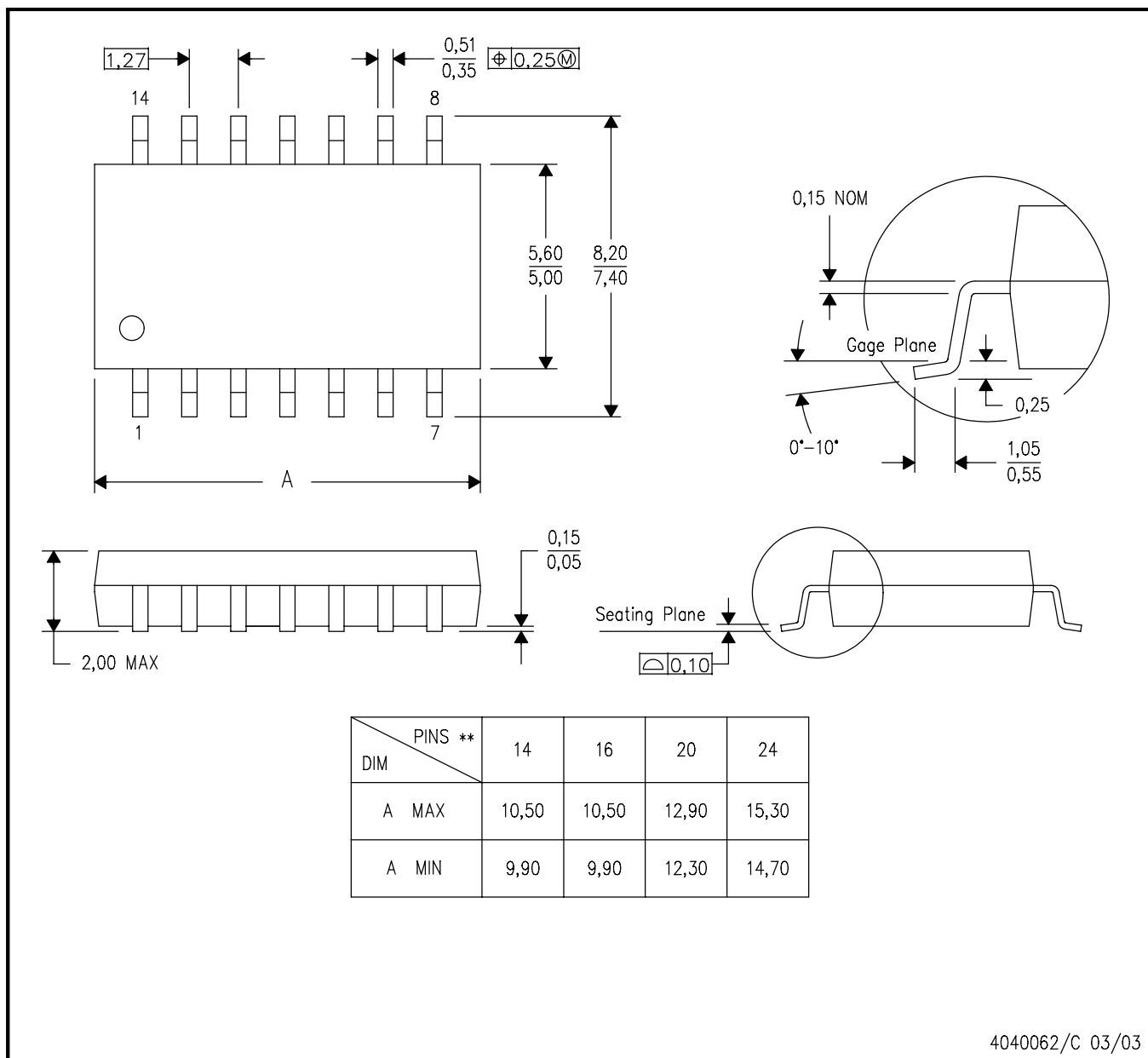
- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products	Applications
Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity
	TI E2E Community
	e2e.ti.com