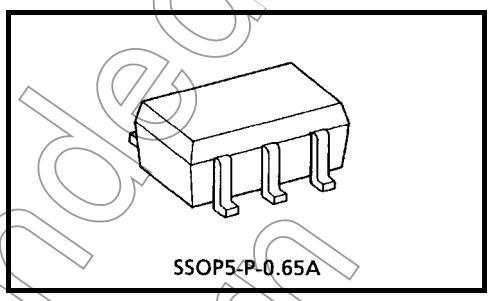
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7SBL384AFU

Single Low-Voltage Bus Switch



Weight: 0.006 g (typ.)

The TC7SBL384AFU is a low ON-resistance, high-speed CMOS 1-bit bus switch with low-voltage operation. The low ON-resistance of the switch allows connections to be made with minimal propagation delay.

The device comprises a single-bit low-impedance switch with output-enable ($\overline{OE}$) input. When $\overline{OE}$ is low, the switch is on and data can flow from port A to port B, or vice versa. When $\overline{OE}$ is high, the switch is open and a high-impedance state exists between the two ports.

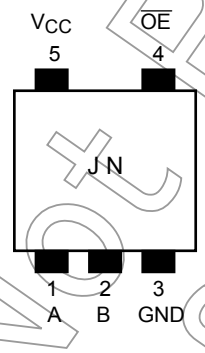
P-MOS and N-MOS channel blocks also render the device suitable for analog signal transmission.

All inputs are equipped with protection circuits to guard against static discharge.

Features

- Operating voltage: V_{CC} = 2~3.6 V
- High speed operation: t_{pd} = 0.31 ns (max) @3 V
- Low ON-resistance: R_{ON} = 5 Ω (typ.) @3 V
- ESD performance: Machine model ≥ ±200 V
  Human body model ≥ ±2000 V
- Power-down protection for inputs. ($\overline{OE}$ input only)
- Package: USV

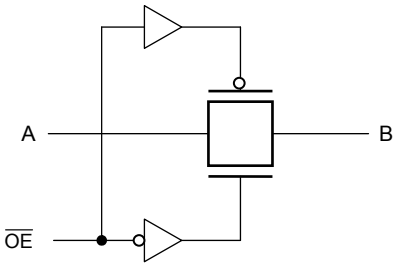
Pin Assignment (top view)



Truth Table

Input $\overline{OE}$	Function
L	A port = B port
H	Disconnect

System Diagram



Absolute Maximum Ratings (Note)

Characteristic		Symbol	Rating	Unit
Power supply range		V_{CC}	−0.5~4.6	V
Control pin input voltage		V_{IN}	−0.5~4.6	V
Switch terminal I/O voltage		V_S	−0.5~Vcc+0.5	V
Clump diode current	Control input pin	I_{IK}	−50	mA
	Switch terminal		±50	
Switch I/O current		I_S	128	mA
Power dissipation		P_D	200	mW
DC V_{CC}/GND current		I_{CC}/I_{GND}	±100	mA
Storage temperature		T_{stg}	−65~150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, may lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristic	Symbol	Rating	Unit
Power supply voltage	V_{CC}	2.0~3.6	V
Control pin input voltage	V_{IN}	0~3.6	V
Switch I/O voltage	V_S	0~Vcc	V
Operating temperature	T_{opr}	−40~85	°C
Input rise and fall time	dt/dv	0~10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.

Electrical Characteristics

DC Characteristics (Ta = –40~85°C)

Characteristic		Symbol	Test Condition	V_{CC} (V)	Min	Typ.	Max	Unit
Control pin input voltage	"H" level	V_{IH}	—	2.0~3.6	0.7 × V_{CC}	—	—	V
	"L" level	V_{IL}	—	2.0~3.6	—	—	0.3 × V_{CC}	
Control pin Input leakage current		I_{IN}	V_{IN} = 0 to 3.6 V	2.0~3.6	—	—	±1.0	μA
Power off leakage current		I_{OFF}	$\overline{OE}$ = 0 to 3.6 V	0	—	—	±1.0	μA
Off-state leakage current (switch off)		I_{SZ}	A, B = 0 to V_{CC}, $\overline{OE}$ = V_{CC}	2.0~3.6	—	—	±1.0	μA
ON resistance (Note 2)		R_{ON}	V_{IS} = 0 V, I_{IS} = 30 mA (Note 1)	3.0	—	3	7	Ω
			V_{IS} = 3.0 V, I_{IS} = 30 mA (Note 1)	3.0	—	4	9	
			V_{IS} = 2.4 V, I_{IS} = 15 mA (Note 1)	3.0	—	5	15	
			V_{IS} = 0 V, I_{IS} = 24 mA (Note 1)	2.3	—	4	10	
			V_{IS} = 2.3 V, I_{IS} = 24 mA (Note 1)	2.3	—	5	15	
			V_{IS} = 2.0 V, I_{IS} = 15 mA (Note 1)	2.3	—	6	25	
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND, I_{OUT} = 0	3.6	—	—	10	μA

Note 1: The typical values are at Ta = 25°C.

Note 2: Measured by the voltage drop between A and B pins at the indicated current through the switch. ON-resistance is determined by the lower of the voltages on the two pins (A or B).

AC Characteristics (Ta = –40~85°C)

Characteristic	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit
Propagation delay time (bus to bus)	t_{pLH}	Figure 1, Figure 2 (Note)	3.3±.0.3	—	0.31	ns
	t_{pHL}		2.5±.0.2	—	0.52	
Output enable time	t_{pZL}	Figure 1, Figure 3	3.3±.0.3	—	5	ns
	t_{pZH}		2.5±.0.2	—	7	
Output disable time	t_{pLZ}	Figure 1, Figure 3	3.3±.0.3	—	6	ns
	t_{pHZ}		2.5±.0.2	—	7	

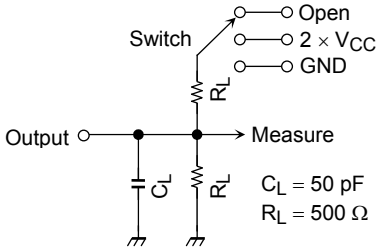
Note: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical ON-resistance of the switch and the 50 pF load capacitance when driven by an ideal voltage from the source (zero output impedance).

Capacitive Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Control pin input capacitance	C_{IN}	(Note)	3.3	3	pF
Switch terminal capacitance	$C_{I/O}$	$\overline{OE}$ = V_{CC} (Note)	3.3	17	pF

Note: This parameter is guaranteed by design.

AC Test Circuit



Parameter	Switch
t_{pLH}, t_{pHL}	Open
t_{pLZ}, t_{pZL}	2 × V_{CC}
t_{pHZ}, t_{pZH}	GND

Figure 1

AC Waveform

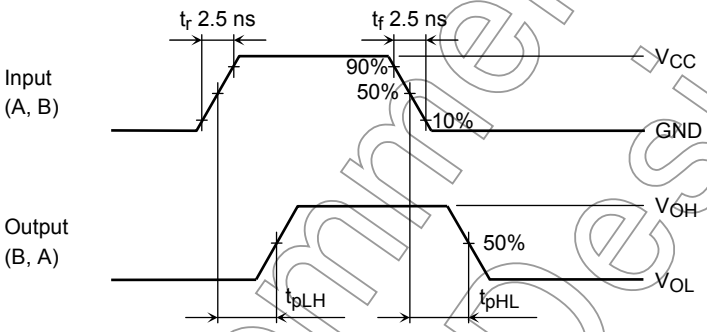


Figure 2 t_{pLH}, t_{pHL}

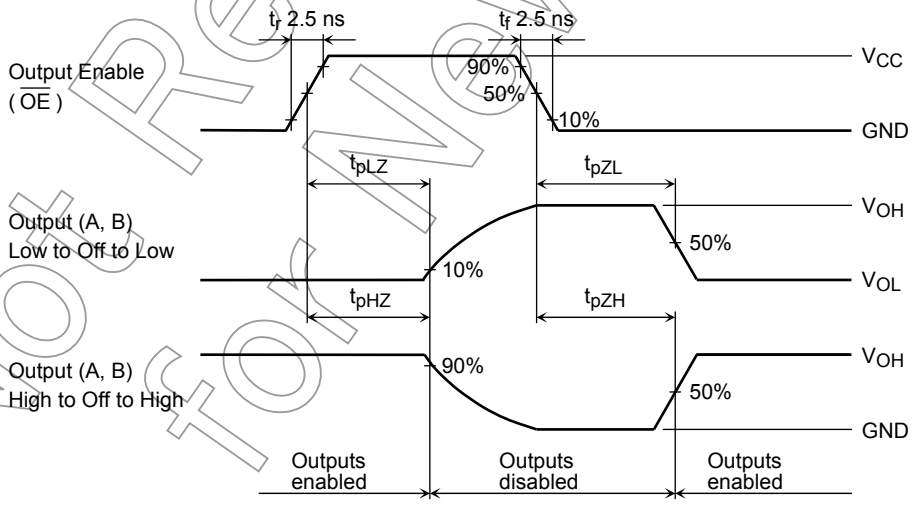
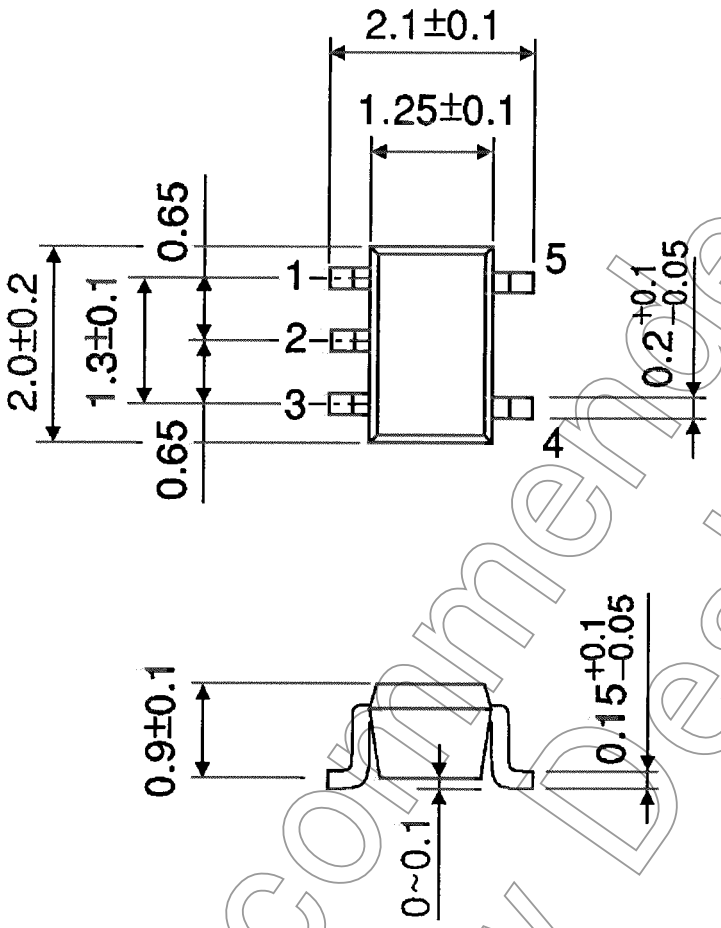


Figure 3 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

Package Dimensions

SSOP5-P-0.65A Unit : mm



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