TRIPLE PLL FIELD PROG. SPREAD SPECTRUM CLOCK SYNTHESIZER ICS291

Description

The ICS291 field programmable spread spectrum clock synthesizer generates up to six high-quality, high-frequency clock outputs including multiple reference clocks from a low-frequency crystal input. It is designed to replace crystals, crystal oscillators and stand alone spread spectrum devices in most electronic systems.

Using IDT's VersaClock™ software to configure PLLs and outputs, the ICS291 contains a One-Time Programmable (OTP) ROM for field programmability. Programming features include input/output frequencies, spread spectrum amount, eight selectable configuration registers and up to two sets of three low-skew outputs.

Each of the two output groups are powered by a separate VDDO voltage. VDDO may vary from 1.8 V to VDD.

Using Phase-Locked Loop (PLL) techniques, the device runs from a standard fundamental mode, inexpensive crystal, or clock. It can replace multiple crystals and oscillators, saving board space and cost.

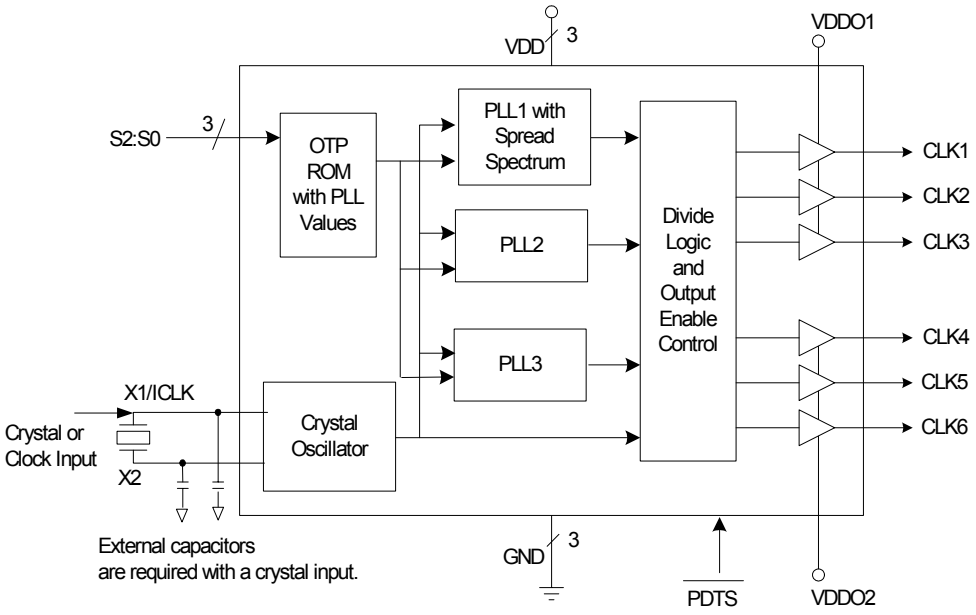
The ICS291 is also available in factory programmed custom versions for high-volume applications.

Features

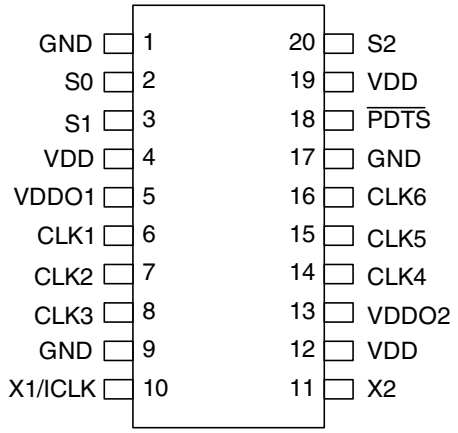
- Packaged as 20-pin TSSOP
- Eight addressable registers
- Replaces multiple crystals and oscillators
- Output frequencies up to 200 MHz at 3.3 V
- Configurable Spread Spectrum Modulation
- Input crystal frequency of 5 to 27 MHz
- Clock input frequency of 3 to 166 MHz
- Up to six reference outputs
- Separate 1.8 to 3.3 V VDDO output level controls for each bank of 3 outputs
- Up to two sets of three low-skew outputs
- Operating voltages of 3.3 V
- Controllable output drive levels
- Advanced, low-power CMOS process
- Available in Pb (lead) free packaging

NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01

Block Diagram



Pin Assignment



20 pin (173 mil) TSSOP

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	GND	Power	Connect to ground.
2	S0	Input	Select pin 0. Internal pull-up resistor.
3	S1	Input	Select pin 1. Internal pull-up resistor.
4	VDD	Power	Connect to +3.3 V.
5	VDDO1	Power	Power supply for outputs CLK1-CLK3.
6	CLK1	Output	Output clock 1. Weak internal pull-down when tri-state.
7	CLK2	Output	Output clock 2. Weak internal pull-down when tri-state.
8	CLK3	Output	Output clock 3. Weak internal pull-down when tri-state.
9	GND	Power	Connect to ground.
10	X1/ICLK	XI	Crystal input. Connect this pin to a crystal or external input clock.
11	X2	XO	Crystal Output. Connect this pin to a crystal. Float for clock input.
12	VDD	Power	Connect to +3.3 V.
13	VDDO2	Power	Power supply for outputs CLK4-CLK6.
14	CLK4	Output	Output clock 4. Weak internal pull-down when tri-state.
15	CLK5	Output	Output clock 5. Weak internal pull-down when tri-state.
16	CLK6	Output	Output clock 6. Weak internal pull-down when tri-state.
17	GND	Power	Connect to ground.
18	$\overline{\text{PDTS}}$	Input	Power-down tri-state. Powers down entire chip and tri-states clock outputs when low. Internal pull-up resistor.
19	VDD	Power	Connect to +3.3 V.
20	S2	Input	Select pin 2. Internal pull-up resistor.

External Components

The ICS291 requires a minimum number of external components for proper operation.

Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Decoupling Capacitors

As with any high-performance mixed-signal IC, the ICS291 must be isolated from system power supply noise to perform optimally.

Decoupling capacitors of 0.01µF must be connected between each VDD and the PCB ground plane. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias on the decoupling circuit.

Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal (C_L -6 pF)*2. In this equation, C_L= crystal load capacitance in pF. Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be 20 pF [(16-6) x 2 = 20].

ICS291 Configuration Capabilities

The architecture of the ICS291 allows the user to easily configure the device to a wide range of output frequencies, for a given input reference frequency.

The frequency multiplier PLL provides a high degree of precision. The M/N values (the multiplier/divide values available to generate the target VCO frequency) can be set within the range of M = 1 to 1024 and N = 1 to 32,895.

The ICS291 also provides separate output divide values, from 2 through 63, to allow the two output clock banks to support widely differing frequency values from the same PLL.

Each output frequency can be represented as:

$$OutputFreq = REFFreq \cdot \frac{M}{N}$$

Output Drive Control

The ICS291 has two output drive settings. For VDDO=VDD, low drive should be selected when outputs are less than 100 MHz. High drive should be selected when outputs are greater than 100 MHz.

For VDDO<2.8 V, high drive should be selected for all output frequencies.

(Consult the AC Electrical Characteristics for output rise and fall times for each drive option.)

IDT VersaClock Software

IDT applies years of PLL optimization experience into a user friendly software that accepts the user's target reference clock and output frequencies and generates the lowest jitter, lowest power configuration, with only a press of a button. The user does not need to have prior PLL experience or determine the optimal VCO frequency to support multiple output frequencies.

VersaClock software quickly evaluates accessible VCO frequencies with available output divide values and provides an easy to understand, bar code rating for the target output frequencies. The user may evaluate output accuracy, performance trade-off scenarios in seconds.

Spread Spectrum Modulation

The ICS291 utilizes frequency modulation (FM) to distribute energy over a range of frequencies. By modulating the output clock frequencies, the device effectively lowers energy across a broader range of frequencies; thus, lowering a system's electromagnetic interference (EMI). The modulation rate is the time from transitioning from a minimum frequency to a maximum frequency and then back to the minimum.

Spread Spectrum Modulation can be applied as either “center spread” or “down spread”. During center spread modulation, the deviation from the target frequency is equal in the positive and negative directions. The effective average frequency is equal to the target frequency. In applications where the clock is driving a component with a maximum frequency rating, down spread should be applied. In this case, the maximum frequency, including modulation, is the target frequency. The effective average frequency is less than the target frequency.

The ICS291 operates in both center spread and down spread modes. For center spread, the frequency can be modulated between ±0.125% to ±2.0%. For down spread, the frequency can be modulated between -0.25% to -4.0%.

Both output frequency banks will utilize identical spread spectrum percentage deviations and modulation rates, if a common VCO frequency can be identified.

Spread Spectrum Modulation Rate

The spread spectrum modulation frequency applied to the output clock frequency may occur at a variety of rates. For applications requiring the driving of “down-circuit” PLLs, Zero Delay Buffers, or those adhering to PCI standards, the spread spectrum modulation rate should be set to 30-33 kHz. For other applications, a 120 kHz modulation option is available.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS291. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Parameter	Condition	Min.	Typ.	Max.	Units
Supply Voltage, VDD	Referenced to GND			7	V
Inputs	Referenced to GND	-0.5		VDD+0.5	V
Clock Outputs	Referenced to GND	-0.5		VDD+0.5	V
Storage Temperature		-65		150	°C
Soldering Temperature	Max 10 seconds			260	°C
Junction Temperature				125	°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (ICS291GP)	0		+70	°C
Ambient Operating Temperature (ICS291GIP)	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.135	+3.3	+3.465	V
Power Supply Ramp Time			4	ms

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.135		3.465	V
VDDO Voltage		VDDO1 and VDDO2	1.80		VDD	V
Operating Supply Current	IDD	Config. Dependent - See VersaClock™ Estimates				mA
		Six 33.3333 MHz outs, VDD=VDDO=3.3 V; $\overline{PDTS}$ = 1, no load, Note 1		25		mA
		$\overline{PDTS}$ = 0, no load		500		µA
Input High Voltage	V_{IH}	S2:S0	VDD/2+1			V
Input Low Voltage	V_{IL}	S2:S0			0.4	V
Input High Voltage, $\overline{PDTS}$	V_{IH}		VDD-0.5			V
Input Low Voltage, $\overline{PDTS}$	V_{IL}				0.4	V
Input High Voltage	V_{IH}	ICLK	VDD/2+1			V
Input Low Voltage	V_{IL}	ICLK			VDD/2-1	V
Output High Voltage (CMOS High)	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Output High Voltage	V_{OH}	I_{OH} = -8 mA (Low Drive); I_{OH} = -12 mA (High Drive)	2.4 VDDO-0.4			V
Output Low Voltage	V_{OL}	I_{OL} = 8 mA (Low Drive); I_{OL} = 12 mA (High Drive)			0.4	V
Short Circuit Current	I_{OS}	Low Drive		±40		mA
		High Drive		±70		
Nom. Output Impedance	Z_O			20		Ω
Internal Pull-up Resistor	R_{PUS}	S2:S0, $\overline{PDTS}$		190		kΩ
Internal Pull-down Resistor	R_{PD}	CLK outputs		120		kΩ
Input Capacitance	C_{IN}	Inputs		4		pF

Note 1: Example with 25 MHz crystal input with six outputs of 33.$\overline{3}$ MHz, no load, and VDD = 3.3 V.

AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	F_{IN}	Fundamental crystal	5		27	MHz
		Clock input	3		166	MHz
Output Frequency		VDDO=VDD	0.314		200	MHz
		1.8 V<VDDO<2.8 V	0.314		150	MHz
Output Rise/Fall Time	t_{OF}	80% to 20%, high drive, Note 1		1.0		ns
Output Rise/Fall Time	t_{OF}	80% to 20%, low drive, Note 1		2.0		ns
Output Rise/Fall Time	t_{OF}	80% to 20%, high drive, 1.8 V≤VDDO≤2.8 Note 2		2.0		ns
Duty Cycle		Note 2	40	49-51	60	%
Output Frequency Synthesis Error		Configuration Dependent		TBD		ppm
Power-up time		PLL lock-time from power-up		4	10	ms
		$\overline{PDTS}$ goes high until stable CLK output, Spread Spectrum Off		0.6	2	ms
		$\overline{PDTS}$ goes high until stable CLK output, Spread Spectrum On		4	7	ms
One Sigma Clock Period Jitter		Configuration Dependent		50		ps
Maximum Absolute Jitter	t_{ja}	Deviation from Mean. Configuration Dependent		±200		ps
Pin-to-Pin Skew		Low Skew Outputs	-250		250	ps

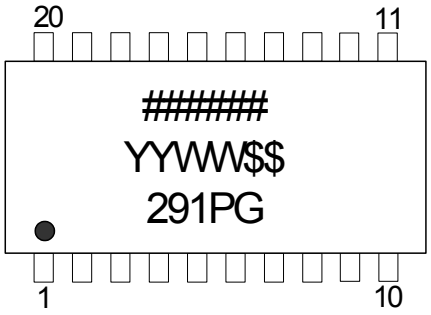
Note 1: Measured with 15 pF load.

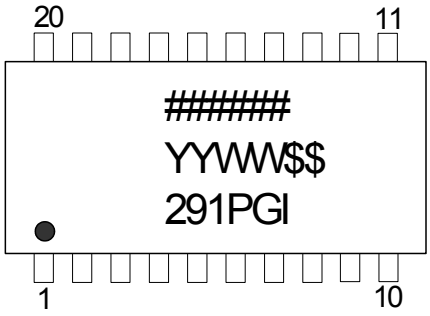
Note 2: Duty Cycle is configuration dependent. Most configurations are min 45% / max 55%.

Thermal Characteristics

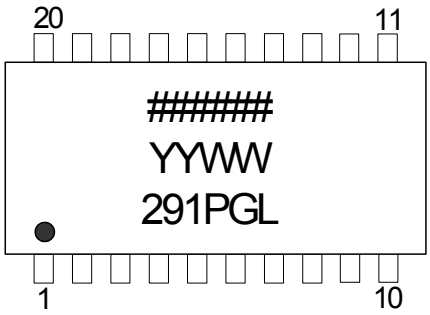
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		93		°C/W
	θ_{JA}	1 m/s air flow		78		°C/W
	θ_{JA}	3 m/s air flow		65		°C/W
Thermal Resistance Junction to Case	θ_{JC}			20		°C/W

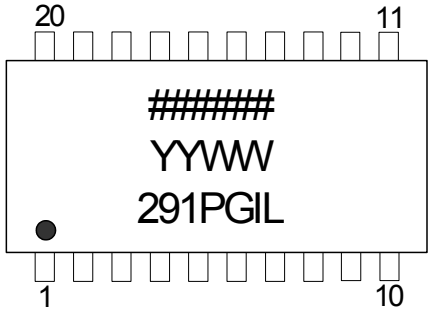
Marking Diagrams





Marking Diagrams (Pb free)



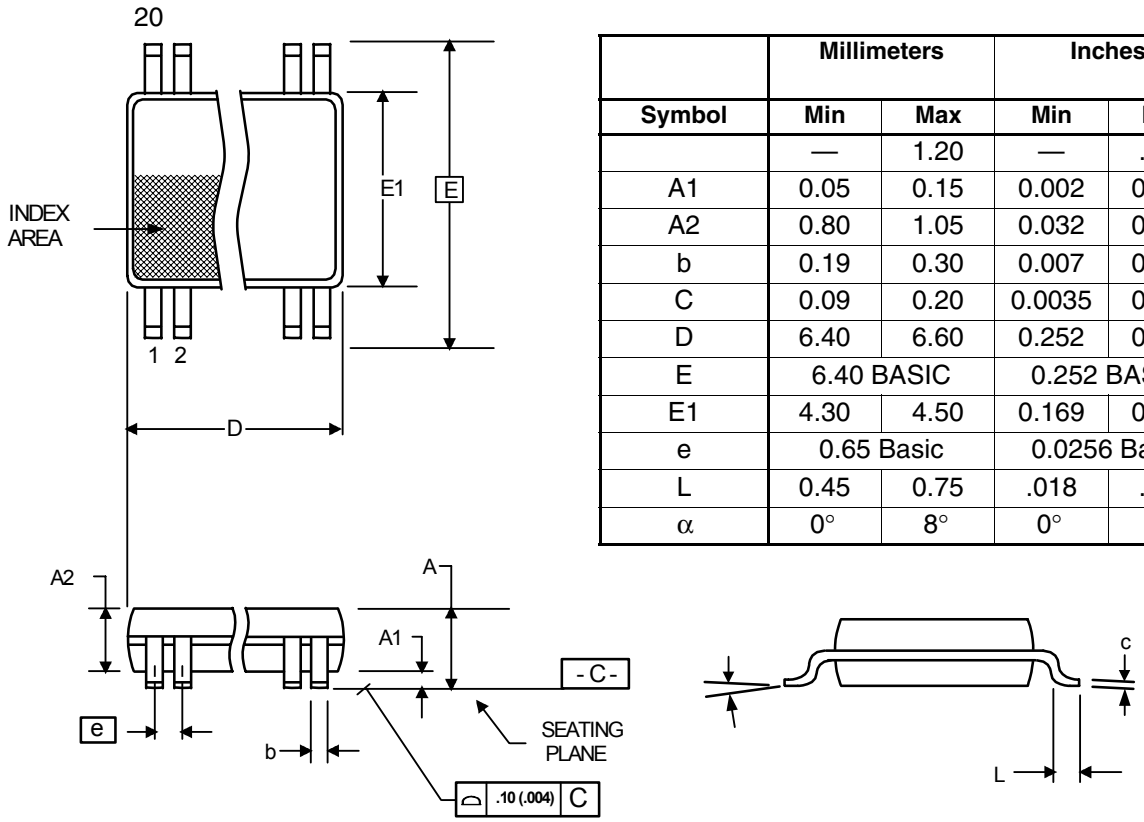


Notes:

1. ###### is the lot number.
2. YYWW is the last two digits of the year and week that the part was assembled.
3. “I” denotes industrial temperature range (if applicable).
4. “L” denotes Pb (lead) free package.
5. Bottom marking: country of origin.

Package Outline and Package Dimensions (20-pin TSSOP, 173 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
	—	1.20	—	.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	6.40	6.60	0.252	0.260
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	.018	.030
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
291PG*	See page 7	Tubes	20-pin TSSOP	0 to +70° C
291PGI*		Tubes	20-pin TSSOP	-40 to +85° C
291PGLF		Tubes	20-pin TSSOP	0 to +70° C
291PGILF		Tubes	20-pin TSSOP	-40 to +85° C
291G-XX*	291G-XX	Tubes	20-pin TSSOP	0 to +70° C
291GI-XX*	291GIXX	Tubes	20-pin TSSOP	-40 to +85° C
291G-XXLF	291GXXL	Tubes	20-pin TSSOP	0 to +70° C
291GI-XXLF	291GIXXL	Tubes	20-pin TSSOP	-40 to +85° C
291G-XXT*	291G-XX	Tape and Reel	20-pin TSSOP	0 to +70° C
291GI-XXT*	291GIXX	Tape and Reel	20-pin TSSOP	-40 to +85° C
291G-XXLFT	291GXXL	Tape and Reel	20-pin TSSOP	0 to +70° C
291GI-XXLFT	291GIXXL	Tape and Reel	20-pin TSSOP	-40 to +85° C

***NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01**

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

The 291G-XX, 291G-XXLF, 291GI-XX, and 291GI-XXLF are factory programmed versions of the 291PG, 291PGLF, 291PGI, and 291PGILF. A unique "-XX" suffix is assigned by the factory for each custom configuration, and a separate data sheet is kept on file. For more information on custom part numbers programmed at the factory, please contact your local IDT sales and marketing representative.

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