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PCI0640B

PCI to IDE Chip

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1 Interface Specifications

1.1 PCI Mode Pin Descriptions

The following is an alphabetical listing of PCI mode signals and their pin assignments. Please refer to the PCI mode pinout diagram for the locations of the pins.

Signal	Pin	I/O
AD[31..0]	7-14, 17-20, 23-26, 28-35, 42-49	IO
Function		
Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts. The address phase is the clock cycle in which FRAME # is asserted. During the address phase AD[31..0] contain a physical address (32 bits). For I/O, this is a byte address; for configuration and memory it is a DWORD address. During data phases AD[7..0] contain the least significant byte (lsb) and AD[31..24] contain the most significant byte (msb). Write data are stable and valid when IRDY# is asserted and read data are stable and valid when TRDY# is asserted. Data are transferred during those clocks where both IRDY# and TRDY# are asserted.		

Signal	Pin	I/O
C/BE[3..0]#	3-6	I
Function		
Byte Enable bits 0 through 3 form the host CPU address bus. These inputs are active low and specify which bytes will be valid for host read/write data transfers.		

Signal	Pin	I/O
DCS0#	55	IO
Function		
Disk Chip Select 0 is normally active low output and is used to select the first IDE port command block registers in the drive(s). This signal connects directly to the ATA bus connector. DCS0# is used as an input at reset to specify PCI0640B operating modes (see Jumper Settings on page 1-20). DCS0# is sampled as an input on the rising edge of RESET#. This pin is internally pulled up.		

Signal	Pin	I/O
DCS1#	56	IO
Function		
Disk Chip Select 1 is normally active low output which is used to select the first IDE port auxiliary registers in the drive(s). This signal connects directly to the ATA bus connector. DCS1# is used as an input at reset to specify PCI0640B operating modes (see Jumper Settings on page 1-20). DCS1# is sampled as an input on the rising edge of RESET#. This pin is internally pulled up.		

Signal	Pin	I/O
DCS2#	80	O
Function		
Disk Chip Select 2. Used to select second IDE port command registers in the drive.		

Signal	Pin	I/O
DCS3#	79	O
Function		
Disk Chip Select 3. Used to select second IDE port auxiliary register.		

Signal	Pin	I/O
DEVSEL#	93	O
Function		
Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, it indicates to a master whether any device on the bus has been selected.		

Signal	Pin	I/O
DIO16#	61	I
Function		
Disk I/O 16 is an active low input which indicates that the disk drive is ready to perform a 16-bit data transfer. The signal connects directly to the ATA connector and will typically be driven active by the drive during PCI0640B transfers to the drive's 1F0h data port. Note that an external 1K-ohm pull-up resistor and a 47pF capacitor pull-down is recommended for this signal.		

Signal	Pin	I/O
DIOR#	57 (primary port), 77 (secondary port)	O
Function		
Disk IO Read is an active low output which enables data to be read from the drive. The duration and repetition rate of DIOR# cycles is determined by PCI0640B programming. DIOR# is driven high when inactive.		

Signal	Pin	I/O
DIOW#	58 (primary port), 78 (secondary port)	O
Function		
Disk I/O Write is an active low output that enables data to be written to the drive. The duration and repetition rate of DIOW# cycles is determined by PCI0640B programming. DIOW# is driven high when inactive.		

Signal	Pin	I/O
DIRQ1	75	I
Function		
Disk Interrupt is an input to the PCI0640B used to generate the IRQ14 output. DIRQ1 is asserted low then high by the drive at the beginning of a block transfer. This input should have a 4.7K-ohm pull-up and a 470pF capacitor pull-down connected to it.		

Signal	Pin	I/O
DIRQ2	86	I
Function		
Disk interrupt input for secondary IDE port is used to generate the IRQ15 output. DIRQ2 is asserted low then high by the drive at the beginning of a block transfer. This input should have a 4.7K-ohm pull-up and a 470pF capacitor pull-down.		

Signal	Pin	I/O
DRST#	59	O
Function		
Disk ReSeT is an active low output which signals the IDE drive(s) to initialize its control registers. DRST# is a buffered version of the RESET# input and connects directly to the ATA connector.		

Signal	Pin	I/O
DSA[2..0]	70, 69, 68	IO
Function		
Disk Address bits 0 through 2 are normally outputs to the ATA connector for register selection in the drive(s). These signals are decoded from the A2 and C/BE[3..0] inputs. DSA[2..0] are also sampled as inputs on the falling edge of RESET#. All of these pins have internal pull-up resistors. 2.2k resistors are recommended where pull-downs are required. (See “Jumper Settings” on page 1-20.)		

Signal	Pin	I/O
DSD[15..0]	36-39, 50-53, 62-65, 71-74	IO
Function		
Disk Data bits 0 through 15 are the 16-bit bi-directional data bus which connects to the IDE drive(s). DSD[7..0] define the lowest data byte while DSD[15..8] define the most significant data byte. The DSD bus is normally in a high-impedance state and is driven by the PCI0640B only during the DIOW# command pulse.		

Signal	Pin	I/O
ENDSKCHG#	85	I
Function		
ENDSKCHG# enables or disables reads to port 3F7. Use 2.2K-ohm pull-down resistors to enable. Port 3F7 is disabled by default.		

Signal	Pin	I/O
ENIDE	21	I
Function		
ENable IDE is an active high input that controls the PCI0640B's default disk operation mode following reset. When set low, the PCI0640B's IDE cycles are disabled following reset. This mode allows software to scan for system hardware and enable the PCI0640B via the PCMD register (index 4). When left floating or pulled high, the PCI0640B is enabled and cannot be disabled via software.		

Signal	Pin	I/O
FRAME #	98	I
Function		
Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAME # is asserted to indicate a bus transaction is beginning. While FRAME # is asserted, data transfers continue. When FRAME # is deasserted, the transaction is in the final data phase.		

Signal	Pin	I/O
IDSEL#	100	I
Function		
Initialization Device Select is used as a chip select during configuration read and write transactions.		

Signal	Pin	I/O
INTA#	84	O/D
Function		
Interrupt A is used to request an interrupt in PCI IDE Native Mode. INTA# is tri-stated when both IDE ports are in Legacy Mode.		

Signal	Pin	I/O
IOCHRDY	76	I
Function		
I/O Channel Ready is an active high input that indicates that the IDE disk drive has completed the current command cycle. A 1K-ohm pull-up resistor is recommended.		

Signal	Pin	I/O
IRDY#	99	I
Function		
Initiator Ready indicates the initializing agent's (bus master's) ability to complete the current data phase of the transaction. This signal is used with TRDY#. A data phase is completed on any clock when both IRDY# and TRDY# are sampled asserted. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.		

Signal	Pin	I/O
IRQ14	22	O
Function		
IRQ14 is used to request an interrupt in PCI IDE Legacy Mode. (For PC-AT compatibles.) IRQ14 is tri-stated when IDE port 0 is in Native Mode.		

Signal	Pin	I/O
IRQ15	83	O
Function		
IRQ15 is used to request an interrupt for secondary IDE port in PCI IDE Legacy Mode. (PC-AT compatible.) IRQ15 is tri-stated when IDE port 1 is in Native Mode.		

Signal	Pin	I/O
PAR	96	I
Function		
PAR is even parity across AD[31..0] and C/BE[3..0]#. Parity generation is required by all PCI agents. PAR is stable and valid one clock after the address phase. For data phases PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. (PAR has the same timing as AD[31..0] but delayed by one clock.)		

Signal	Pin	I/O
PCICLK	89	I
Function		
Clock Signal provides timing for all transactions on PCI and is an input to every PCI device. All other PCI signals, except RESET# and IRQ, are sampled on the rising edge of PCICLK, and all other timing parameters are defined with respect to this edge.		

Signal	Pin	I/O
PCIMODE	2	I
Function		
PCIMODE is set to high when chip is used in PCI bus. When chip is used in VL bus, PCIMODE is set to low.		

Signal	Pin	I/O
PERR#	95	IO
Function		
Error may be pulsed active by an agent that detects a parity error. PERR# can be used by any agent to signal data corruptions. However, on detection of a PERR# pulse, the central resource may generate a nonmaskable interrupt to the host CPU, which often implies that the system will be unable to continue operation once error processing is complete.		

Signal	Pin	I/O
RESET#	1	I
Function		
RESET# is an active low input that is used to set the internal registers of the PCI0640B to their initial state. RESET# is typically the system power-on reset signal as distributed on the PCI bus.		

Signal	Pin	I/O
STOP#	97	IO
Function		
STOP# indicates the current target is requesting the master to stop the current transaction.		

Signal	Pin	I/O
TRDY#	92	O
Function		
Target Ready indicates the target agent's ability to complete the current data phase of the transaction. TRDY# is used with IRDY#. A data phase is completed on any clock when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that valid data is present on AD(31..0). During a write, it indicates the target is prepared to accept data.		

Signal	Pin	I/O
VDD	16, 41, 67, 91	I
Function		
Positive power supply input.		

Signal	Pin	I/O
VSS	15, 27, 40, 54, 66, 90	I
Function		
Ground reference power supply input.		

1.2 VL Mode Pin Descriptions

The following is an alphabetical listing of VL mode signals and their pin assignments. Please refer to the VL mode pinout diagram for the locations of the pins.

Signal	Pin	I/O
ADS#	98	I
Function		
ADdress Strobe is an active low input that indicates that there is a valid address and command on the bus. ADS# connects directly to the host CPU ADS# signal.		

Signal	Pin	I/O
BE[3..0]	3-6	I
Function		
Byte Enable bits 0 through 3 (together with the HA[15..2] signals) form the host CPU address bus. These inputs are active low and specify which bytes will be valid for host read/write data transfers.		

Signal	Pin	I/O
CS0#	55	IO
Function		
Chip Select 0 is normally an active low output that is used to select the command block regiisters in the drive(s). This signal connects directly to the ATA bus connector. DCS0# is used as an input at reset to specify PCI0640B operating modes. DCS0# is sampled as an input on the falling edge of RESET#.		

Signal	Pin	I/O
CS1#	56	IO
Function		
Chip Select 1 is normally an active low output that is used to select the control block registers in the drive(s). This signal connects directly to the ATA bus connector. As an input DCS1# is used to specify PCI0640B operating modes. DCS1# is sampled as an input on the falling edge of RESET#.		

Signal	Pin	I/O
DC#	96	I
Function		
Data or Control is a low input that is used to distinguish between I/O and interrupt or halt cycles.		

Signal	Pin	I/O
DCHRDY	76	I
Function		
Disk ReaDY is an active high input that indicates that the IDE disk drive has completed the current command cycle. DCHRDY is sampled at the rising edge of VLCLK at the programmed end of the command cycle. If DCHRDY is high, the command is terminated. If DCHRDY is sampled low, the command cycle is extended. DCHRDY will then be sampled with every positive VLCLK edge until it is tested high. Once sampled high, the command will end normally. Note that an external 1K-ohm pull-up resistor should be connected to this pin for normal operation.		

Signal	Pin	I/O
DIO16#	61	I
Function		
Disk I/O 16 is an active low input that indicates that the disk drive is ready to perform a 16-bit data transfer. The signal connects directly to the ATA connector and will typically be driven active by the drive during PCI0640B transfers to the drive's 1F0h data port. Note that an external 1K-ohm pull-up resistor and a 47pF pull-down capacitor are recommended for this signal.		

Signal	Pin	I/O
DIOR#	57	O
Function		
Disk I/O Read is an active low output that enables data to be read from the drive. The duration and repetition rate of DIOR# cycles is determined by PCI0640B programming. DIOR# is driven high when inactive.		

Signal	Pin	I/O
DIOW#	58	O
Function		
Disk I/O Write is an active low output that enables data to be written to the drive. The duration and repetition rate of DIOW# cycles is determined by PCI0640B programming. DIOW# is driven high when inactive.		

Signal	Pin	I/O
DIRQ	75	I
Function		
Disk Interrupt is an input to the PCI0640B used to generate the IRQ14 output. DIRQ is asserted low then high by the drive at the beginning of a data block transfer. This input should have a 4.7K-ohm pull-up connected to it.		

Signal	Pin	I/O
DRST#	59	O
Function		
Disk ReSeT is an active low output that signals the IDE drive(s) to initialize its control registers. DRST# is an inverted, buffered version of the RESET input and connects directly to the ATA connector.		

Signal	Pin	I/O
DSA[2..0]	70, 69, 68	IO
Function		
Disk Address, bits 0 through 2, are normally outputs to the ATA connector for register selection in the drive(s). These signals are decoded from the A2 and BE[3..0] inputs. DSA[2..0] are also sampled as inputs at reset to specify the least significant bits of the device ID number. These signals are recommended to have 10K-ohm pull-up or pull-down resistors. DSA[2..0] are sampled as inputs on the rising edge of RESET#.		

Signal	Pin	I/O
DSD[15..0]	36-74	IO
Function		
Disk Data, bits 0 through 15, are the 16-bit bi-directional data bus that connects to the IDE drive(s). DSD[7..0] define the lowest data byte while DSD[15..8] define the most significant data byte. The DSD bus is normally in a high-impedance state and is driven by the PCI0640B only during the DIOW# command pulse.		

Signal	Pin	I/O
ENIDE	21	I
Function		
In VL mode, ENable IDE enables the PCI0640B chip when set HIGH and disables the chip when set LOW.		

Signal	Pin	I/O
HA[15..2]	77-98	I
Function		
Host Address bits 2 thorugh 15 (together with the BE[3..0]# signals) form the host CPU address bus.		

Signal	Pin	I/O
HD[31..0]	7-20, 23-26, 28-35, 42-49	IO
Function		
Host Data is the 32-bit bi-directional data bus that connects to the host CPU. HD[7..0] define the lowest data byte, while HD[31..24] define the most significant data byte. The active byte(s) on a CPU transfer are specified by the BE[3..0]# signals. The HD bus is normally in a high-impedance stat and is driven only during T2 states of PCI0640B read cycles.		

Signal	Pin	I/O
IRQ	22	O
Function		
Interrupt ReQest is an tri-state output normally connected to IRQ14 of the ISA bus. When PCI0640B is enabled, the IRQ14 output will track the DIRQ input. Otherwise IRQ is in a high-impedance state.		

Signal	Pin	I/O
LDEV#	93	O
Function		
Local DEVice is an active low output that indicates that the current host CPU address is a valid PCI0640B address. LDEV# is normally in a high-impedance state and is asynchronously decoded from the HA[15..2], MIO# and DC# signals. LDEV# typically connects to the system “chipset” logic. Note that LDEV# may glitch during address transitions and should be sampled appropriately by the chipset.		

Signal	Pin	I/O
LRDY0#	92	O
Function		
Local ReaDY 0 is an active low output that indicates that the current host CPU transfer is complete. LRDY# is typically connected to either the CPU directly or the PC system “chipset” as determined by the operation of the chipset. LRDY0# is normally in a high-impedance state and functions in an “open collector” style. As a PCI0640B cycle is completed, LRDY0# will first be enabled driving high and then immediately pulled low. It will remain active for 1 t-state, then drive high and finally be disabled to end the sequence.		

Signal	Pin	I/O
MIO#	97	I
Function		
Memory or I/O is an input that distinguishes between memory and I/O cycles.		

Signal	Pin	I/O
PCIMODE	2	I
Function		
PCIMODE distinguishes between PCI mode and VL mode: HIGH for PCI mode and LOW for VL mode.		

Signal	Pin	I/O
RDY#	99	I
Function		
CPU ReaDY is an active low signal that indicates the end of the current host CPU transfer. RDY# connects directly to the host CPU's READY# input. The PCI0640B tracks this signal to ensure that it remains in synchronization with the CPU under all conditions.		

Signal	Pin	I/O
RESET#	1	I
Function		
CPU ReSeT is an active low input.		

Signal	Pin	I/O
VDD	16, 41, 67, 91	I
Function		
Positive power supply input.		

Signal	Pin	I/O
VLCLK	89	I
Function		
CLocK is the host CPU clock signal. It connects directly to the VL bus clock input.		

Signal	Pin	I/O
VSS	15, 27, 40, 54, 66, 90	I
Function		
Ground reference power supply input.		

Signal	Pin	I/O
WR#	100	I
Function		
Write or Read is an input that is used to distinguish between write and read cycles.		

Signal	Pin	I/O
	60	
Function		
Not used.		

1.3 I/O Registers

1.3.1 Configuration Registers

Name	Function	Index
VID	Vendor ID (1095h) (RO)	0-1

Name	Function	Index
DID	Device ID (0640h) (RO)	2-3

Name	Function	Index
PCMD	Command Register (RW)	4-5
Bits		
15-9	reserved	
8-7	always 0	
6	0 disable parity error response 1 enable parity error response	
5-1	always 0	
0	1 IDE enabled 0 IDE disabled	

Name	Function	Index
PSTTS	Status Register (RW)	6-7
Bits		
15	detected parity error	
14	always 0	
13	always 0	
12	always 0	
11	always 0	
10-9	DEVSEL timing (RO) 00 fast 01 medium 10 slow	
8-0	reserved	

Name	Function	Index
REVID	Revision ID (RO)	8

Name	Function	Index
PROGIF	Programming interface = 00h (RO) when DSA1 is pulled down at reset = 0Ah (RW) when DSA1 is not pulled down at reset. Bits 0-3 are used to toggle between Legacy and Native Modes.	9

Name	Function	Index
SUBCL	Sub-class = 01h IDE controller (RO)	Ah

Name	Function	Index
BASCL	Base class = 01h Mass storage controller (RO)	Bh

Name	Function	Index
BaseA0	Base address register 0 (R/W)	10-13h

Name	Function	Index
BaseA1	Base address register 1 (R/W)	14-17h

Name	Function	Index
BaseA2	Base address register 2 (R/W)	18-1Bh

Name	Function	Index
BaseA3	Base address register 3 (R/W)	1C-1Fh

Name	Function	Index
INTLINE	Interrupt Line (R/W) = 14 (0Eh)	3Ch

Name	Function	Index
INPINE	Interrupt Pin (RO) = 1	3Dh

1.3.2 Common Registers

Name	Function	Index
CFR	Configuration (RO)	50h
Bits		
7	DSA0 Jumper 0—Disable ID write 1—Enable ID write	
6	DSA1 Jumper 0—Disable Base address register; R=0 1—Enable Base address register R/W	
5	VESA configuration port selection 0—178h, 17Ch 1—078h, 07Ch	
4-3	Device ID selection 00—60h 01—61h 10—62h 11—63h	
2	IDE drive 0/1 interrupt status Read CFR will clear this bit 0—no interrupt pending 1—interrupt pending	
1-0	Device revision = 02	

Name	Function	Index
CNTRL	Control Register (RW)	51h
Bits		
7	Drive 1 read ahead 0—enable 1—disable (default)	
6	Drive 0 read ahead 0—enable 1—disable	
5	Host write FIFO/reg longer data hold time 0—enable (FIFO data valid until rising edge of TRDY#) 1—disable (FIFO data valid until falling edge of TRDY#)	
4	PCI parity check 0—enable 1—disable	
3	2nd port 0—disable (default) 1—enable	
2	Devsel timing 0—medium 1—fast	
1	Host write timing to FIFO 0—slow timing (5 clocks if Bit 5 = 0; 4 clocks if Bit 5 = 1) 1—fast timing (4 clocks if Bit 5 = 0; 3 clocks if Bit 5 = 1)	
0	Host read timing from FIFO 0—slow timing (5 clocks) 1—fast timing (3 clocks)	

Name	Function	Index
CMDTIM	IDE Command Block Timing Register (RW)	52h
Bits		
7-4	IOR/W active count	
3-0	Command Recovery count	

Name	Function	Index
ARTTIM0	Drive 0 Address Setup Register (RW)	53h
Bits		
7-6	Address setup count 00—4 clks 01—2 clks 10—3 clks 11—5 clks	
5-0	reserved	

Name	Function	Index
DRWTIM0	Drive 0 Data Read/Write Timing Register (RW)	54h
Bits		
7-4	active count	
3-0	recovery count	

Name	Function	Index
ARTTIM1	Drive 1 Address Setup Register (RW)	55h
Bits		
7-6	Address setup count 00—4 clks 01—2 clks 10—3 clks 11—5 clks	
Bit 5-0	reserved	

Name	Function	Index
DRWTIM1	Drive 1 Data Read/Write Timing Register (RW)	56h
Bits		
7-4	active count	
3-0	recovery count	

Name	Function	Index
ARTTIM23	Drive 2/3 Address Setup Register (RW)	57h
Bits		
7-6	Address setup count 00—4 clks 01—2 clks 10—3 clks 11—5 clks	
5	reserved	
4	IDE drive 2/3 interrupt status Read ARTTIM23 will clear this bit 0—no interrupt pending 1—interrupt pending	
3	Drive 3 read ahead 0—enable 1—disable (default)	
2	Drive 2 read ahead 0—enable 1—disable (default)	

Name	Function	Index
DRWTIM23	Drive 2/3 Data Read/Write Timing Register (RW)	58h
Bits		
7-4	active count	
3-0	recovery count	

Name	Function	Index
BRST	Burst Length Control Register (RW) default = 40h This value equals the read-ahead count in quad words. Example: 40h x 8 = 200h (512) bytes	59h

1.3.3 Active Count Function

Active Count	R/W Active Time
0000	16 clks
0001	2 clks
0010	2 clks
0011	3 clks
0100	4 clks
0101	5 clks
0110	6 clks
0111	7 clks
1000	8 clks
1001	9 clks
1010	10 clks
1011	11 clks
1100	12 clks
1101	13 clks
1110	14 clks
1111	15 clks

1.3.4 Recovery Count Function

	Read Recovery Time		
Recovery Count	Active count 0 or 4 to15	Active count 1 to 3	Write Recovery Time
0000	17 clks	17 clks	17 clks
0001	3 clks	2 clks	3 clks
0010	3 clks	3 clks	3 clks
0011	4 clks	4 clks	4 clks
0100	5 clks	5 clks	5 clks
0101	6 clks	6 clks	6 clks
0110	7 clks	7 clks	7 clks
0111	8 clks	8 clks	8 clks
1000	9 clks	9 clks	9 clks
1001	10 clks	10 clks	10 clks
1010	11 clks	11 clks	11 clks
1011	12 clks	12 clks	12 clks
1100	13 clks	13 clks	13 clks
1101	14 clks	14 clks	14 clks
1110	15 clks	15 clks	15 clks
1111	16 clks	16 clks	16 clks

1.3.5 Task File Registers

Name	Host Addr	Function
HDATA*	1F0(170)	data register (RW)
HDWPC	1F1(171)	write pre-comp (WO)
HDERR	1F1(171)	error register (RO)
HDSCT	1F2(172)	sector count (RW)
HDSSN	1F3(173)	starting sector # (RW)
HDCLL	1F4(174)	cylinder low (RW)
HDCLH	1F5(175)	cylinder high (RW)
HDSDH	1F6(176)	SDH (RW)
HDCMD	1F7(177)	command (WO)
HDSTT	1F7(177)	status (RO)
HDFDR	3F6(376)	fixed disk control auxiliary register (WO)
HDASR	3F6(376)	alternate status auxiliary register (RO)

*HDATA can be accessed as a 16-bit-wide register, for all commands. HDATA can be accessed as a 32-bit-wide register for read/read multiple/write/write multiple commands when read ahead is enabled.

1.4 Configuration Setup

1.4.1 VL Mode

1) Write to port 78h (178h) with 5xh to set the register index.

2) Read/write port 7Ch (17Ch) to access the selected register.

1.4.2 PCI Mode Configuration

Depending on your motherboard chip set, either Configuration Mechanism #1 or Configuration Mechanism #2 is applicable. Configuration Mechanism #2 is described below. For Configuration #1 methodology, refer to the PCI Spec 2.0.

Notes:

1) Although PCI BIOS (INT 1Ah) is a portable alternative to Mechanism #1 and #2, it is not recommended because MS-DOS's EMM386.SYS causes the system to hang when function Find PCI Device is accessed (AMI and Phoenix BIOS).

2) The PCI-0640B supports byte/word/dword reads, but supports only byte/word writes to the configuration registers.

1.4.3 Configuration Mechanism #2

1) Enter PCI Configuration Mode by writing 10h to port CF8h.

2) Scan the PCI device IDs from 0h to Fh for the presence of a PCI-0640B controller. (There should be 1095h in port Cx00h and 0640h in port Cx02h, where x=device ID.)

3) To read or write internal registers, read or write to port Cxyyh, where x=device ID from (2) and yy=configuration register's index.

4) Exit PCI Configuration Mode by writing 00 to port CF8h.

1.4.4 VL-Mode Operation

1) If multiple PCI0640B devices are present, the host CPU selects a PCI0640B device for an I/O IDE operation by writing device ID (60h to 63h) to 078h (or 178h). This step is skipped if only one PCI0640B is present in the system.

2) Normal I/O requests to IDE drives can then be processed.

1.5 PCI0640B Interrupt Processing on PCI

When DSA1 is pulled low during reset, both IDE ports are in PCI IDE Legacy Mode. When DSA1 has no pull-down during reset, each IDE port may independently be set to PCI IDE Legacy Mode or Native Mode via the Programming Interface Byte (configuration register PROGIF, Index 9h).

When an IDE port is in PCI IDE Legacy Mode, the PCI-0640B is compatible with standard ISA IDE. The IDE task file registers are mapped to the standard ISA port addresses, and IDE drive interrupts occur at IRQ14 (primary) or IRQ15 (secondary).

When an IDE port is in PCI IDE Native Mode, the IDE task file registers may be mapped to non-standard port addresses, and IDE drive interrupts occur at PCI INTA. Therefore, if both IDE ports are in PCI IDE Native Mode, drive interrupts from both IDE ports are multiplexed into PCI INTA. In this case, the interrupt status bits must be polled to determine which IDE port generated the interrupt, or whether the interrupt was generated by another PCI device sharing INTA on the bus.

1) The host reads CFR (index 50h). If bit 2 is set, then the interrupt occurred on the primary IDE port.

2) The host reads ARTIM23. If bit 4 is set, then the interrupt occurred on the secondary IDE port.

3) If 1) and 2) are both false, then the interrupt was generated by another PCI device sharing INTA with the PCI-0640B.

1.6 Read Ahead Operation

The chip will snoop the IDE command register. If a read or read multiple command is written to it, then the chip will load the readahead count according to the current BRST register (index 59h) setting.

1.7 PCI0640B IDE Controller Pinout

1.7.1 Host Interface Pinout

PCI	Pin #	I/O	Function
ENIDE	21	I	Enable chip operation
PCICLK	89	I	Clock input
RESET#	1	I	Reset input
PCIMODE	2	I	Tied HIGH if PCI mode
FRAME#	98	I	
IRDY#	99	I	
TRDY#	92	B/T	
DEVSEL#	93	T	

PCI	Pin #	I/O	Function
STOP#	97	B/I	
IDSEL	100	I	
PAR	96	B/I	
IRQ14	22	T	Tri-state output to interrupt 14 (PC-AT compatible)
C/BE#<3>	3	I	
C/BE#<2>	4	I	
C/BE#<1>	5	I	
C/BE#<0>	6	I	
DIOR#	77	O	IOR# for the secondary IDE port
DIOW#	78	O	IOW# for the secondary IDE port
DCS3#	79	O/I	Drive chip select for 176
DCS2#	80	O/I	Drive chip select for 17x
	81	I	
	82	I	
IRQ15	83	O	To interrupt 15 (PC-AT compatible)
INTA#	84	O/C	Interrupt request to PCI host
ENDSKCHG#	85	I	Enable or disable 3F7 port decode
DIRQ2	86	I	
	87	I	
	88	I	
	94	I	
PERR#	95	B/I	
AD<31>	7	B	
AD<30>	8	B	
AD<29>	9	B	
AD<28>	10	B	
AD<27>	11	B	
AD<26>	12	B	
AD<25>	13	B	
AD<24>	14	B	
AD<23>	17	B	
AD<22>	18	B	
AD<21>	19	B	
AD<20>	20	B	
AD<19>	23	B	
AD<18>	24	B	
AD<17>	25	B	
AD<16>	26	B	
AD<15>	28	B	
AD<14>	29	B	
AD<13>	30	B	
AD<12>	31	B	

PCI	Pin #	I/O	Function
AD<11>	32	B	
AD<10>	33	B	
AD<9>	34	B	
AD<8>	35	B	
AD<7>	42	B	
AD<6>	43	B	
AD<5>	44	B	
AD<4>	45	B	
AD<3>	46	B	
AD<2>	47	B	
AD<1>	48	B	
AD<0>	49	B	

1.7.2 Drive Interface Pinout

PCI	Pin #	I/O	Function
DRST#	59	O	Drive Reset
IOCHRDY	76	I	I/O channel ready
DCSO#	55	O	Drive chip select for 1Fx
DCS1#	56	O	Chip select for 3F6
DSA<2>	70	O	Drive address 2
DSA<1>	69	O	Drive address 1
DSA<0>	68	O	Drive address 0
DIOR#	57	O	Drive IOR#
DIOW#	58	O	Drive IOW#
DSD<15>	36	B	
DSD<14>	37	B	
DSD<13>	38	B	
DSD<12>	39	B	
DSD<11>	50	B	
DSD<10>	51	B	
DSD<9>	52	B	
DSD<8>	53	B	
DSD<7>	62	B	
DSD<6>	63	B	
DSD<5>	64	B	
DSD<4>	65	B	
DSD<3>	71	B	
DSD<2>	72	B	
DSD<1>	73	B	
DSD<0>	74	B	
DIO16#	61	I	Drive IO16#

PCI	Pin #	I/O	Function
DIRQ1	75	I	Drive IRQ
NC	60		

1.7.3 VDD/VSS Pins

VDD Pins	VSS Pins
16	15
41	27
67	40
91	54
	66
	90

1.8 Jumper Settings

DSA0	0—Disable Chip ID port address decoding 1—Enable Chip ID port address decoding
DSA2	0 = Device ID port address is 178h 1 = Device ID port address is 078h
DSA1	0—Disable Base Address Registers. Base Address Registers always return 0. Primary channel uses IRQ14. Secondary channel uses IRQ15. IDE task file registers are mapped to the default port addresses of 1Fx (primary) and 17x (secondary). 1—Enable Base Address Registers. Base Address Registers respond as defined in PCI IDE spec 0.6 under control of PROGIF register. (See page 1-11.)
DCS1#, DCS#0	Device ID Selection (for multiple chip only) 00—60h 01—61h 10—62h 11—63h When Chip ID port address decoding is enabled, writing to the device ID port with a value other than the currently selected Device ID will disable the chip *including its configuration space*.
ENDSKCHG#	Drive Address Register enable/disable (3F7/377 when DSA1 = 0) 1—disable (default) 0—enable (2.2K)

Note: 0 = 2.2K pull-down
1 = no pull-down

2 Power Specifications

2.1 DC Specifications

2.1.1 Maximum Ratings

Symbol	Parameter	Limits	Units
VDD	DC supply voltage	Vss-0.5V to 6.5V	Volts
Vinm	Maximum input Voltage	Vss-0.5 to VDD+0.5	Volts
Voutm	Maximum output Voltage	Vss-0.5 to 5.5V	Volts
Topr	Storage Temperature	-65 to 150	Deg. C

2.1.2 Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
VDD	DC supply voltage	4.75	5.25	Volts
Vin	Input Voltage	Vss	VDD	Volts
Vout	Output Voltage	Vss	VDD	Volts
Topr	Operating Temperature	0	70	Deg. C

2.2 DC Characteristics

(For VDD= 5V, 0 to 70 Deg. C)

Symbol	Parameter	Min	Max	Units	Notes
VIL	Input Voltage Low	-0.3	0.8	Volts	Note 4
VIH	Input Voltage High	2.0	VDD+0.3	Volts	Note 4
VILC	CMOS level Input Voltage Low	-0.3	0.8	Volts	Note 1,4
VIHC	CMOS Level Input Voltage High	3.7	VDD+0.3	Volts	Note 1,4
VOL	Output Voltage Low		0.46 0.45	Volts Volts	Note 2,4,5 Note 2,4,6
VOH	Output Voltage High IOH = -2mA	2.4		Volts	Note 2,4
ILI	Input Leakage Current		15	µA	Note 30 V< VOL< VCC
IIL	Input Leakage Current	-400		µA	Note 3,4 VIL = 0.45

ILO	Output Leakage Current		15	µA	0.45< Vout< VCC
CIN	Input or I/O Capacitance		10	PF	

Notes:

1. CMOS Input level pin are = ENIDE, PCICLK, PCIMOD
2. TRDY#, STOP#, PAR, PERR# are PCI compliant driver pins, see specification.
3. DCS3#, DCS2#, IRQ15, INTA#, DIRQ23, IOCHRDY, CS0#, CS1#, DSA0, DSA1, DSA2, DSD0, DIO16# and DIRQ1 inputs each have an internal pullup transistor. In this case, IIL spec. will take precedance.
4. RESET#, IOCHRDY#, DIO16# and DIRQ1 are TTL Schmitt trigger input pins, Please refer to graphs for typical input output and pull up characteristic.
5. IOL = 8mA : DEVSEL#, IRQ14, IRQ15, INTA#, AND AD[0..31]
6. IOL = 16mA: DCS3#, DCS2#, DRST#, CS0#, CS1#, DSA[0..2], DIOR#, DIOW# and DSD[0..15].

2.3 AC Specifications

2.3.1 Timing Waveform

All AC timing is measured from the 0.8V and 2.0V on the source signal to the 0.8V and 2.0V level on the signal under test.

2.3.2 Clock Timing

Parameter	Min	Max	Units
CLK Frequency	0	50	MHz
CLK Period	20		ns
CLK High Time	7		ns
CLK Low Time	7		ns
CLK Rise Time		2	ns
CLK Fall Time		2	ns

2.3.3 Host Interface Timing (loading = 50 pf)

Signal		Min (ns)	Max (ns)
FRAME#, IRDY#, CBE#, AD[0..31]	Setup time to CLK high	7	
DEVSEL #	High to low from CLK high Low to high from CLK high	5 4	16 14
TRDY#	High to low f rom CLK high Low to high from CLK high	4 4	14 13
AD[0..31]	Read delay from CLK high	6	19
AD[0..31]	Active to float delay from CLK high	4	16

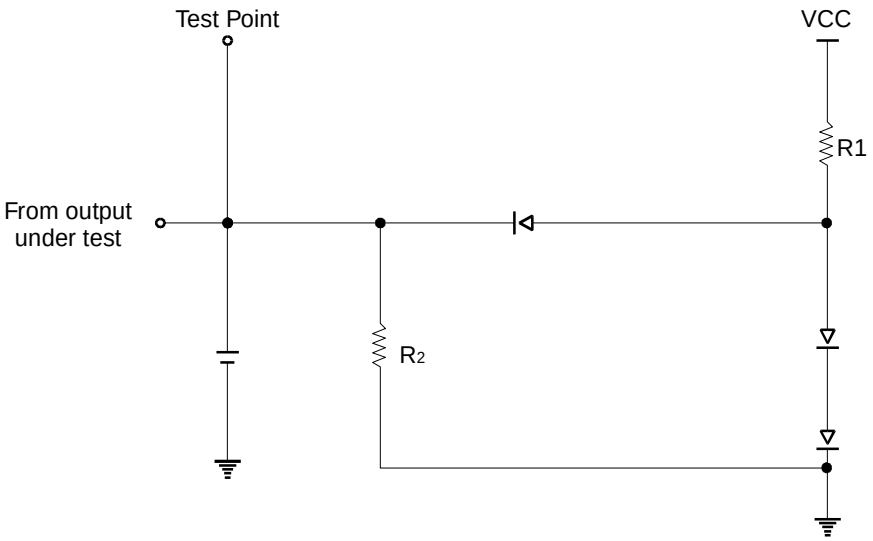
2.3.4 IDE Drive Timing (loading = 75 pf)

Signal		Min (ns)	Max (ns)
DCS0#, DCS1#, DSA[0..2]	High to low from CLK high Low to high from CLK high	9 6	28 21
DIOR#, DIOW#	High to low from CLK high Low to high from CLK high	7 5	24 19
DSD to DIOW# (2 CLKS)	Low to high setup time Hold time	45 50	56 57
DCS0# low to DIOW#, DIOR# low for port 1F0h		52	59
DIOW#, DIOR# high to DCS0# high for port 1F0h		62	68
IOCHRDY to CLK high setup time		10	

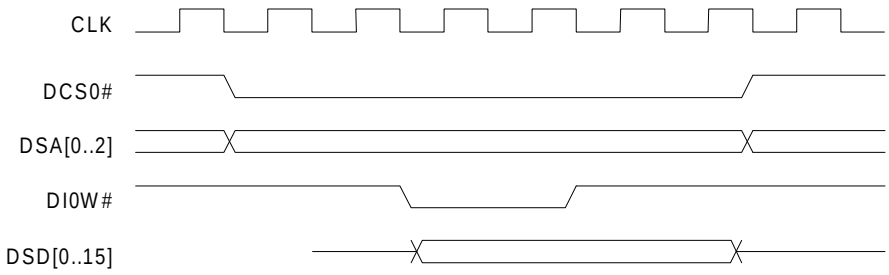
2.3.5 IDE Drive Timing (loading = 120 pf)

Signal		Min (ns)	Max (ns)
DCS0#, DCS1#, DSA[0..2]	High to low from CLK high Low to high from CLK high	10 7	37 24
DIOR#, DIOW#	High to low from CLK high Low to high from CLK high	8 6	29 20
DSD[0..15] to DIOW# (2 CLKS)	Low to high setup time Hold time	45 50	56 56
DCS0# low to DIOW#, DIOR# low for port 1F0h		49	55
DIOW#, DIOR# high to DCS0# high for port 1F0h		53	60
IOCHRDY to CLK high setup time		10	

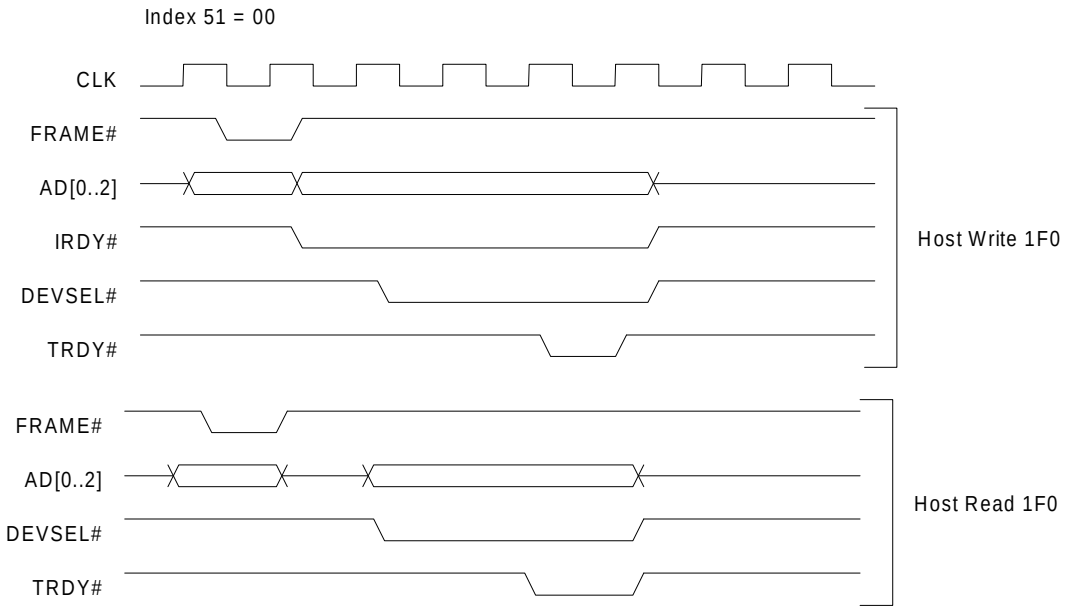
2.4 Output Test Load

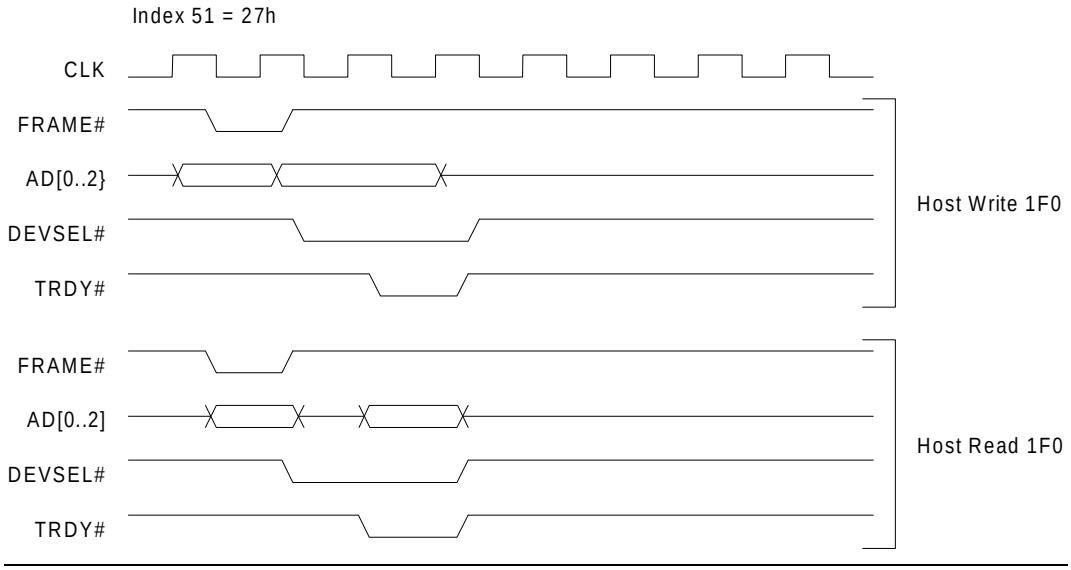


2.5 IDE Write Timing



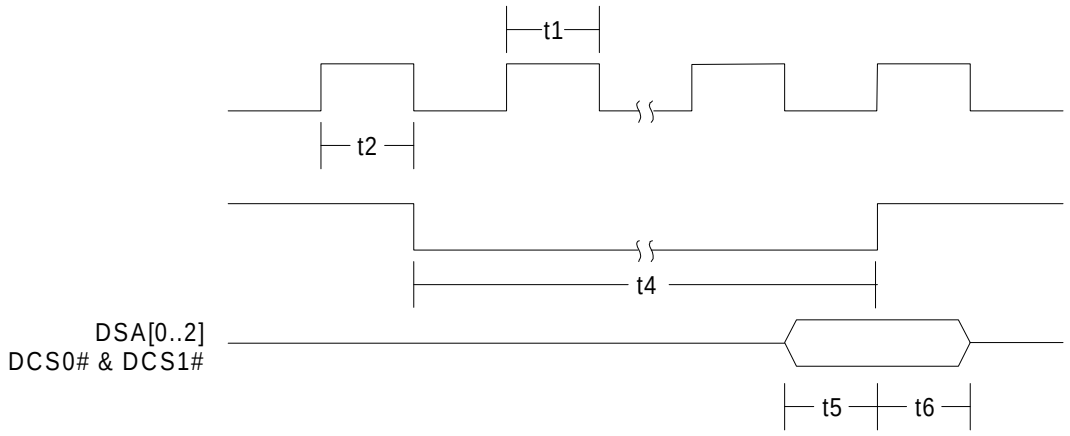
2.6 Host Read/Write Timing





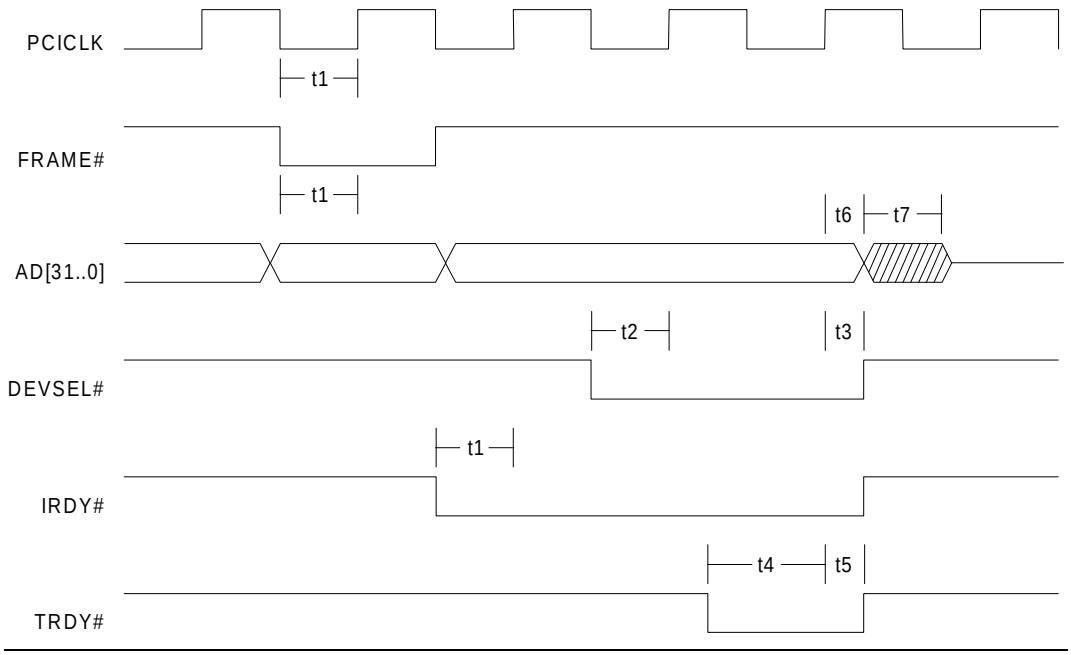
If Index 51 = 07h, host writing 1F0 will have one more clock cycle.

2.7 VCLK, RESET# Timing



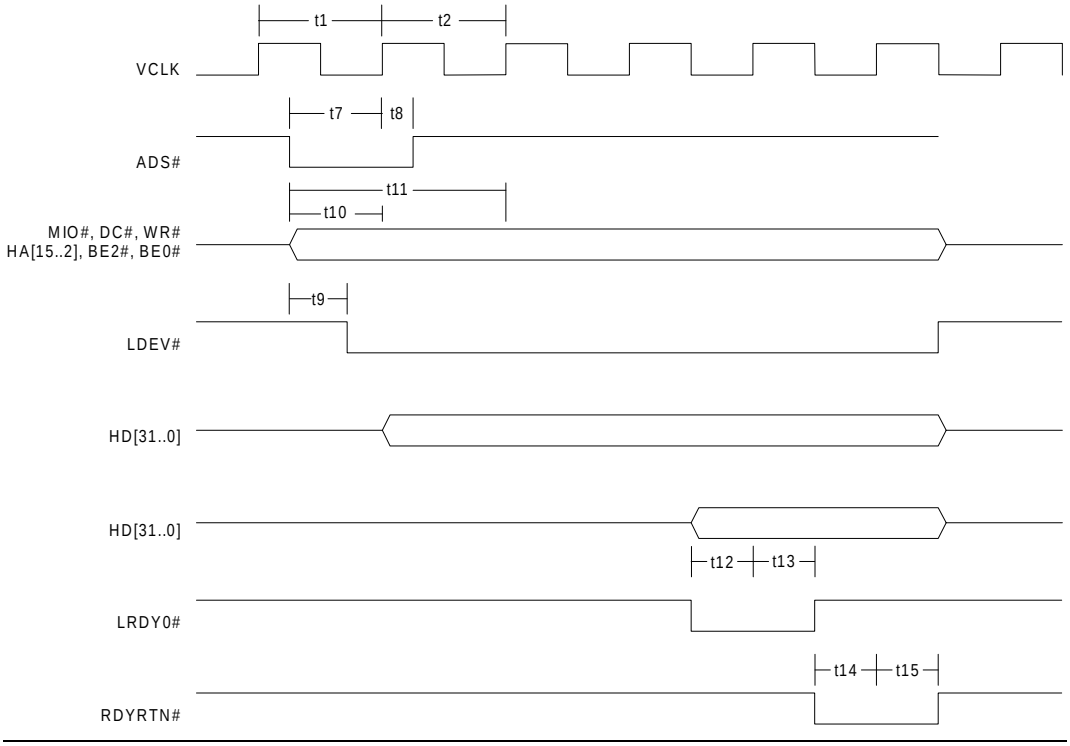
Symbol	Parameter	Min	Max	Unit
t1	VCLK Period	20	—	ns
t2	VCLK high time	5	—	ns
t3	VCLK low time	5	—	ns
t4	RESET# pulse width	16	—	VCLK
t5	Pos pin to RESET# setup time	200	—	ns
t6	Pos pin hold time from RESET#	10	—	ns

2.8 PCI Host Timing



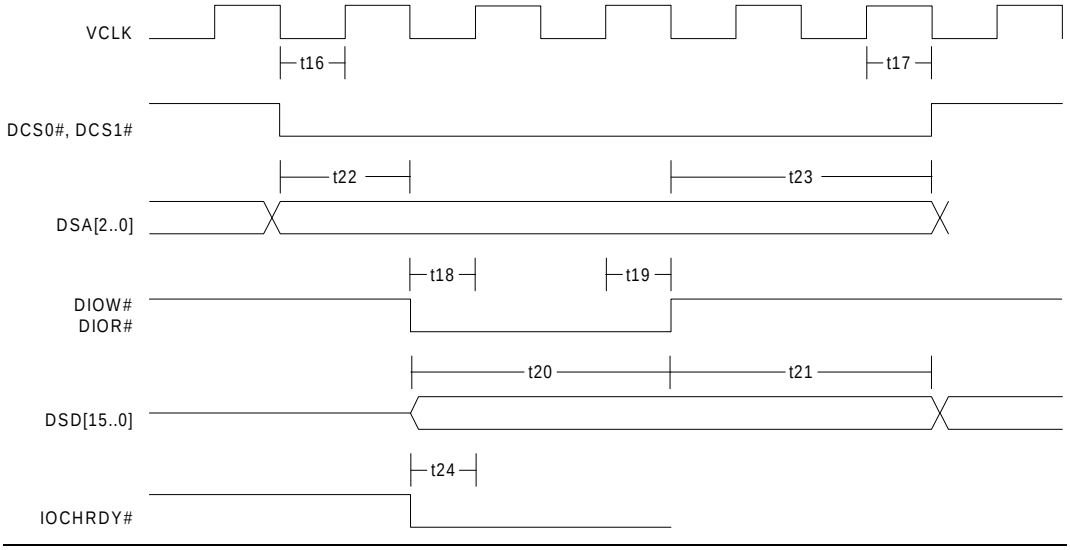
Symbol	Parameter	Timing
t1	FRAME#, irdy#, c/be[3..0]#, AD[31..0] setup time	7 ns
t2	DEVSEL#, high to low from CLK high	5-16 ns
t3	DEVSEL, low to high from CLK high	4-14 ns
t4	TRDY#, high to low from CLK high	4-14 ns
t5	TRDY#, low to high from CLK high	6-13 ns
t6	AD[31..0] hold time	6-19 ns
t7	active to float delay from CLK	5-16 ns

2.9 VL Mode Timing



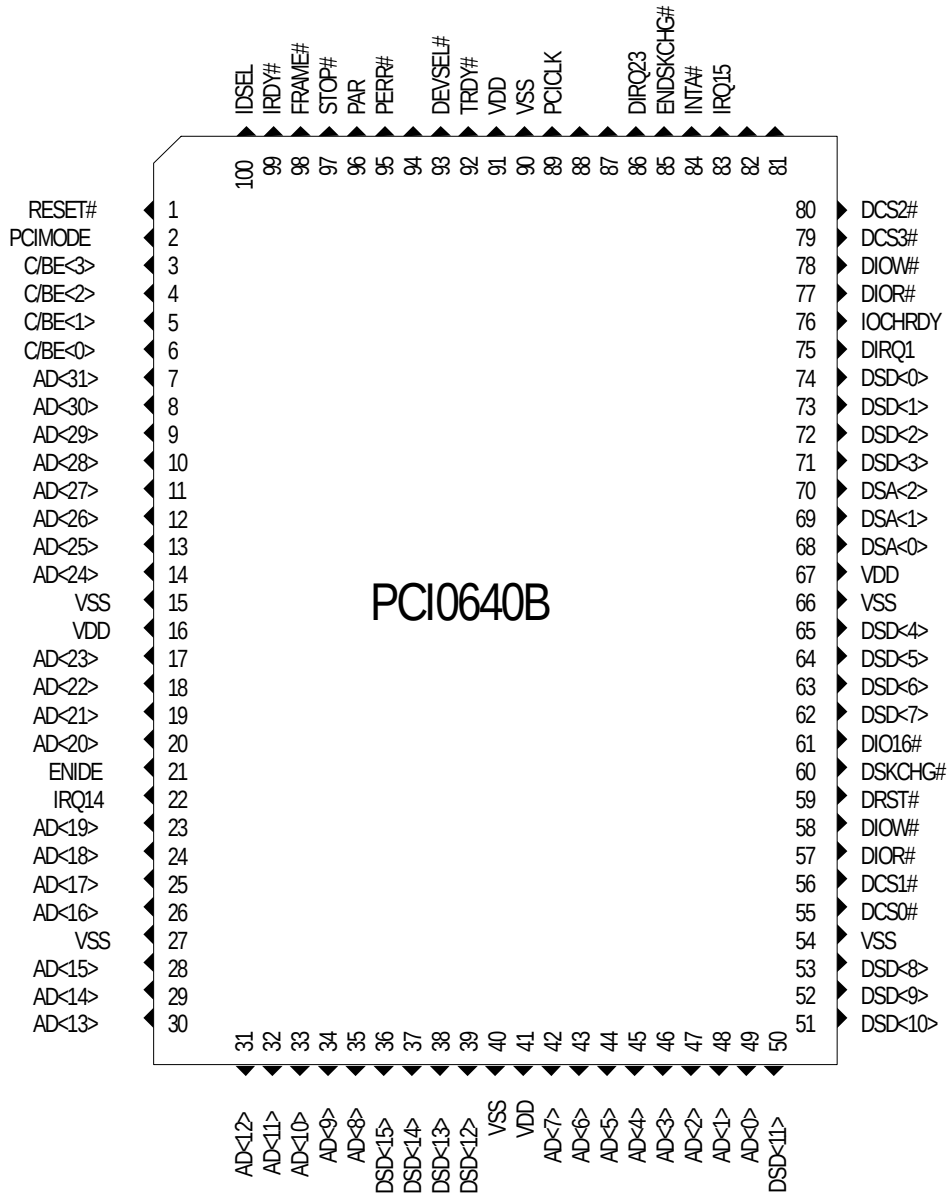
Symbol	Parameter	Timing
t7	ADS# to VCLK setup time	7 ns
t8	ADS# to VCLK hold time	6 ns
t9	LDEV# active delay from address	3-9 ns
t10	MIO#, DC#, WR# to VCLK setup time at t1	5 ns
t11	MIO#, DC#, WR# to VCLK setup time at t2	10 ns
t12	LRDY0# active delay from VCLK	4-14 ns
t13	LRDY0# inactive delay from VCLK	4-13 ns
t14	RDYRTN# to VCLK setup time	6 ns
t15	RDYRTN# to VCLK hold time	4 ns

2.10 IDE Timing



Symbol	Parameter	Timing
t16	DCS0#, DCS1#, DSA[2..0] high to low from CLK high	9-28 ns
t17	DCS0#, DCS1#, DSA[2..0] low to high from CLK high	6-21 ns
t18	DIOR#, DIOW# high to low from CLK high	7-24 ns
t19	DIOR#, DIOW# low to high from CLK high	5-13 ns
t20	DSD[15..0] to DIOW# setup time	45-56 ns
t21	DSD[15..0] to DIOW# hold time	50-67 ns
t22	DCS0# low to DIOW#, DIOR# low for port 1F0	52-59 ns
t23	DIOW#, DIOR# high to DCS0# high for port 1F0	62-68 ns
t24	IOCHRDY to CLK high setup time	10 ns

A Diagrams


PCI0640B
1 RESET#
2 PCIMODE
3 C/BE<3>
4 C/BE<2>
5 C/BE<1>
6 C/BE<0>
7 AD<31>
8 AD<30>
9 AD<29>
10 AD<28>
11 AD<27>
12 AD<26>
13 AD<25>
14 AD<24>
15 VSS
16 VDD
17 AD<23>
18 AD<22>
19 AD<21>
20 AD<20>
21 ENIDE
22 IRQ14
23 AD<19>
24 AD<18>
25 AD<17>
26 AD<16>
27 VSS
28 AD<15>
29 AD<14>
30 AD<13>
31 AD<12>
32 AD<11>
33 AD<10>
34 AD<9>
35 AD<8>
36 DSD<15>
37 DSD<14>
38 DSD<13>
39 DSD<12>
40 VSS
41 VDD
42 AD<7>
43 AD<6>
44 AD<5>
45 AD<4>
46 AD<3>
47 AD<2>
48 AD<1>
49 AD<0>
50 DSD<11>
51 DSD<10>
52 DSD<9>
53 DSD<8>
54 VSS
55 DCS0#
56 DCS1#
57 DIOR#
58 DIOW#
59 DRST#
60 DSKCHG#
61 DIO16#
62 DSD<7>
63 DSD<6>
64 DSD<5>
65 DSD<4>
66 VSS
67 VDD
68 DSA<0>
69 DSA<1>
70 DSA<2>
71 DSD<3>
72 DSD<2>
73 DSD<1>
74 DSD<0>
75 DIRQ1
76 IOCHRDY
77 DIOR#
78 DIOW#
79 DCS3#
80 DCS2#
81 IRQ15
82 INTA#
83 ENDSKCHG#
84 DIRQ23
85 VSS
86 VDD
87 TRDY#
88 DEVSEL#
89 PERR#
90 PAR
91 STOP#
92 FRAME#
93 IRDY#
94 IDSEL
95 PCICLK
96 100

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