TEXAS INSTRUMENTS

TPS54673EVM-225 6-Amp TPS54873EVM-225 8-Amp

SWIFT™ Regulator With Disabled Sink During Start-Up Evaluation Module

User's Guide

January 2003

PMP EVMs

SLVU079

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Preface

Read This First

About This Manual

This user's guide describes the characteristics, operation, and use of the TPS54673EVM–225 and TPS54873EVM–225 evaluation modules. It covers all pertinent areas involved to properly use this EVM board along with the devices that it supports. The physical PCB layout, schematic diagram, and circuit descriptions are included.

How to Use This Manual

This document contains the following chapters:

- Chapter 1—Introduction
- Chapter 2—Test Setup and Results
- Chapter 3—Board Layout
- Chapter 4—Schematic and Bill of Materials

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Data Sheets:	Literature Number:
TPS54673	SLVS433
TPS54873	SLVS444

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Chapter 1

Introduction

This chapter contains background information for the TPS54673 and TPS54873, as well as support documentation for the TPS54673EVM-225 and TPS54873EVM-225 evaluation modules (SLVP225).

The TPS54x73EVM-225 performance specifications, schematic, and bill of materials are given.

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1.1 Background

The TPS54x73EVM-225 evaluation module uses the TPS54673 or TPS54873 synchronous buck regulators with disabled sink during start-up (DSDS) to provide an output voltage of from 0.9 V to 2.5 V from a nominal 3.3 V input or 0.9 V to 3.3 V for a nominal 5-V input. Rated input voltage and output current range is given in *Table 1–1*. These EVMs are designed to demonstrate the small PCB areas that may be achieved when designing with the TPS54x73 family of regulators. The swicthing frequency is set at a nominal 700 kHz, allowing the use of a small footprint 0.65 μH output inductor. The MOSFETs of the TPS54x73 are incorporated inside the TPS54x73 package. This eliminates the need for external MOSFETs and their associated drivers. The low drain-to-source on resistance of the MOSFETs gives the TPS54x73 high efficiency and helps to keep the junction temperature low at high output currents. The compensation components are provided external to the IC, and they allow for an adjustable output voltage and a customizable loop reponse. The disabled sink during start-up (DSDS) feature allows the TPS54x73 family of regulators to be used in applications where it is necessary to prebias the output to maintain a specified difference between I/O and core voltages during start-up.

Table 1–1. Input Voltage and Output Current Summary

EVM	Input Voltage Range	Output Current Range
TPS54673EVM-225	3.0 V to 6.0 V	–6 A to 6 A
TPS54873EVM-225	4.0 V to 6.0 V	–8 A to 8 A

1.2 Performance Specification Summary

A summary of the TPS54x73EVM–225 performance specifications is provided in *Table 1–2* and *Table 1–3*. All specifications are given for an an output voltage of 3.3 V and an output voltage of 2.5 V for the TPS54673 and an uput voltage of 5 V and an output voltage of 3.3 V for the TPS54873. The ambient temperature is 25°C, for all measurements, unless otherwise noted. The data presented in *Table 1–2* and *Table 1–3* are compiled with no precharge on the output (J3 open, no voltage source present on J4). Using the precharge circuitry on this EVM requires careful consideration of line and load conditions for proper operation and may limit the useful operating range of the TPS54x73 device.

Table 1–2. TPS54673EVM-225 Performance Specification Summary

Specification	Test Conditions	Min	Typ	Max	Units
Input voltage range		3.0	3.3 or 5.0	6.0	V
Output voltage set point		0.9	2.5	3.3	V
Output current range	V_I = 3 V to 6 V			6	A
Line regulation (see Note 1)	I_O = 3 A, V_I = 3.02 V to 6 V		±4		mV
Load regulation	V_I = 3.3 V, I_O = 0 A to 6 A		±4		mV
Load transient response	I_O = 1.5 A to 4.5 A, t_r = 40 µs		–20		mV_{PK}
			120		µs
	I_O = 4.5 A to 1.5 A, t_f = 40 µs		20		mV_{PK}
			100		µs
Loop bandwidth	V_I = 3 V		80		kHz
Phase margin	V_I = 3 V		48		°
Loop bandwidth	V_I = 6 V		125		kHz
Phase margin	V_I = 6 V		49		°
Input ripple voltage			245	275	mV_{PP}
Output ripple voltage			7	10	mV_{PP}
Output rise time		4.7	8.4	15	ms
Operating frequency			700		kHz
Maximum efficiency	V_I = 3.3 V, Vo = 2.5 V, I_O = 1.0 A		93%		

Note: Maximum duty cycle is approached as V_I approaches 3 V, limiting input voltage range for V_O = 2.5 V.

Table 1–3. TPS54873EVM-225 Performance Specification Summary

Specification	Test Conditions	Min	Typ	Max	Units
Input voltage range		4.0	5.0	6.0	V
Output voltage set point		0.9	3.3	3.3	V
Output current range	V_I = 4 V to 6 V			8	A
Line regulation	I_O = 4 A		±4		mV
Load regulation	V_I = 5 V, I_O = 0 A to 8 A		±5		mV
Load transient response	I_O = 2 A to 6 A, t_r = 40 µs		–18		mV_{PK}
			100		µs
	I_O = 6 A to 2 A, t_f = 40 µs		18		mV_{PK}
			80		µs
Loop bandwidth	V_I = 4 V		100		kHz
Phase margin	V_I = 4 V		45		°
Loop bandwidth	V_I = 6 V		125		kHz
Phase margin	V_I = 6 V		45		°
Input ripple voltage			360	400	mV_{PP}
Output ripple voltage			7	10	mV_{PP}
Output rise time		4.7	8.4	15	ms
Operating frequency			700		kHz
Maximum efficiency	V_I = 5 V, Vo = 3.3 V, I_O = 2.0 A		93.5%		

1.3 Modifications

The TPS54x73EVM-225 is designed to demonstrate the small size that can be attained when designing with the TPS54x73, so many of the features which allow for extensive modifications have been ommited from this EVM. Changing the value of R4 can change the output voltage in the range of 0.9 V to 3.3 V. The value of R4 for a specific output voltage can be calculated by using equation 1 . *Table 1–4* lists the values for R4 for some common output voltages.

$$R4 = 10\ k\Omega \times \frac{0.891\ V}{V_O - 0.891\ V} \tag{1}$$

Table 1–4. Output Voltage Programming

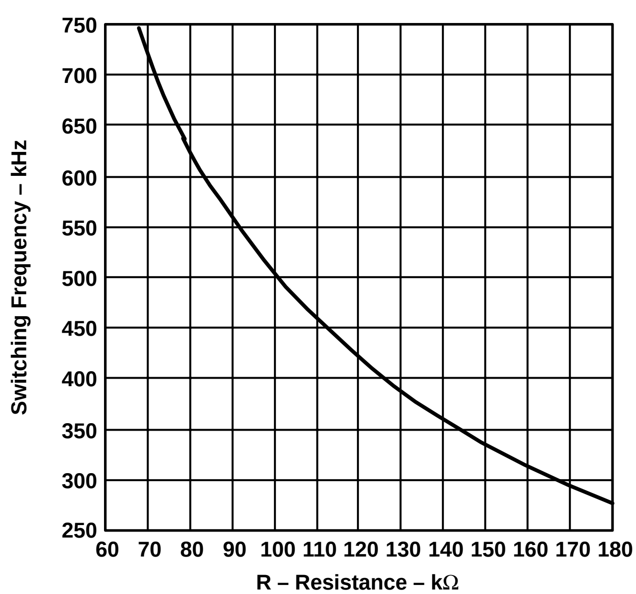
Output Voltage (V)	R4 Value (k)
0.9	1000
1.2	28.7
1.5	14.7
1.8	9.76
2.5	5.49
3.3	3.74

The minimum output voltage is limited by the minimum controllable on-time of the device, 200 ns, and is dependent upon the duty cycle and operating frequency. The approximat minimum output voltage can be calculated using:

$$V_{OUTMIN} = 200\ ns \times f_s \times V_{INMIN} \tag{2}$$

The switching frequency may be trimmed to any value between 280 kHz and 700 kHz by changing the value of R6. Decreasing the switching frequency results in increased output ripple, unless the value of L1 is increased. A plot of the value of RT versus the switching frequency is given in *Figure 1–1*.

Figure 1–1. Frequency Trimming Resistor Selection Graph



The TPS54x73EVM–225 EVM also supports alternate output filter configurations by means of pads located on the back side of the PCB. The positions for C15, C16, and C17 provide space for up to three electrolytic type surface, mount capacitors, while the position for L2 accommodates popular inductors such as Vishay IHLP-5050 series with a 0.5 in. × 0.5 in. package. Since changes in the output filter affect the overall loop response, the user may find it desirable to change the values used in the compensation network (R1, R2, R3, C1, C2, and C3). The 0-Ω resistor R8 in the feedback path is provided as a convenient place to break the loop for testing any compensation value changes. While the provided compensation network can provide a stable output for a wide variety of output filter component values, it is always a good idea to verify any changes to the output filter or compensation network.

The primary intended usage for the TPS54x73 device family is in applications requiring a precharge condition on the output. These types of applications include power supplies for DSPs and microprocessors where the I/O and core voltages must track each other within a certain amount during start-up. The TPS54673 and TPS 54873 incorporate disable sink during start-up (DSDS) to allow this type of functionality in the SWIFT™ family of dc/dc converters. A typical design approach is to tie the output of the core voltage to the output of the I/O voltage with a number of series diodes so that the core voltage are at a level equal to the I/O voltage minus the drop across the diodes during start-up. The TPS54x73EVM-225 EVM provides four series diodes, D1 through D4, and allows the user to precharge the output from either the EVM input voltage or an external source. To use the input voltage as the precharge source, install a jumper across the J3 header. To supply an external source, use the J4 connector terminals, while leaving J3 open. Headers J5 through J8 are provided to select the number of series diodes; install a jumper across the header to bypass the adjacent diode. Care must be taken to use the correct number of diodes for the application. Under no circumstances can the output voltage be allowed to precharge to a level higher than the preset output voltage. If this condition occurs during start-up, the TPS54x73 device does not begin switching. If a voltage transient on the precharge voltage source causes the series diodes to conduct, current may be sunk through the low side FET in the device, possibly damaging the device. The actual voltage drop across the diodes during start-up depends on the initial load condition of the circuit as well as the ambient temperature.

Chapter 2

Test Setup and Results

This chapter describes how to properly connect, set up, and use the TPS54x73EVM-225 evaluation module. The chapter also includes test results typical for the TPS54x73EVM-225 and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

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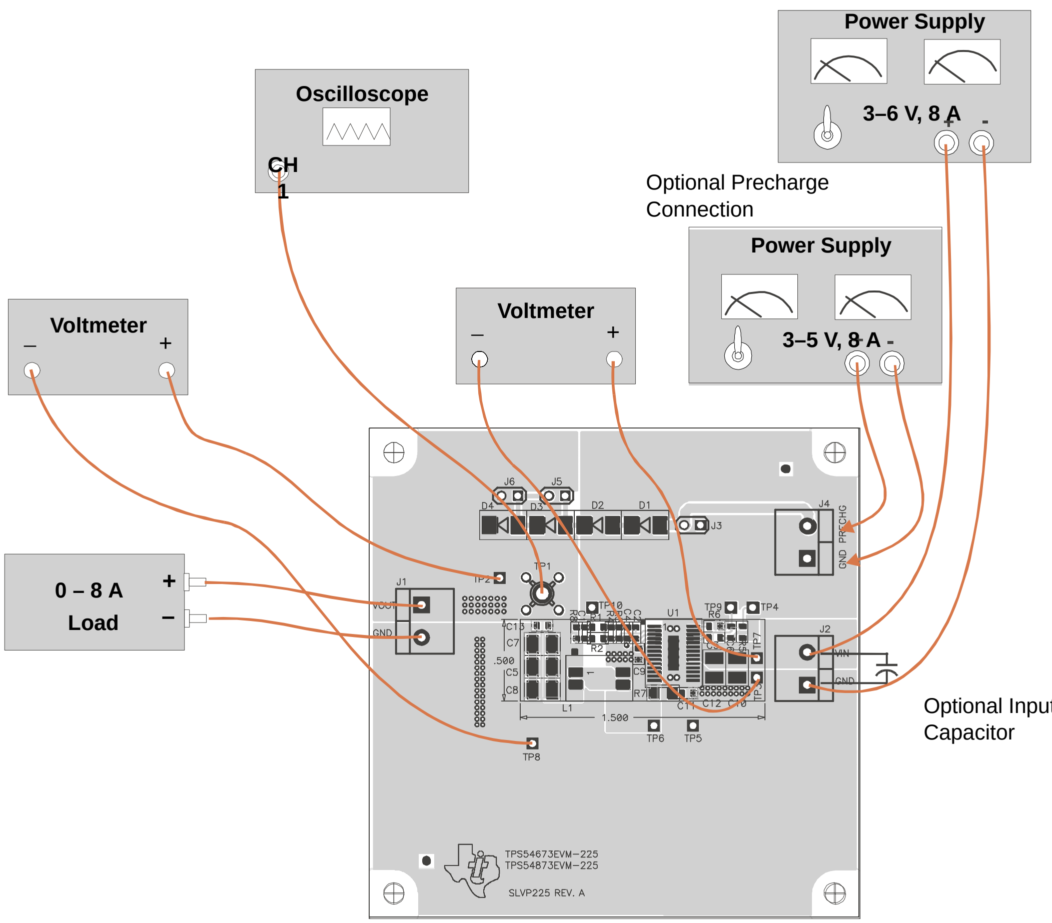
2.1 Input/Output Connections

The TPS54x73EVM-225 has the following input/output connections: Vout J1, Vin J2, and Prechg_in J4. A diagram showing the connection points is shown in Figure 2–1. A power supply capable of supplying 6 A should be connected to J2 through a pair of 20-AWG wires. The load should be connected to J2 through a pair of 16-AWG wires. The maximum load current may be reduced from 8 A for the TPS54873EVM–225 and 6 A for the TPS54673EVM–225. Wire lengths should be minimized to reduce losses in the wires. Test point TP1 provides a place to easily connect an oscilloscope voltage probe to monitor the output voltage. The TPS54X72 is intended to be used as a point of load regulator. In typical applications, it is usually located close to the input voltage source. When using the TPS54x73EVM-225 with an external power supply as the source for V_I, an additional bulk capacitor may be required, depending upon the output impedance of the source and length of the hookup wires. The test results presented are obtained using a 470 µF, 16-V additional input capacitor. Connection is shown for no precharge only. To utilize the precharge feature, connect the optional power supply to the J4 connector or connect the input voltage to the series diode array by inserting a jumper across the J3 header.

Figure 2–1. Connection Diagram



2.2 Efficiency

The TPS54x73EVM-225 efficiency peaks at load current of about 1 A to 2 A, and then decreases as the load current increases towards full load. The efficiency shown in *Figure 2–2* is for the TPS54673 and the TPS54873 at an ambient temperature of 25°C. The efficiency is lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the MOSFETs. The efficiency is slightly lower at 700 kHz than at lower switching frequencies, due to the gate and switching losses in the MOSFETs.

Figure 2–2. Measured Efficiency, TPS54673

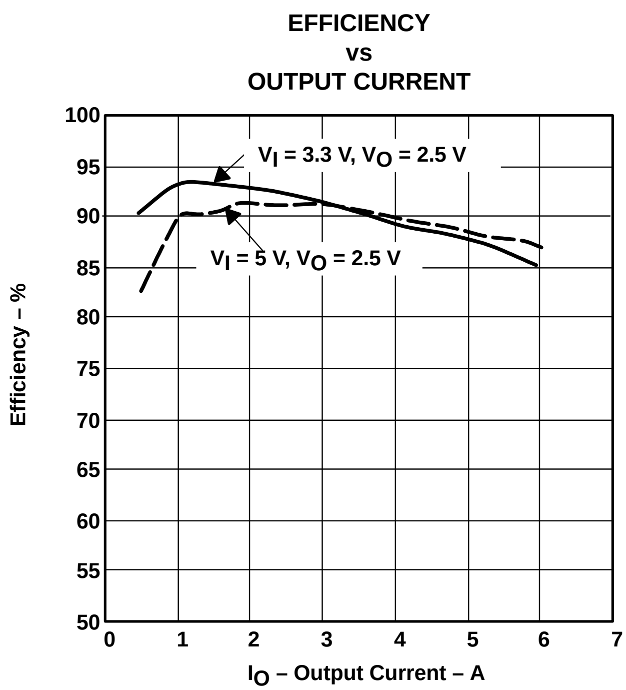
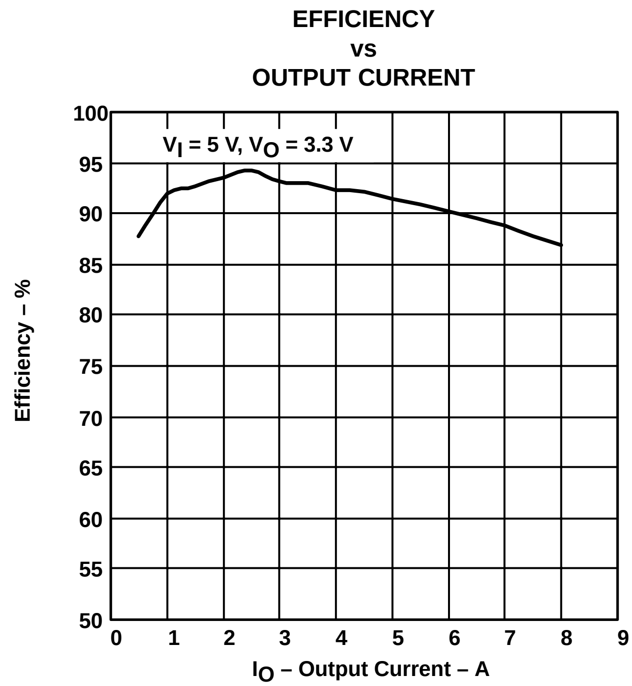


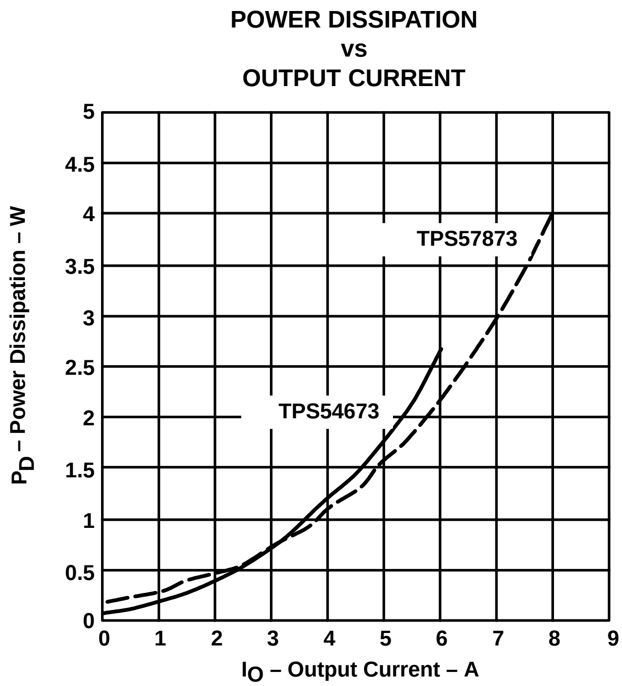
Figure 2–3. Measured Efficiency, TPS54873



2.3 Power Dissipation

The low junction-to-case thermal resistance of the PWP package, along with a good board layout, allows the TPS54x73EVM-225 EVMs to output full rated load current while maintaining safe junction temperatures. With a 3.3-V input source and a 6-A load, the junction temperature is approximately 60°C, while the case temperature is approximately 55°C. The total circuit losses at 25°C are shown in *Figure 2–4*. The input voltage for the TPS54673 is 3.3 V and for the TPS54673, 5.0 V. For additional information on the dissipation ratings of the devices, see the individual product data sheets.

Figure 2–4. Measured Circuit Losses



2.4 Output Voltage Regulation

The output voltage load regulation of the TPS54x73EVM-225 is shown in *Figure 2–5*, while the output voltage line regulation is shown in *Figure 2–6*. Measurements are given for an ambient temperature of 25°C.

Figure 2–5. Load Regulation

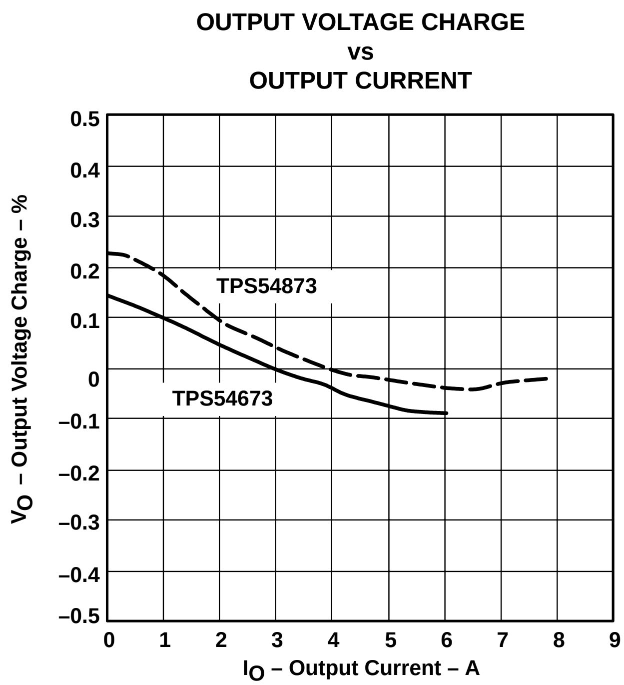
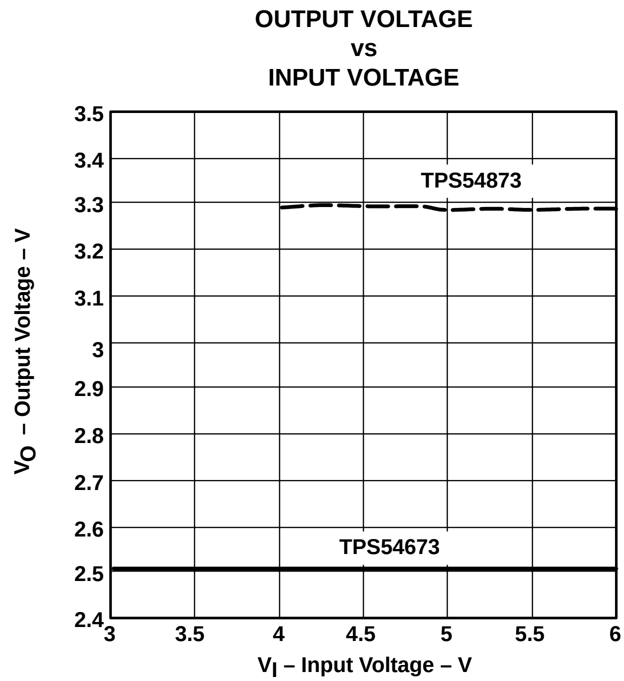


Figure 2–6. Line Regulation



Note: The lower limit for the TPS54673 input voltage is about 3.02 V because the device is operating at its maximum duty cycle.

2.5 Load Transients

The TPS54x73EVM–225 response to load transients is shown in *Figure 2–7* and *Figure 2–8*. The current step is from 25 to 75 percent of maximum rated load. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

Figure 2–7. Load Transient Response, TPS54673

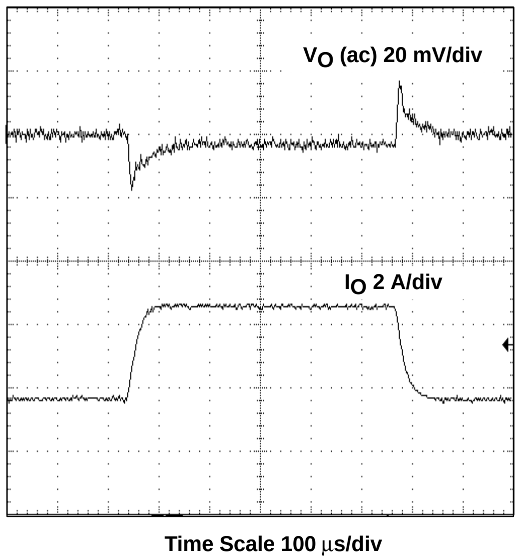
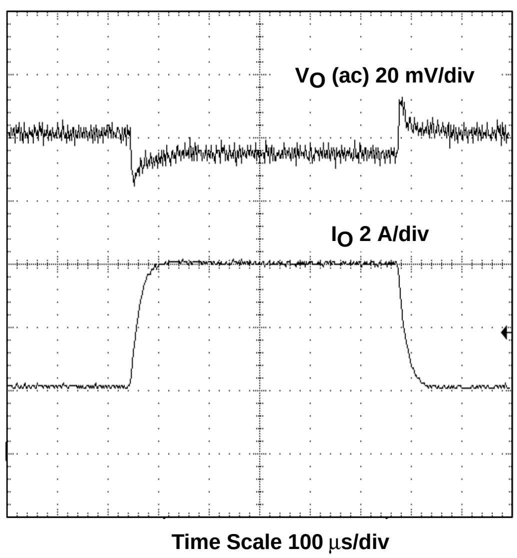


Figure 2–8. Load Transient Response, TPS54873



2.6 Loop Characteristics

The TPS54x73EVM-225 load response characteristics are shown in *Figure 2–9*, *Figure 2–10*, and *Figure 2–11*. The current step is from –50% to 50% of maximum rated load. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

Figure 2–9. Measured Loop Response, TPS54673, V_I = 3 V

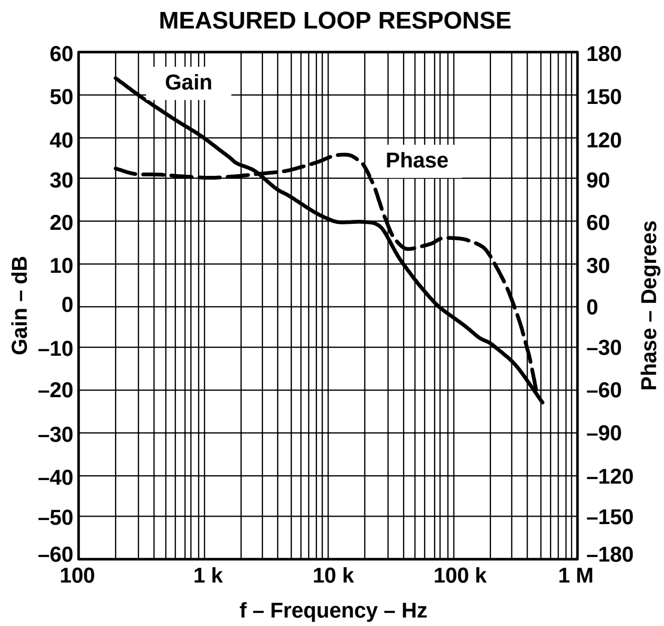


Figure 2–10. Measured Loop Response, TPS54673, V_I = 6 V

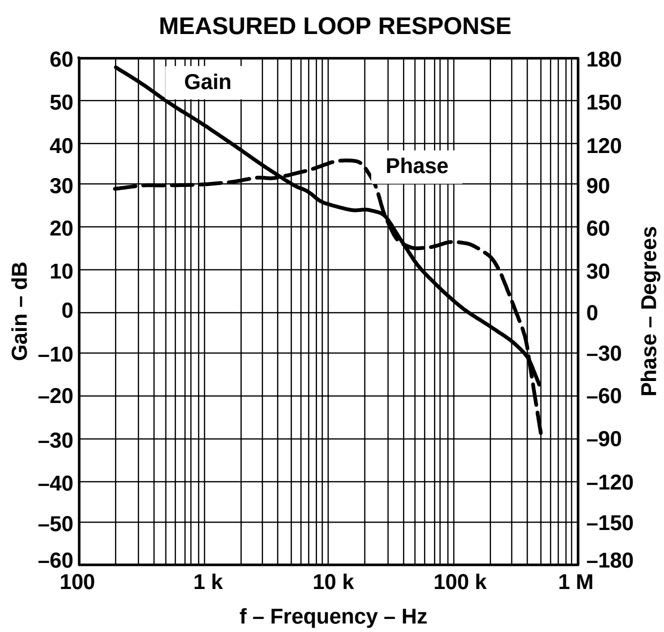


Figure 2–11. Measured Loop Response, TPS54873, V_I = 4 V

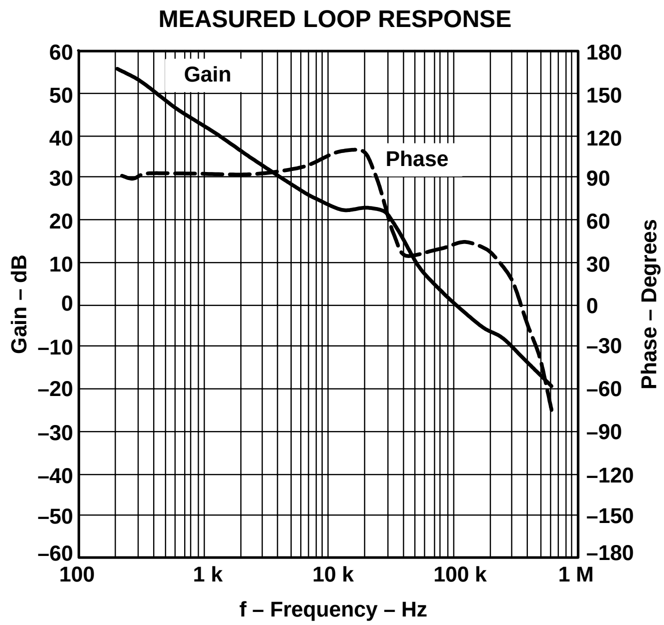
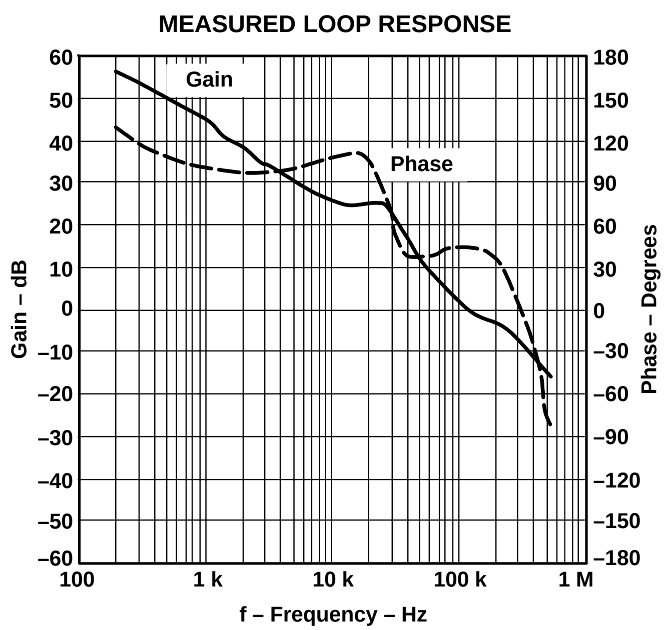


Figure 2–12. Measured Loop Response, TPS54873, V_I = 6 V



2.7 Output Voltage Ripple

The TPS54x73EVM-225 output voltage ripple is shown in *Figure 2–13* and *Figure 2–14* for each device type. The input voltage is 3.3 V for the TPS54673. The input voltage is 5 V for the TPS54873. Output current for each device is the rated full load. Voltage is measured directly across output capacitors.

Figure 2–13. Measured Output Voltage Ripple, TPS54673

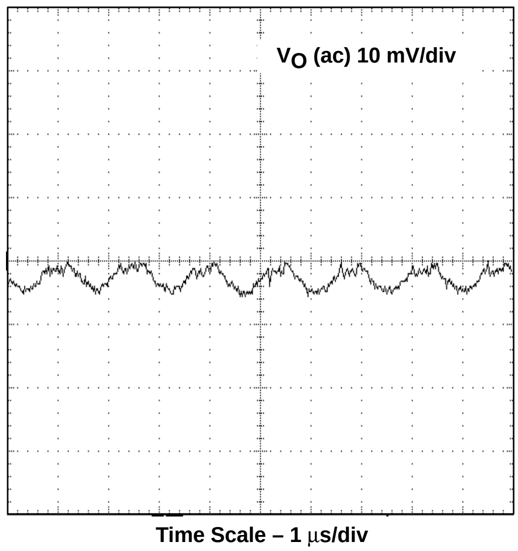
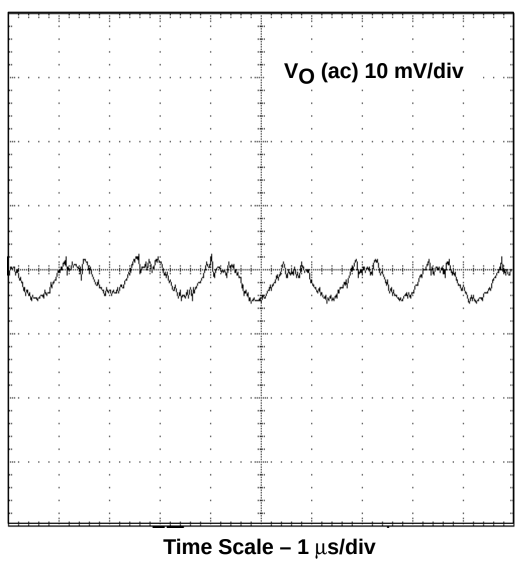


Figure 2–14. Measured Output Ripple Voltage, TPS54873



2.8 Input Voltage Ripple

The TPS54x73EVM-225 input voltage ripple is shown in *Figure 2–15* and *Figure 2–16* for each device type. The input voltage is 3.3 V for the TPS54673 the input voltage is 5 V for the TPS54873. Output current for each device is the rated full load.

Figure 2–15. Input Voltage Ripple, TPS54673

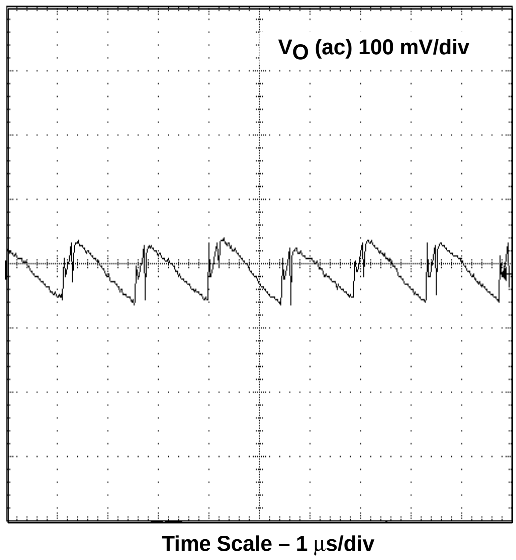
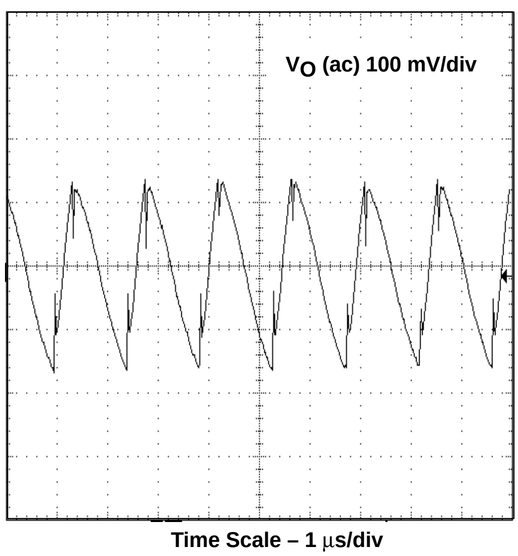


Figure 2–16. Input Voltage Ripple, TPS54873



2.9 Start-Up

Start-up voltage waveforms of the TPS54673EVM–225 are shown in *Figure 2–17* through *Figure 2–19*. Figure 2–17 shows the start-up waveform with no precharge on the output. When the V_I reaches the nominal 2.95-V UVLO threshold, the slow-start capacitor (C6) begins to charge. When the voltage on the SS/ENA pin reaches the enable threshold of 1.2 V, the internal reference begins to ramp up at the slow-start rate. As the internal reference voltage increases relative to the voltage at VSENSE, the duty cycle of the PWM comparator output increases. The internal FETs are inhibited from switching until the output of the PWM comparator reaches maximum duty cycle. When maximum duty cycle is reached, switching starts and the output rises quickly while the output voltage catches up with the slow-start ramp rate. At this point the voltage on the VSENSE pin matches the internal reference and the output continues to ramp up to the final set point value of 2.5 V at the slow-start rate.

Figure 2–17. Measured Start-Up Waveform, TPS54673 With No Precharge

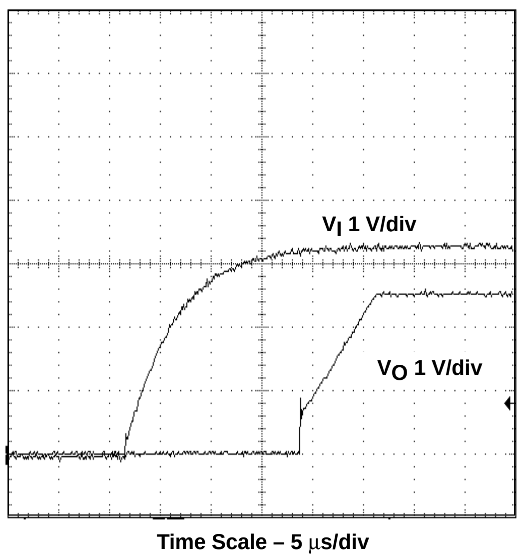


Figure 2–18 Shows the start-up waveform with the output precharged and a 2-Ω load. The precharge is achieved by connecting the 3.3-V input to the output with two diodes in series. The start-up mechanism is the same as described above except that the internal reference must ramp up above the voltage fed back from the precharged output to the VSENSE pin before switching can start. Once this occurs, the output continues to ramp up to the output set point of 2.5 V at the slow-start rate.

Figure 2–18. Measured Start-Up Waveform, TPS54373 With Precharge

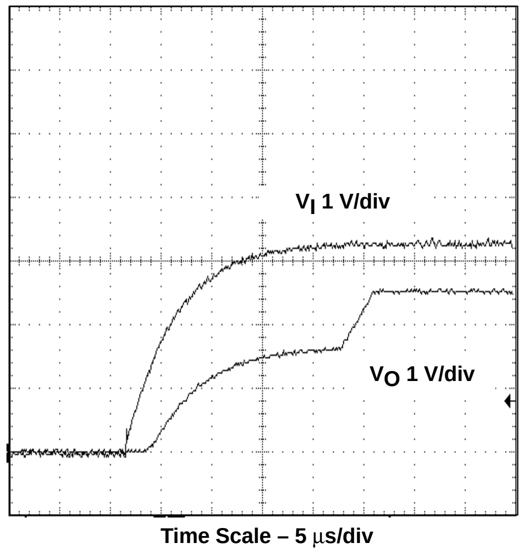


Figure 2–20 shows the start-up waveform with the output precharged and no load. Compare the precharge level to that in *Figure 2–18* to see how start-up load current affects the voltage drop across the diodes and the final precharge voltage. As in the previous example, when the internal reference exceeds the voltage fed back to the VSENSE pin, the output begins to ramp up to its final preset value at the slow-start rate. It is important to note how the precharge level in *Figure 2–19* is very close to the final output value. The precharge level must never exceed the output set point under any line or load condition for proper circuit operation.

Figure 2–19. Measured Start-Up Waveform, TPS54673 With Precharge and No Load

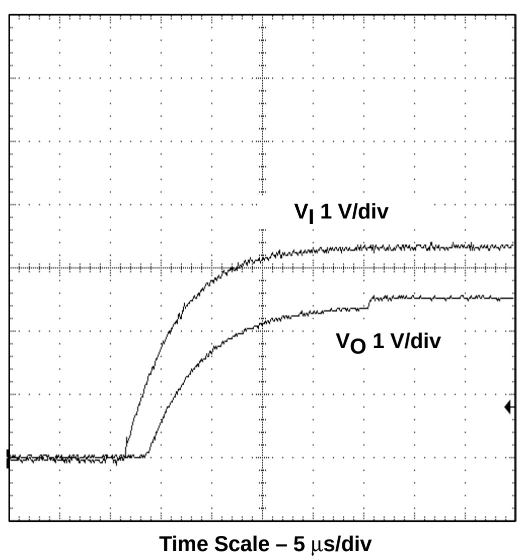


Figure 2–20, *Figure 2–21*, and *Figure 2–22* show the same series start-up waveforms for the TPS54873-225. The above descriptions of the TPS54673 waveforms are applicable for the TPS54873 except that the input voltage is 5 V, the output voltage is 3.3 V, and the UVLO start-up threshold is 3.8 V.

Figure 2–20. Measured Start-Up Waveform

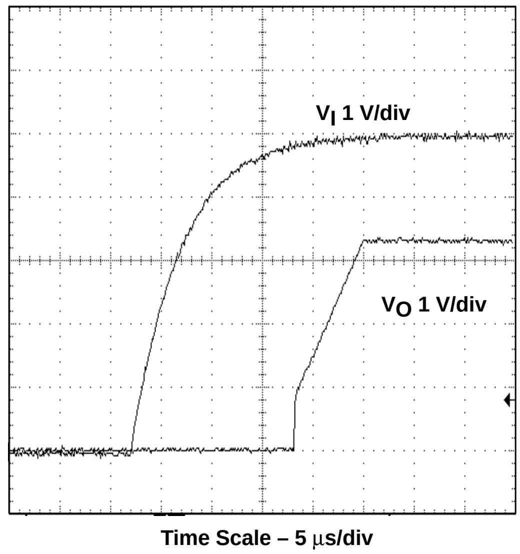


Figure 2–21. Measured Start-Up Waveform, TPS54873 With Precharge

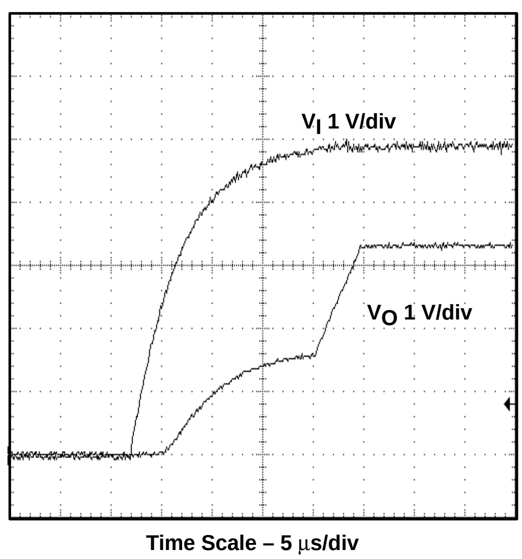
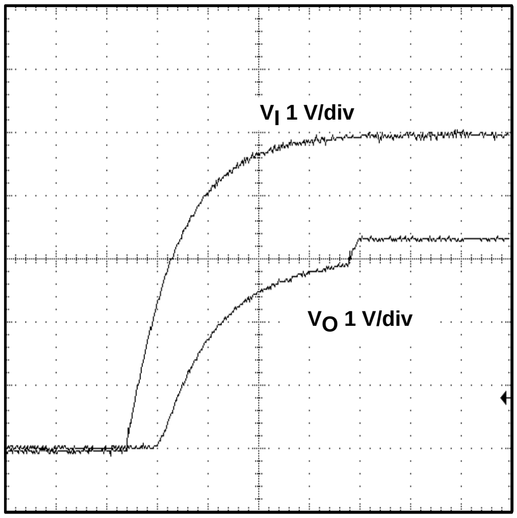


Figure 2–22. Measured Start-Up Waveform, TPS54873 With Precharge and No Load



Time Scale – 5 µs/div

Chapter 3

Board Layout

This chapter provides a description of the TPS54x73EVM-225 board layout and layer illustrations.

Topic **Page**

3.1 Layout

The board layout for the TPS54x73EVM-225 is shown in Figure 3–1 through Figure 3–6. The top-side layer of the TPS54x73EVM-225 is laid out in a manner typical of a user application. The bottom layer of the TPS54x73EVM-225 is designed to accommodate an optional alternate output filter configuration. The top and bottom layers are 1.5 oz. copper, while the two internal layers are 0.5 oz. copper.

The top layer contains the main power traces for V_I, V_O, and $V_{(phase)}$. Also on the top layer are connections for the remaining pins of the TPS54x73 and a large area filled with ground. The two internal layers are identical and are dedicated ground planes. The bottom layer contains pads for an optional alternate output filter, including space for three D3 or D4 case size electrolytic capacitors and an alternate inductor of 0.5 in. x 0.5 in. size ground traces. The top and bottom ground traces are connected to the internal ground planes with multiple vias placed around the board including 12 directly under the TPS54x73 device to provide a thermal path from the PowerPAD™ land to ground.

The input-decoupling capacitors (C10 and C12), bias-decoupling capacitor (C3), and boot-strap capacitor (C9) are all located as close to the IC as possible. In addition, the compensation components are also kept close to the IC. The compensation circuit ties to the output voltage at the point of regulation, adjacent to the high frequency bypass output capacitor.

Figure 3–1. Top-Side Layout

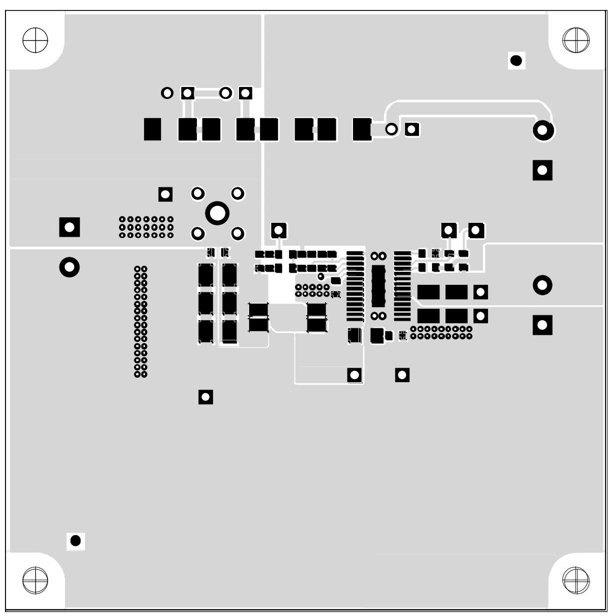


Figure 3–2. Internal Layer 1 Layout

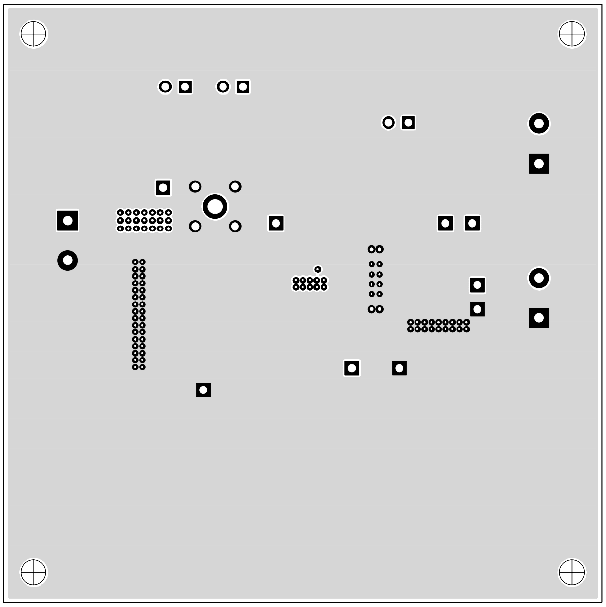


Figure 3–3. Internal Layer 2 Layout

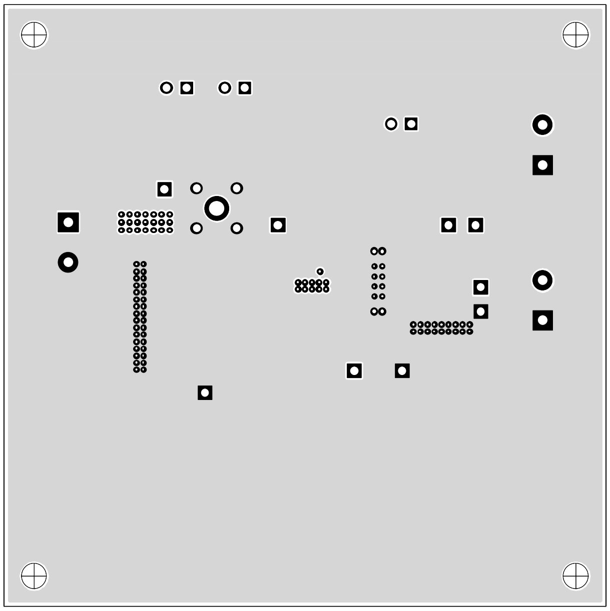


Figure 3–4. Bottom Side Layout (Looking From Top Side)

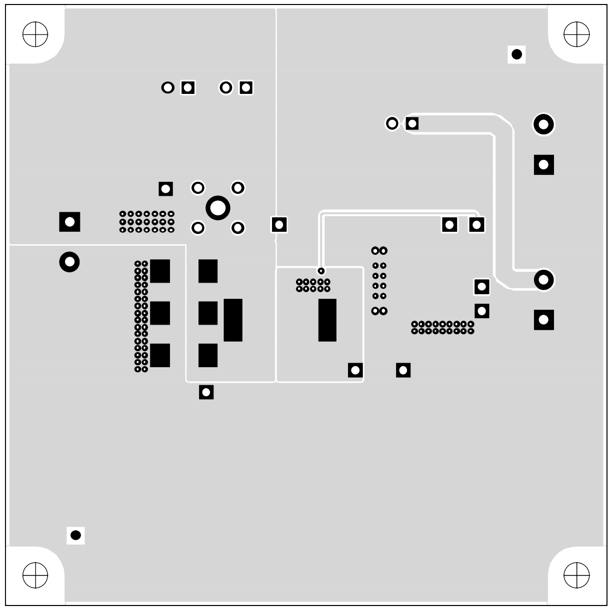


Figure 3–5. Top Side Assembly

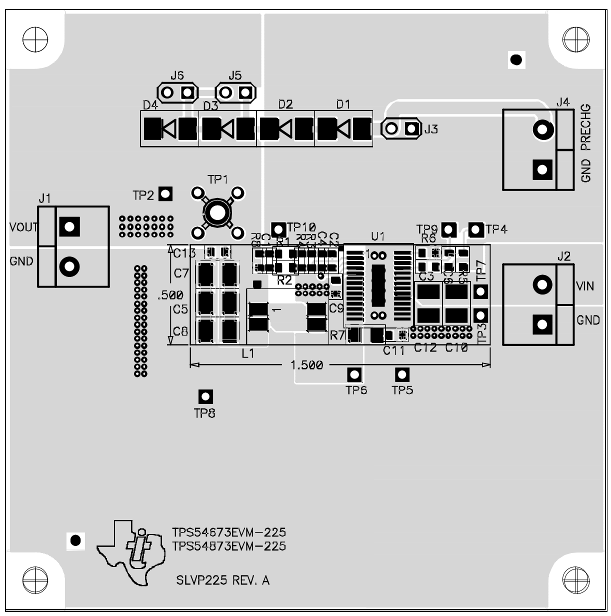
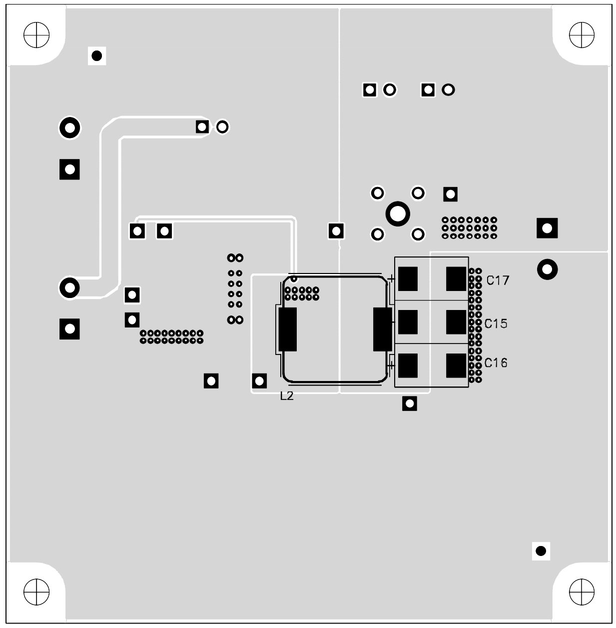


Figure 3–6. Bottom Side Assembly (Showing Optional Components)



Chapter 4

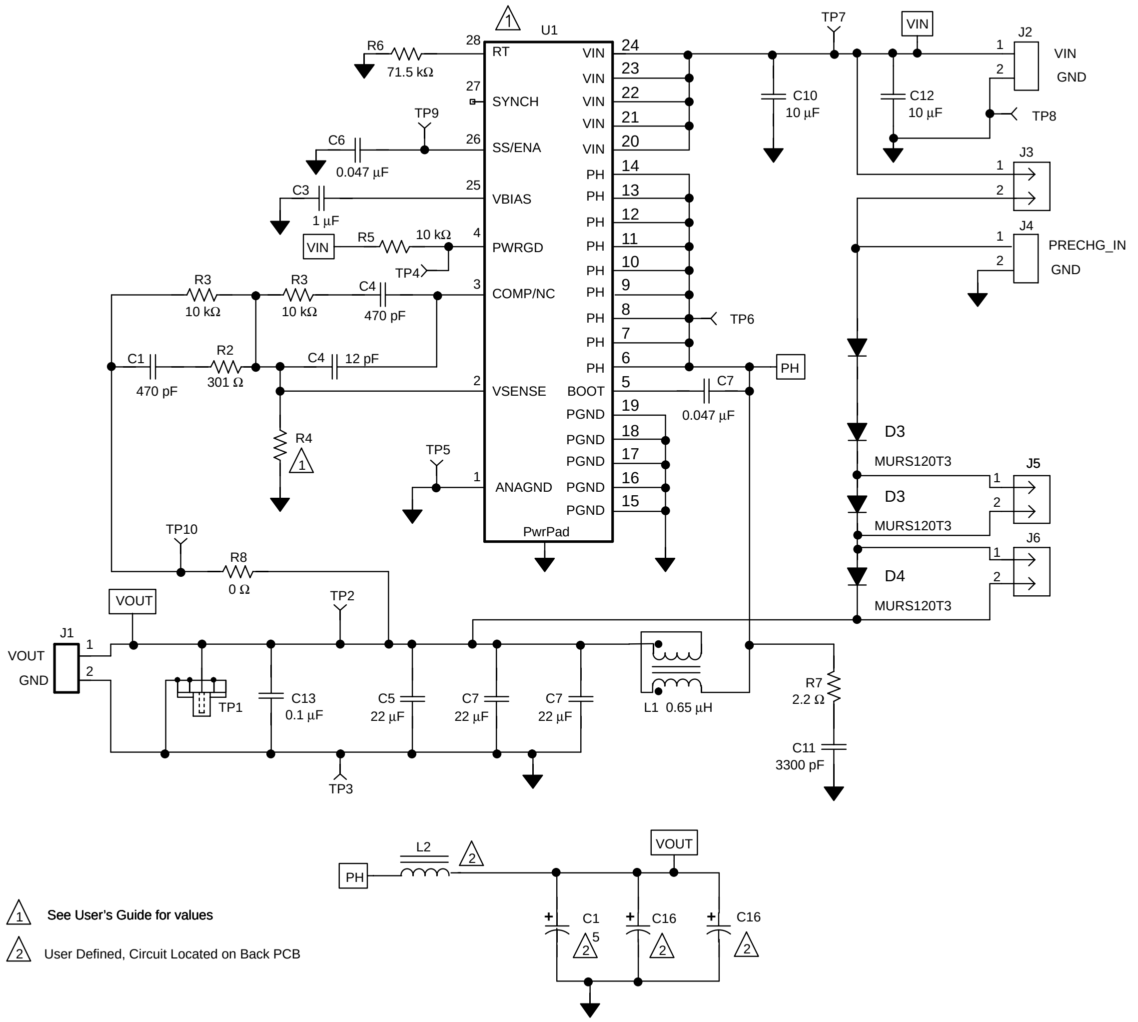
Schematic and Bill of Materials

The TPS54x73EVM-225 schematic and bill of materials are presented in this chapter.

Topic **Page**

4.1 Schematic

Figure 4–1. TPS54x73EVM-225 Schematic



4.2 Bill of Materials

Table 4–1. TPS54x73EVM-225 Bill of Materials

Count						
–1	–2	RefDes	Description	Size	MFR	Part Number
2	2	C1, C4	Capacitor, ceramic, 470 pF, 50 V, C0G, 5%	603	Panasonic	GRM1885C1H471JA01
2	2	C10, C12	Capacitor, ceramic, 10 µF, 10 V, X5R, 20%	1210	Taiyo Yuden	LMK325BJ106MN
1	1	C11	Capacitor, ceramic, 3300 pF, 50 V, X7R 10 %	603	Panasonic	ECJ–1VB1H332K
1	1	C13	Capacitor, ceramic, 0.1 µF, 25 V, X7R, 10%	603	Murata	GMR188R71E104KA01
–	–	C15, C16, C17	Open	7343 (D)		
1	1	C2	Capacitor, ceramic, 12 pF, 50 V, C0G, 5%	603	Murata	GRM1885C1H120JZ01
1	1	C3	Capacitor, ceramic, 1 µF, 10 V, X5R, 10%	603	TDK	C1608X5R1A105M
3	3	C5, C7, C8	Capacitor, ceramic, 22 µF, 6.3 V, X5R, 20%	1210	Taiyo Yuden	JMK325BJ226MN
2	2	C6, C9	Capacitor, ceramic, 0.047 µF, 25 V, X7R, 10%	603	Murata	GRM188R71E473KA01
4	4	D1, D2, D3, D4	Diode, ultra fast rectifier, 1 A, 200 V	SMB	On Semiconductor	MURS120T3
3	3	J1, J2, J4	Terminal block, 2 pin, 15 A, 5,1 mm	148830	OST	ED1609
3	3	J3, J5, J6	Header, 2 pin, 100 mil spacing, (36-pin strip)	0.100×2	Sullins	PTC36SAAN
1	1	L1	Inductor, 0.65 µH, 12 A	0.340×0.250	Pulse	PA0277
–	–	L2	Open	0.51 × 0.51		
4	4	R1, R2, R6, R7	Resistor, chip, 10.0 kΩ, 1/16–W, 1%	603	Std	Std
3	3	R1, R3, R5	Resistor, chip, 10 kΩ, 1/16 W, 1%	603	Std	Std
1	1	R2	Resistor, chip, 301 Ω, 1/16 W, 1%	603	Std	Std
1		R4	Resistor, chip, 5.49 kΩ, 1/16 W, 1%	603	Std	Std
	1	R4	Resistor, chip, 3.74 kΩ, 1/16 W, 1%	603	Std	Std
1	1	R6	Resistor, chip, 71.5 kΩ, 1/16 W, 1%	603	Std	Std
1	1	R7	Resistor, chip,2.2 Ω, 1/16 W, 1%	603	Std	ERJ-8RQF2R2
1	1	R8	Resistor, chip,0 Ω, 1/15 W, 1%	603	Std	Std
1	1	TP1	Adapter, 3,5 mm probe clip (or 131-5031-00)	72900	Tektronic	131-4244-00
6	6	TP2, TP4, TP6, TP7, TP9, TP10	Test point, red, 1 mm	0.038”	Farnell	240–345
3	3	TP3, TP5, TP8	Test point, black, 1 mm	0.038”	Farnell	240-333
1	–	U1	IC, SWIFT dc/dc converter, 3 V to 6 V, 6 A	PWP28	TI	TPS54673PWP
–	1	U1	IC, SWIFT dc/dc converter, 3 V to 6 V, 6 A	PWP28	TI	TPS54873PWP

Table 4–1. TPS54x73EVM-225 Bill of Materials (Continued)

Count		RefDes	Description	Size	MFR	Part Number
–1	–2					
1	1	–	PCB, 3 in. × 3 in. × 0.062 in.		Any	SLVP225
3	3	–	Shunt, 100 mil, black	0.100	3M	929950-00