



HEF4541B

Programmable timer

Rev. 7 — 15 August 2024

Product data sheet

1. General description

The HEF4541B is a programmable timer. It consists of a 16-stage binary counter, an integrated oscillator to be used with external timing components, an automatic power-on reset and output control logic. The external components R_{TC} and C_{TC} determines the frequency of the oscillator within the frequency range 1 Hz to 100 kHz. An external clock signal at input RS can replace the oscillator. The timer advances on the positive-going transition of RS. A LOW on the auto reset input (AR) and a LOW on the master reset input (MR) enables the internal power-on reset. A HIGH level at input MR resets the counter independent on all other inputs. Resetting, disables the oscillator to provide no active power dissipation.

A HIGH at input AR turns off the power-on reset to provide a low quiescent power dissipation of the timer. The 16-stage counter divides the oscillator frequency by 2^8 , 2^{10} , 2^{13} or 2^{16} depending on the state of the address inputs (A0, A1). The divided oscillator frequency is available at output O. The phase input (PH) features a complementary output signal. When the mode select input (MODE) is LOW the timer is a single transition timer and when HIGH the timer is a 2^n frequency divider.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

2. Features and benefits

- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Complies with JEDEC standard JESD 13-B
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
HEF4541BT	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

4. Functional diagram

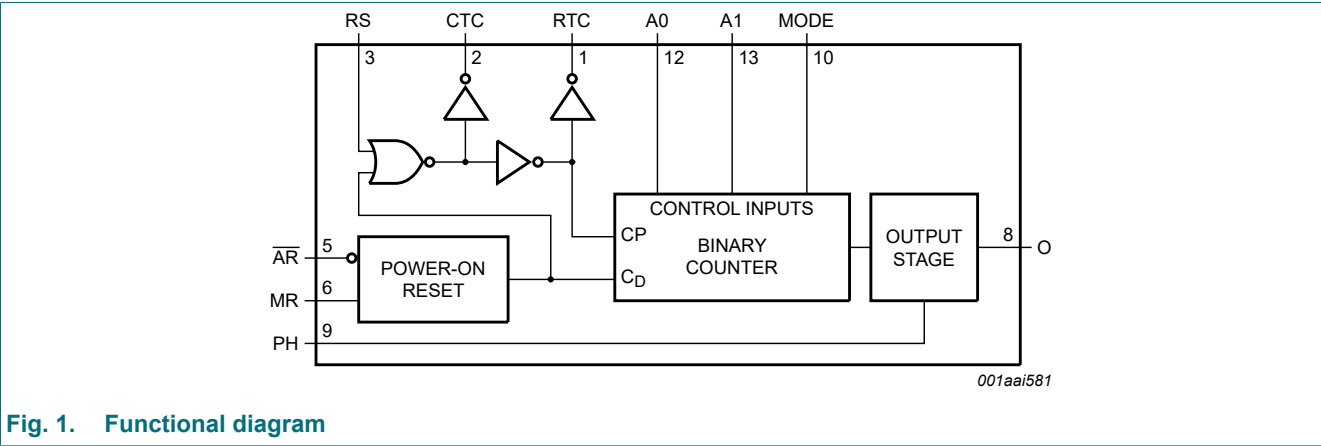


Fig. 1. Functional diagram

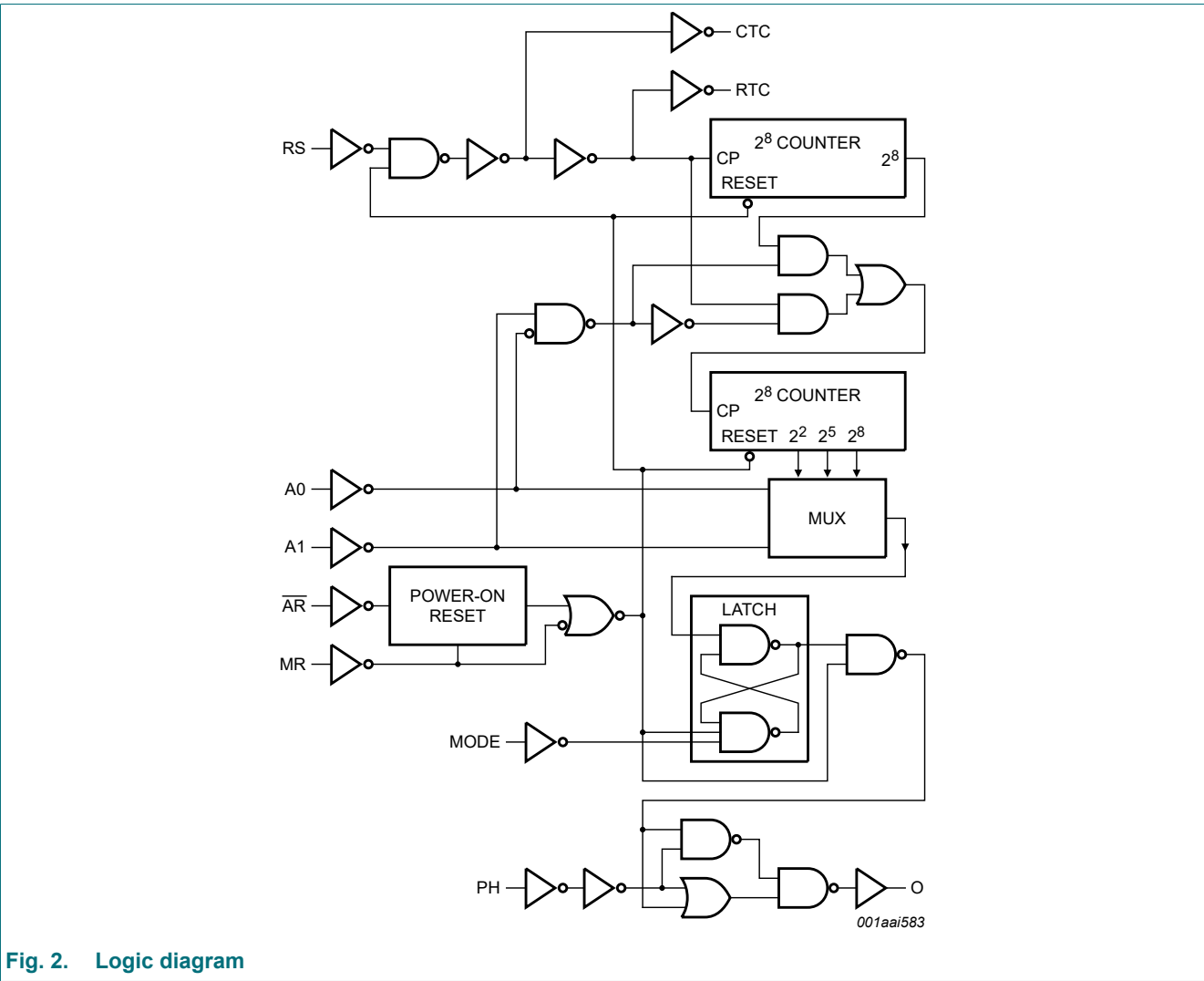
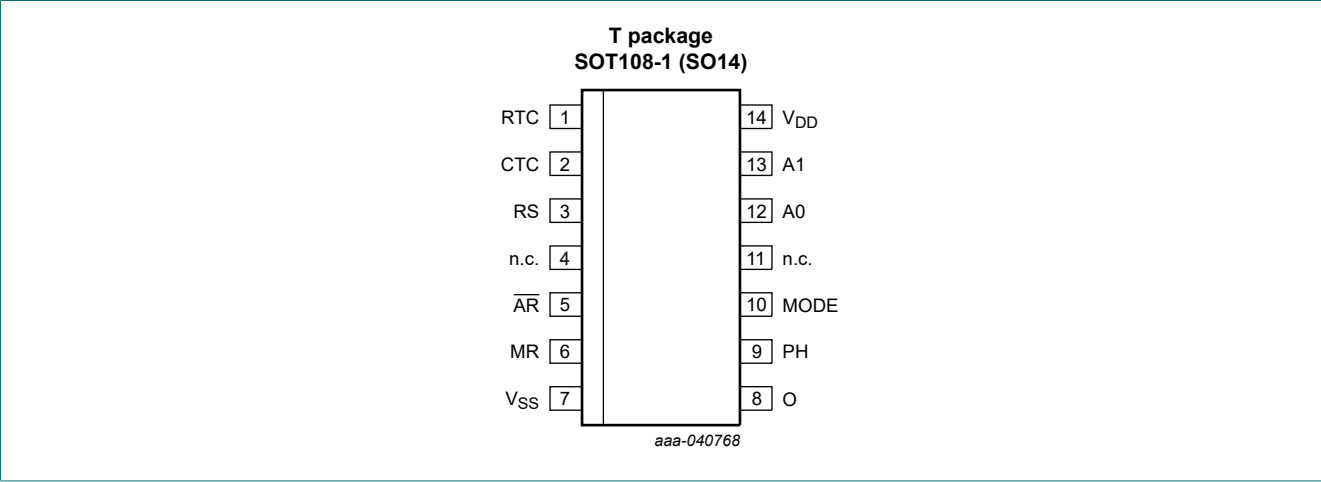


Fig. 2. Logic diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
RTC	1	external resistor connection
CTC	2	external capacitor connection
RS	3	external resistor connection (RS) or external clock input
n.c.	4, 11	not connected
AR	5	auto reset input (active low)
MR	6	master reset input
V _{SS}	7	ground (0 V)
O	8	timer output
PH	9	phase input
MODE	10	mode select input
A0, A1	12, 13	address inputs
V _{DD}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input				MODE
AR	MR	PH	MODE	
H	L	X	X	auto reset disabled
L	L	X	X	auto reset enabled[1]
X	H	X	X	master reset active
X	L	X	H	normal operation selected division to output
X	L	X	L	single-cycle mode[2]
X	L	L	X	output initially LOW after reset
X	L	H	X	output initially HIGH, after reset

- [1] For correct power-on reset, the supply voltage should be above 8.5 V. For $V_{DD} < 8.5\text{ V}$, disable the auto reset and connect $\overline{AR}$ to V_{DD} .
- [2] The timer is initialized on a reset pulse and the output changes state after 2^{n-1} counts and remains in that state (latched). A master reset or a LOW to HIGH transition on the MODE input, resets this latch.

Table 4. Frequency selection table

A0	A1	Number of counter stages n	$\frac{f_{OSC}}{f_O} = 2^n$
L	L	13	8192
L	H	10	1024
H	L	8	256
H	H	16	65536

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{DD} + 0.5\text{ V}$	-	±10	mA
V_I	input voltage		-0.5	$V_{DD} + 0.5$	V
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{DD} + 0.5\text{ V}$	-	±10	mA
$I_{I/O}$	input/output current	O output	-	±10	mA
T_{stg}	storage temperature		-65	+150	°C
T_{amb}	ambient temperature		-40	+125	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C to }+125\text{ °C}$ [1]	-	500	mW
P	power dissipation		-	100	mW

- [1] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.

8. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD}	supply voltage		3	15	V
V _I	input voltage		0	V _{DD}	V
T _{amb}	ambient temperature	in free air	-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{DD} = 5 V	-	3.75	μs/V
		V _{DD} = 10 V	-	0.5	μs/V
		V _{DD} = 15 V	-	0.08	μs/V

9. Static characteristics

Table 7. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD}; unless otherwise specified.

Symbol	Parameter	Conditions	V _{DD}	T _{amb} = -40 °C		T _{amb} = 25 °C		T _{amb} = 85 °C		T _{amb} = 125 °C		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level input voltage	I _O < 1 μA	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
V _{IL}	LOW-level input voltage	I _O < 1 μA	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V
V _{OH}	HIGH-level output voltage	I _O < 1 μA	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V
V _{OL}	LOW-level output voltage	I _O < 1 μA	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V
I _{OH}	HIGH-level output current	CTC, RTC;										
		V _O = 2.5 V	5 V	-	-1.4	-	-1.2	-	-0.95	-	-0.95	mA
		V _O = 4.6 V	5 V	-	-0.5	-	-0.4	-	-0.3	-	-0.3	mA
		V _O = 9.5 V	10 V	-	-1.4	-	-1.2	-	-0.95	-	-0.95	mA
		V _O = 13.5 V	15 V	-	-4.8	-	-4.0	-	-3.2	-	-3.2	mA
		O;										
		V _O = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	-	-1.1	mA
		V _O = 4.6 V	5 V	-	-0.64	-	-0.5	-	-0.36	-	-0.36	mA
		V _O = 9.5 V	10 V	-	-1.6	-	-1.3	-	-0.9	-	-0.9	mA
		V _O = 13.5 V	15 V	-	-4.2	-	-3.4	-	-2.4	-	-2.4	mA

Symbol	Parameter	Conditions	V _{DD}	T _{amb} = -40 °C		T _{amb} = 25 °C		T _{amb} = 85 °C		T _{amb} = 125 °C		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
I _{OL}	LOW-level output current	CTC, RTC;										
		V _O = 0.4 V	5 V	0.33	-	0.27	-	0.20	-	0.20	-	mA
		V _O = 0.5 V	10 V	1.0	-	0.85	-	0.68	-	0.68	-	mA
		V _O = 1.5 V	15 V	3.2	-	2.7	-	2.3	-	2.3	-	mA
		O;										
		V _O = 0.4 V	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
		V _O = 0.5 V	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		V _O = 1.5 V	15 V	4.2	-	3.2	-	2.4	-	2.4	-	mA
I _I	input leakage current		15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	µA
I _{DD}	supply current	I _O = 0 A	5 V	-	5	-	5	-	150	-	150	µA
			10 V	-	10	-	10	-	300	-	300	µA
			15 V	-	20	-	20	-	600	-	600	µA
C _I	input capacitance		-	-	-	-	7.5	-	-	-	-	pF

Table 8. Reset characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD}; see Table 12 for test conditions; unless otherwise specified.

Symbol	Parameter	Conditions	V _{DD}	T _{amb} = -40 °C		T _{amb} = +25 °C			T _{amb} = +85 °C		T _{amb} = +125 °C		Unit
				Min	Max	Min	Typ	Max	Min	Max	Min	Max	
I _{DD}	supply current	supply current for power-on reset enable; AR = MR = 0 V; other inputs at 0 V or V _{DD}	5 V	-	80	-	20	80	-	230	-	230	µA
			10 V	-	750	-	250	600	-	700	-	700	µA
			15 V	-	1.6	-	0.5	1.3	-	1.5	-	1.5	mA
V _{DD}	supply voltage	supply voltage for automatic reset initialization; AR = MR = 0 V; other inputs at 0 V or V _{DD}	-	-	-	8.5	5	-	-	-	-	-	V

10. Dynamic characteristics

Table 9. Dynamic characteristics

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified. For test circuit, see Fig. 4.

Symbol	Parameter	Conditions	V _{DD}	Extrapolation formula	Min	Typ[1]	Max	Unit
t _{pd}	propagation delay	RS to O; 2 ⁸ selected; see Fig. 3	5 V	[2] 348 ns + (0.55 ns/pF)C _L	-	375	750	ns
			10 V	139 ns + (0.23 ns/pF)C _L	-	150	300	ns
			15 V	102 ns + (0.16 ns/pF)C _L	-	110	220	ns
		RS to O; 2 ¹⁰ selected; see Fig. 3	5 V	398 ns + (0.55 ns/pF)C _L	-	425	850	ns
			10 V	154 ns + (0.23 ns/pF)C _L	-	165	330	ns
			15 V	112 ns + (0.16 ns/pF)C _L	-	120	240	ns
		RS to O; 2 ¹³ selected; see Fig. 3	5 V	483 ns + (0.55 ns/pF)C _L	-	510	1020	ns
			10 V	179 ns + (0.23 ns/pF)C _L	-	190	380	ns
			15 V	127 ns + (0.16 ns/pF)C _L	-	135	270	ns
		RS to O; 2 ¹⁶ selected; see Fig. 3	5 V	548 ns + (0.55 ns/pF)C _L	-	575	1150	ns
			10 V	199 ns + (0.23 ns/pF)C _L	-	210	420	ns
			15 V	142 ns + (0.16 ns/pF)C _L	-	150	300	ns
t _W	pulse width	RS LOW; MR HIGH; see Fig. 3	5 V	[3]	60	30	-	ns
			10 V		30	15	-	ns
			15 V		24	12	-	ns
f _{clk(max)}	maximum clock frequency	RS; see Fig. 3	5 V		8	16	-	MHz
			10 V		15	30	-	MHz
			15 V		18	36	-	MHz
f _{osc}	oscillator frequency	R _t = 5 kΩ; C _t = 1 nF; R _S = 10 kΩ; see Fig. 5	5 V		-	90	-	kHz
			10 V		-	90	-	kHz
			15 V		-	90	-	kHz
		R _t = 56 kΩ; C _t = 1 nF; R _S = 120 kΩ; see Fig. 5	5 V		-	8	-	kHz
			10 V		-	8	-	kHz
			15 V		-	8	-	kHz

- [1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).
- [2] t_{pd} is the same as t_{PHL} and t_{PLH}.
- [3] t_W is the same as t_{VL(min)} and t_{WH(min)}.

Table 10. Dynamic power dissipation

P_D can be calculated from the formulas shown. $V_{SS} = 0\text{ V}$; $t_r = t_f \leq 20\text{ ns}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Symbol	Parameter	V _{DD}	Typical formula[1]
P _D	dynamic power dissipation	Per package	
		5 V	P _D = 1300 × f _i + (f _o × C _L × V _{DD} ²) μW
		10 V	P _D = 5300 × f _i + (f _o × C _L × V _{DD} ²) μW
		15 V	P _D = 12000 × f _i + (f _o × C _L × V _{DD} ²) μW
		Total, using the on-chip oscillator	
		5 V	P _D = 1300 × f _{osc} + f _o C _L V _{DD} ² + 2C _{TC} V _{DD} ² f _{osc} + 10V _{DD} μW
		10 V	P _D = 5300 × f _{osc} + f _o C _L V _{DD} ² + 2C _{TC} V _{DD} ² f _{osc} + 100V _{DD} μW
		15 V	P _D = 12000 × f _{osc} + f _o C _L V _{DD} ² + 2C _{TC} V _{DD} ² f _{osc} + 400V _{DD} μW

- [1] f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF; V_{DD} = supply voltage in V;
f_{osc} = oscillator frequency in MHz; C_{TC} = timing capacitance in pF.

10.1. Waveforms and test circuit

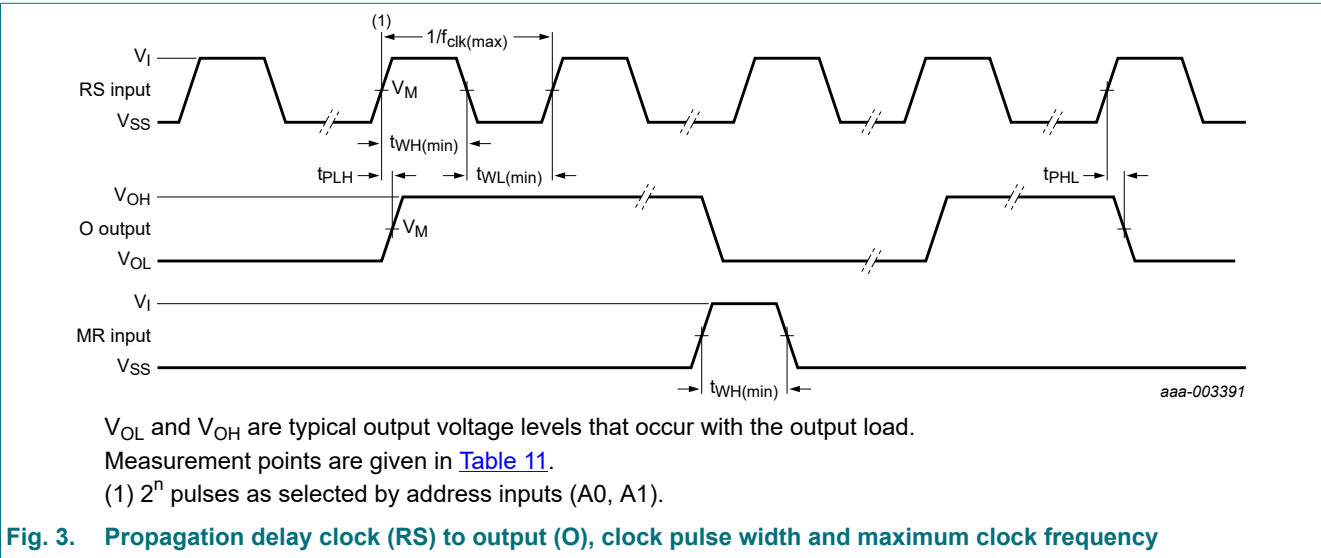


Table 11. Measurement points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$

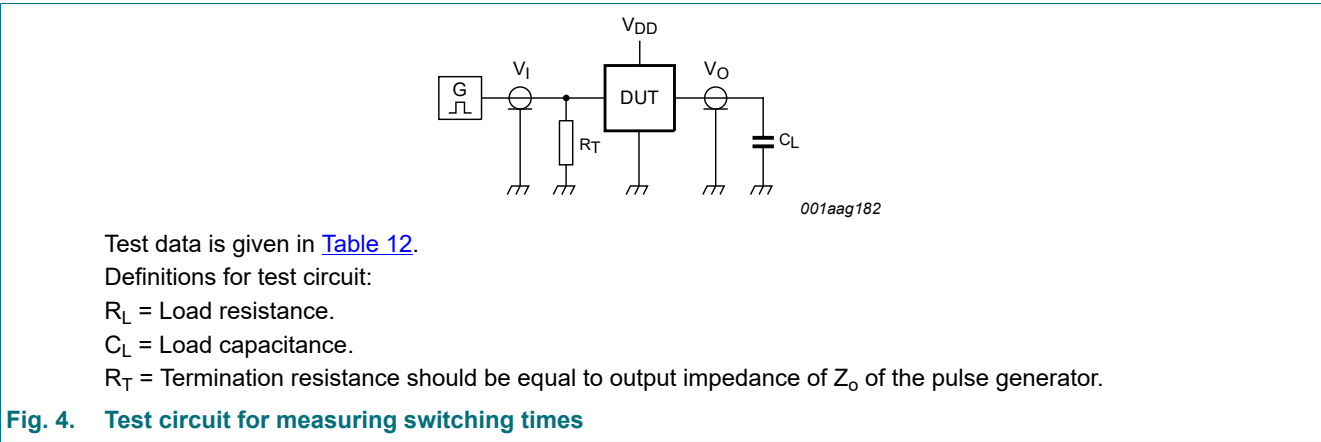


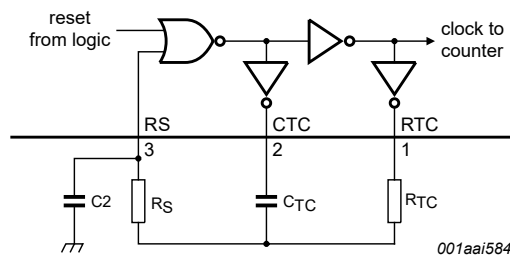
Table 12. Test data

Supply	Input		Load
V_{DD}	V_I	t_r, t_f	C_L
5 V to 15 V	V_{SS} or V_{DD}	≤ 20 ns	50 pF

11. Application information

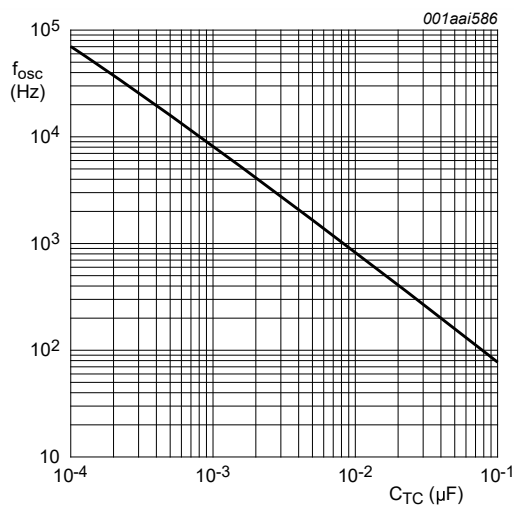
RC oscillator timing component limitations

$R_{TC}C_{TC}$ determines the oscillator frequency, provided $R_{TC} \ll R_S$ and $R_S C_2 \ll R_{TC}C_{TC}$. The function of R_S is to minimize the influence of the forward voltage across the input protection diodes on the frequency. The stray capacitance C_2 should be kept as small as possible. In consideration of accuracy, C_{TC} must be larger than the inherent stray capacitance. R_{TC} must be larger than the LOCMOS 'ON' resistance in series with it, which typically is 500 Ω at $V_{DD} = 5$ V, 300 Ω at $V_{DD} = 10$ V and 200 Ω at $V_{DD} = 15$ V. The recommended values for these components to maintain agreement with the typical oscillation formula are: $C_{TC} \geq 100$ pF, up to any typical value, 10 k $\Omega \leq R_{TC} \leq 1$ M Ω .

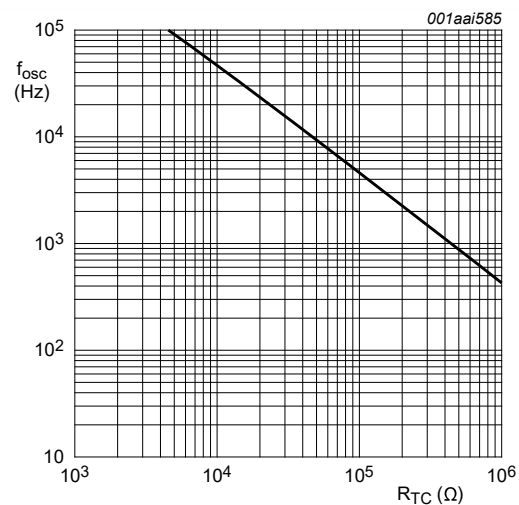


Typical formula for oscillator frequency: $f_{osc} = \frac{1}{2.3 \times R_{TC} \times C_{TC}}$

Fig. 5. External component connection for RC oscillator; $R_S \approx R_{TC}$

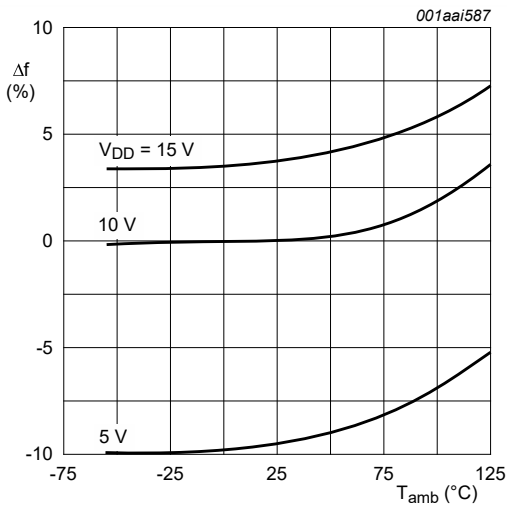


a. C_{TC} curve at $R_{TC} = 56$ k Ω ; $R_S = 120$ k Ω .

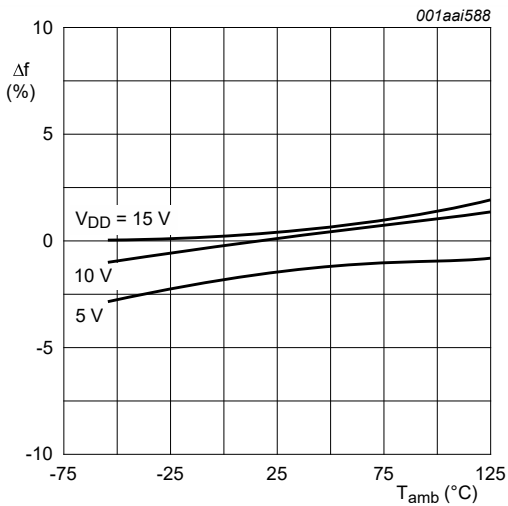


b. R_{TC} curve at $C_{TC} = 1$ nF; $R_S = 2 R_{TC}$.

Fig. 6. RC oscillator frequency as a function of R_{TC} and C_{TC} at $V_{DD} = 5$ V to 15 V; $T_{amb} = 25$ °C



a. $R_{TC} = 56\text{ k}\Omega$; $C_{TC} = 1\text{ nF}$; $R_S = 0\text{ }\Omega$.



b. $R_{TC} = 56\text{ k}\Omega$; $C_{TC} = 1\text{ nF}$; $R_S = 120\text{ k}\Omega$.

Fig. 7. Frequency deviation (Δf) as a function of ambient temperature

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

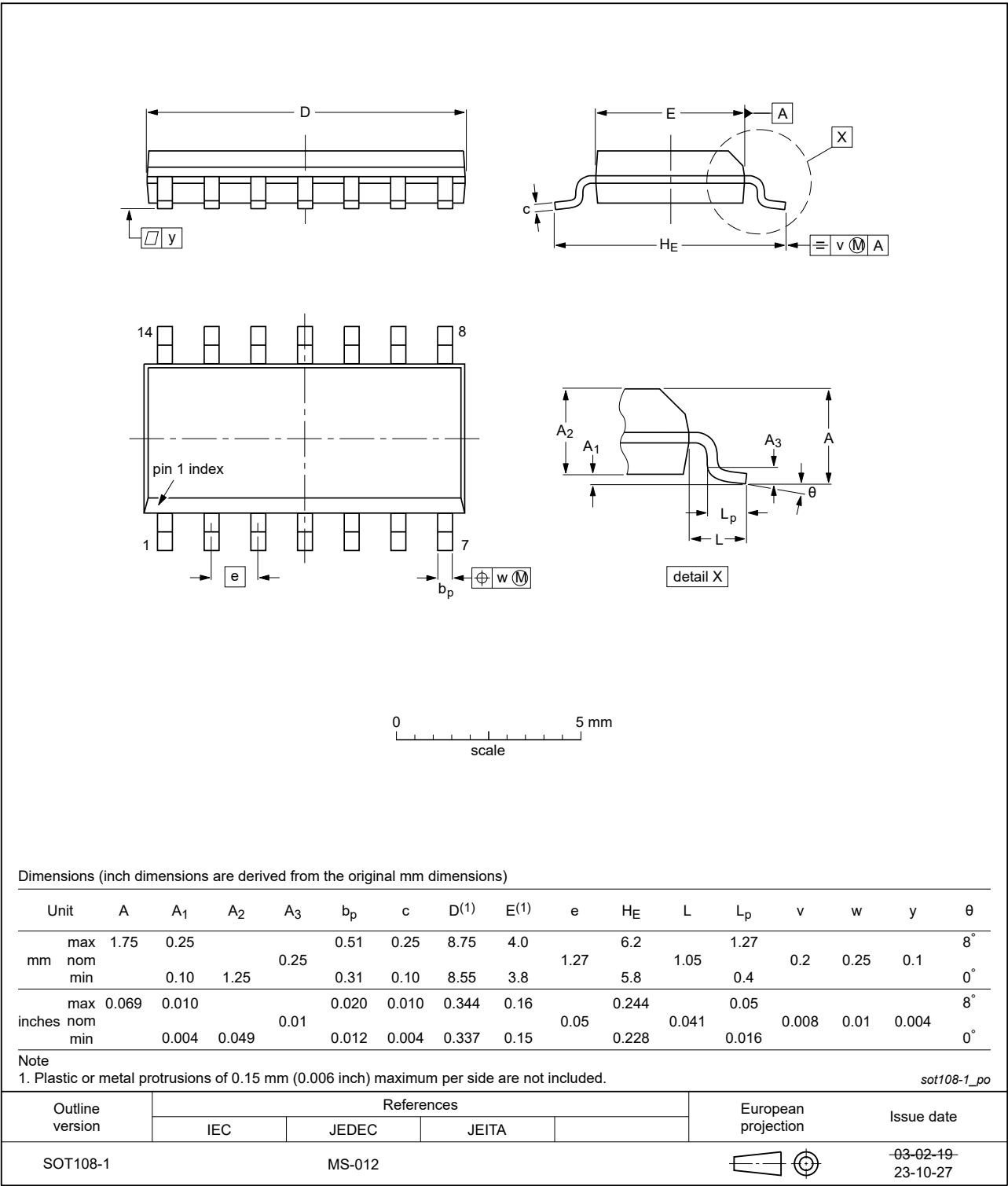


Fig. 8. Package outline SOT108-1 (SO14)

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4541B v.7	20240815	Product data sheet	-	HEF4541B v.6
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard. • Fig. 8: Aligned SO package outline drawing to JEDEC MS-012			
HEF4541B v.6	20211125	Product data sheet	-	HEF4541B v.5
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Maximum temperature changed to 125 °C throughout the data sheet. • Section 2 updated. • Section 7: Derating values for P_{tot} total power dissipation have been updated.			
HEF4541B v.5	20151215	Product data sheet	-	HEF4541B v.4
Modifications:	• Type number HEF4541BP (SOT27-1) removed.			
HEF4541B v.4	20120625	Product data sheet	-	HEF4541B_CNV v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 2 added.			
HEF4541B_CNV v.3	19950101	Product specification	-	HEF4541B_CNV v.2
HEF4541B_CNV v.2	19950101	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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Date of release: 15 August 2024