HS-26CT32RH-T

Radiation HardenedQuad Differential Line Receiver

FN4593
Rev 1.00
July 1999

Intersil's Satellite Applications Flow™ (SAF) devices are fully tested and guaranteed to 100kRAD total dose. These QML Class T devices are processed to a standard flow intended to meet the cost and shorter lead-time needs of large volume satellite manufacturers, while maintaining a high level of reliability.

The Intersil HS-26CT32RH-T is a Quad Differential Line Receiver designed for digital data transmission over balanced lines and meets the requirements of EIA Standard RS-422. Radiation Hardened CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments.

The HS-26CT32RH-T has an input sensitivity of 200mV (typ.) over the common mode input voltage range of ±7V. The receivers are also equipped with input fail safe circuitry, which causes the outputs to go to a logic "1" when the inputs are open. TTL compatible Enable and Disable functions are common to all four receivers.

Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

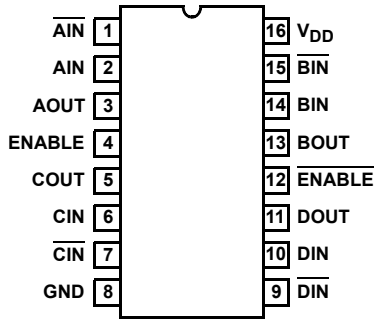
Detailed Electrical Specifications for the HS-26CT32RH-T are contained in SMD 5962-95631. A "hot-link" is provided from our website for downloading.

Intersil's Quality Management Plan (QM Plan), listing all Class T screening operations, is also available on our website.

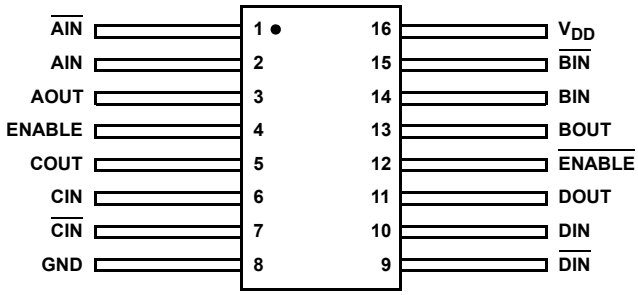
- QML Class T, Per MIL-PRF-38535
- Radiation Performance
  - Gamma Dose . . . . . 1×10^5 RAD(Si)
  - SEU and SEL . . . . . Immune to 100MeV/mg/cm^2
- EIA RS-422 Compatible Inputs
- TTL Compatible Enable Inputs
- Input Fail Safe Circuitry
- High Impedance Inputs when Disabled or Powered Down
- Low Power Dissipation 138mW Standby (Max)
- Single 5V Supply
- Full -55^{o}C to 125^{o}C Military Temperature Range

Pinouts

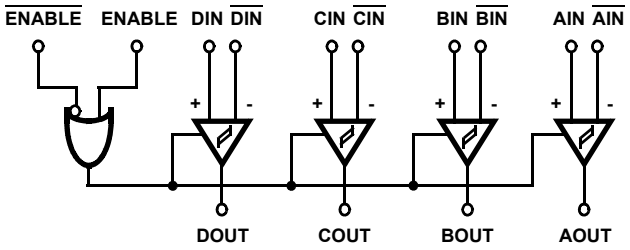
HS1-26CT32RH-T (SBDIP) CDIP2-T16
TOP VIEW



HS9-26CT32RH-T (FLATPACK), CDFP4-F16
TOP VIEW



Functional Diagram



TRUTH TABLE

DEVICE POWER ON/OFF	INPUTS			OUTPUT
	ENABLE	$\overline{\text{ENABLE}}$	INPUT	OUT
ON	0	1	X	HI-Z
ON	1	X	VID ≥ VTH (Max)	1
ON	1	X	VID ≤ VTH (Min)	0
ON	X	0	VID ≥ VTH (Max)	1
ON	X	0	VID ≤ VTH (Min)	0
ON	1	X	Open	1
ON	X	0	Open	1

Die Characteristics

DIE DIMENSIONS:

2140µm x 3290µm x 533µm ±25.4µm

(85 x 130 x 21mils ±1mil)

METALLIZATION:

M1: Mo/Tiw

Thickness: 5800Å

M2: Al/Si/Cu

Thickness: 10kÅ ±1kÅ

SUBSTRATE POTENTIAL:

Internally connected to V_{DD}. May be left floating.

BACKSIDE FINISH:

Silicon

PASSIVATION:

Type: SiO_2

Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

< 2.0e5 A/cm^2

TRANSISTOR COUNT:

315

PROCESS:

Radiation Hardened CMOS, AVLSI

Metallization Mask Layout

HS-26CT32RH-T