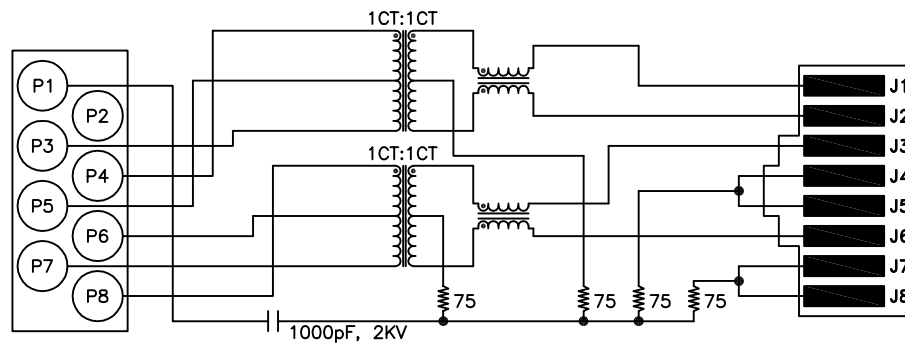




NOTES:

- 1.0 PINS WITHOUT ELECTRICAL CONNECTION ARE OMITTED.
- 2.0 ALL RESISTORES ARE $\pm 5\%$ TOLERANCE.

ELECTRICAL SPECIFICATIONS:

- 1.0 TURNS RATIO: (P8-P6-P7) : (J3-J6) : 1CT : 1CT $\pm 3\%$
(P4-P5-P3) : (J1-J2) : 1CT : 1CT $\pm 3\%$
- 2.0 INDUCTANCE: (P7-P8) : 350uH MIN. @ 0.1V, 100KHz, 8mA DC Bias
(P4-P3) : 350uH MIN. @ 0.1V, 100KHz, 8mA DC Bias
- 3.0 LEAKAGE INDUCTANCE: P7-P8 (WITH J6 AND J3 SHORT) : 0.3uH MAX. @ 1MHz
P4-P3 (WITH J2 AND J1 SHORT) : 0.3uH MAX. @ 1MHz
- 4.0 INTERWINDING CAPACITANCE: (P8,P6,P7) TO (J6,J3) : 25pf TYP @ 1MHz
(P4,P5,P3) TO (J2,J1) : 25pf TYP @ 1MHz
- 5.0 DC RESISTANCE: (J6-J3)=(J2-J1) : 1.2 ohms Max.
- 6.0 RETURN LOSS: (P7-P8)=100 OHMS AND (P4-P3)=100 OHM REF.
1MHz TO 30MHz : -18dB MIN.
30MHz TO 60MHz : -(19-20 LOG (f/30MHz))
60MHz TO 80MHz : -12dB MIN.
NOTE: 100 OHMS CONNECTED TO (J2-J1) OR (J6-J3).
- 7.0 DIELECTRIC WITHSTAND: (J1, J2) TO (P7, P8) : 1500 VAC
(J3, J6) TO (P4, P3) : 1500 VAC
- 8.0 INSERTION LOSS: RS=RL=100 ohms
1-65MHz : -1 dB MAX
- 9.0 RISE TIME: RISE TIME: RS=100 OHMS AND RL = 100 OHMS
OUTPUT VOLTAGE = 1 V peak : 3.0 nS MAX
PULSE WIDTH= 112nS : 3.0 nS MAX
- 10.0 CROSS TALK: 1-100 MHz : -35 dB TYP
- 11.0 COMMON TO COMMON MODE ATTENUATION: 30MHz TO 100MHz : -35 dB TYP

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SHEET
1 OF 3

DRAWING NO.

SI-50102

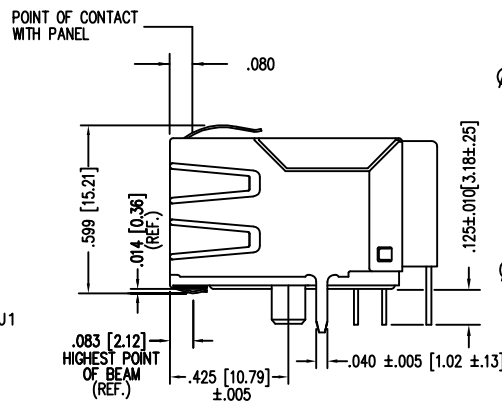
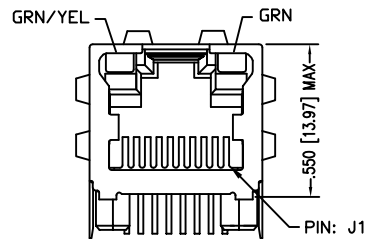
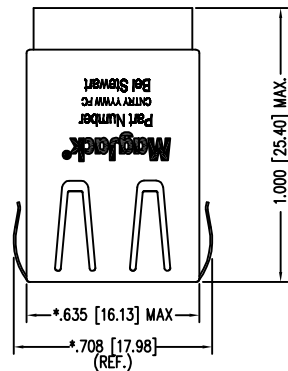
REV.
01

STANDARD LED	WAVELENGTH	* Forward V (MAX)	(TYP)
YELLOW	590 nm	2.5 V	2.1 V
GREEN	565 nm	2.5 V	2.2 V
GREEN 5V	565 nm		6 V

* WITH A FORWARD CURRENT OF 20 mA

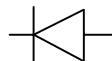
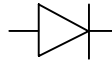
NOTES:

- TOLERANCES COMPLY WITH F.C.C. DIMENSION REQUIREMENTS
- DIMENSIONS SHOWN WITH "*" TO BE CENTRAL ABOUT CENTER LINE
- DIMENSIONS SHOWN ARE SUBJECT TO CHANGE WITHOUT NOTICE.
- PIN NOT ELECTRICALLY CONNECTED MAYBE OMITTED. SEE ELECTRICAL DRAWING FOR OMITTED PINS.
- STANDARD 50 MICRO-INCH SELECTIVE GOLD PLATING
- REFLOW COMPATIBLE - 230°C/90 SEC.
- ALL POLYMERS FLAMMABILITY - UL94V0



BICOLOR LED POLARITY

GRN



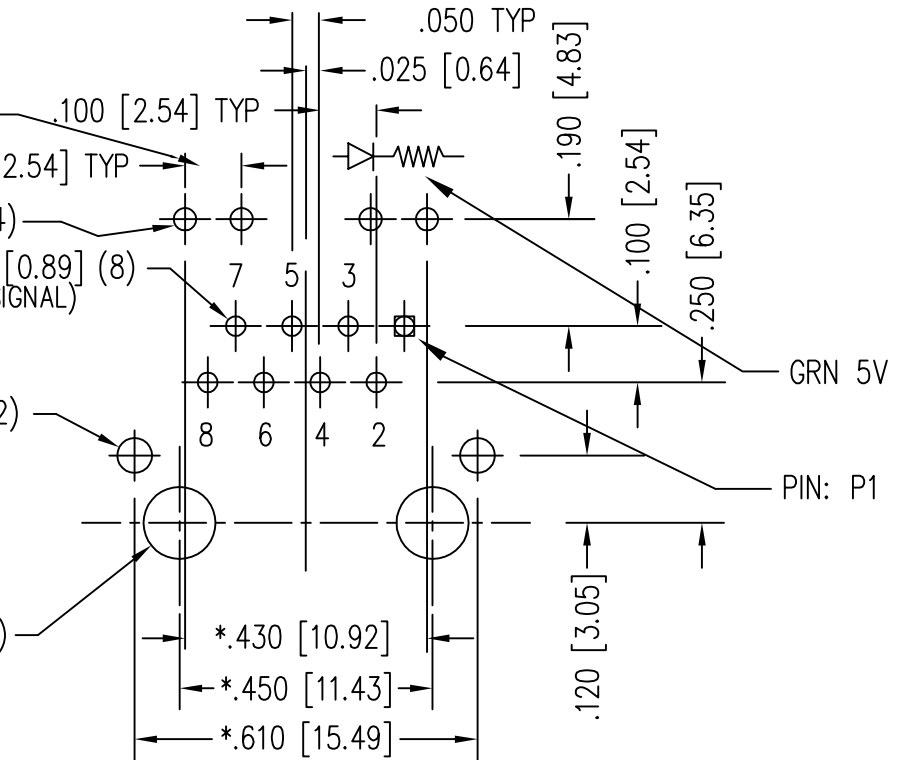
YEL

BICOLOR GRN/YEL LED

∅.040 [1.02] (4)
∅.035 [0.89] (8)
(SIGNAL)

∅.062 [1.57] (2)
(SHIELD)

∅ .128 [3.25]
.125 [3.18] (2) (POSTS)



P.C.B. RECOMMENDED HOLE LAYOUT
SEEN FROM COMPONENT SIDE
TOLERANCE ±.003 [0.08] UNLESS OTHERWISE SPECIFIED

CT750006

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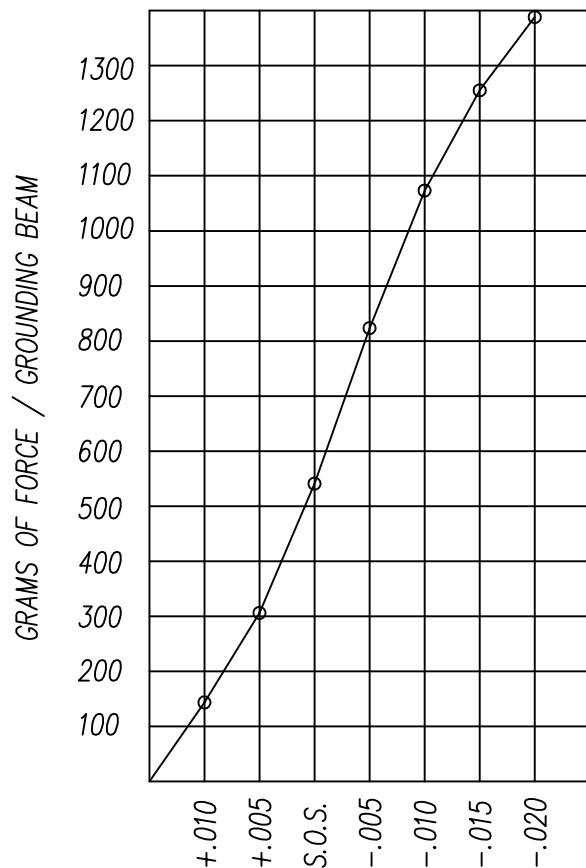
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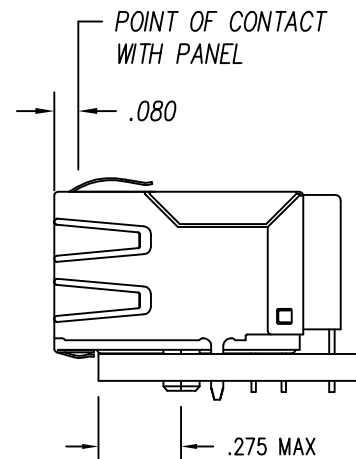
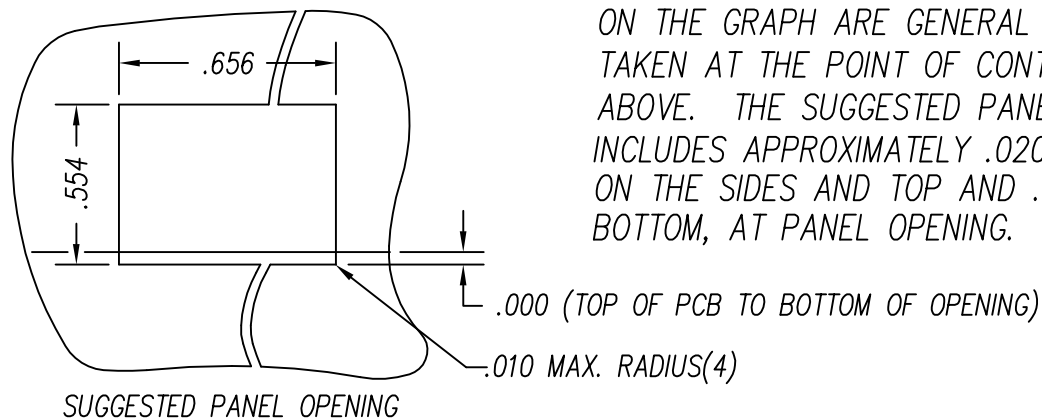
SHEET
2 OF 3

DRAWING NO.

SI-50102 REV. 01



PANEL GROUNDING BEAM DEFLECTION
S.O.S. = SUGGESTED OPENING SIZE



THE SUGGESTED PANEL OPENING IS INTENDED TO GIVE THE USER THE ABILITY TO HAVE REASONABLE JACK / PANEL CLEARANCES YET MAINTAIN RELIABLE GROUNDING CAPABILITY. THESE VARIABLES CAN BE ADJUSTED IN EITHER DIRECTION BUT MAY CARRY SOME CONSEQUENCES IN THE FORM OF LOWER MATING FORCES OR TIGHTER ASSEMBLY TOLERANCES. FORCE VALUES ON THE GRAPH ARE GENERAL AVERAGES TAKEN AT THE POINT OF CONTACT SHOWN ABOVE. THE SUGGESTED PANEL OPENING INCLUDES APPROXIMATELY .020 CLEARANCE ON THE SIDES AND TOP AND .013 ON THE BOTTOM, AT PANEL OPENING.

CT720034X1/24-001302

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SHEET
3 OF 3

DRAWING NO.

SI-50102 REV. 01