

HEF4015B

Dual 4-bit static shift register

Rev. 11 — 8 August 2024

Product data sheet

1. General description

The HEF4015B is a dual edge-triggered 4-bit static shift register (serial-to-parallel converter). Each shift register has a serial data input (nD), a clock input (nCP), four fully buffered parallel outputs (Q0 to Q3) and an overriding asynchronous master reset input (nMR). Information present on nD is shifted to the first register position, and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of nCP. A HIGH on nMR clears the register and forces Q0 to Q3 to LOW, independent of nCP and nD. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{DD} .

2. Features and benefits

- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Tolerant of slow clock rise and fall times
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Complies with JEDEC standard JESD 13-B
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

3. Applications

- Serial-to-parallel converter
- Buffer stores
- General purpose register

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
HEF4015BT	-40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

5. Functional diagram

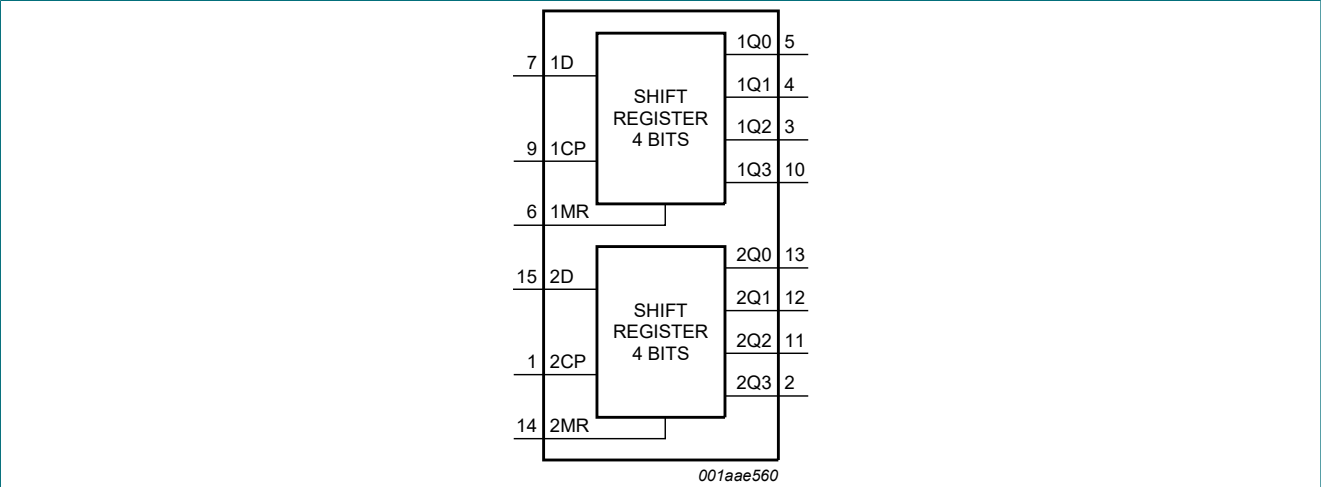


Fig. 1. Functional diagram

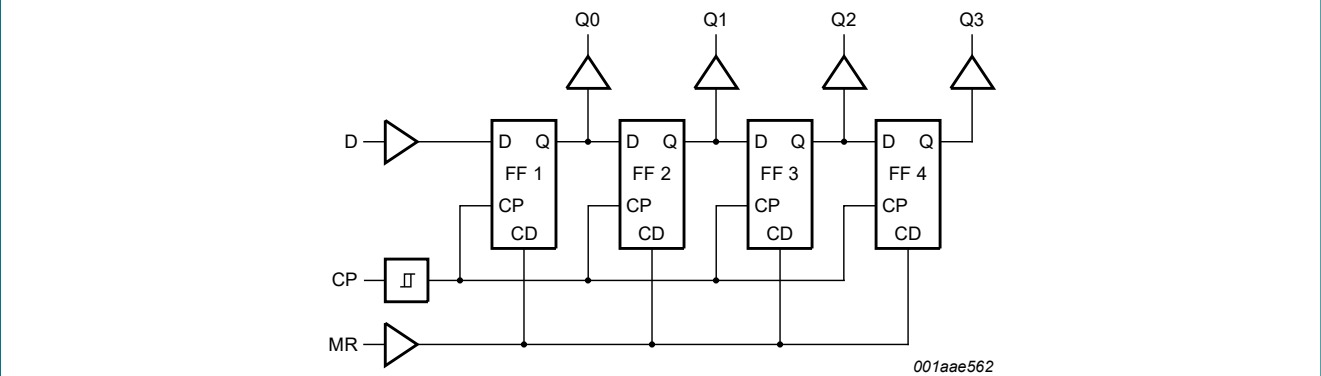
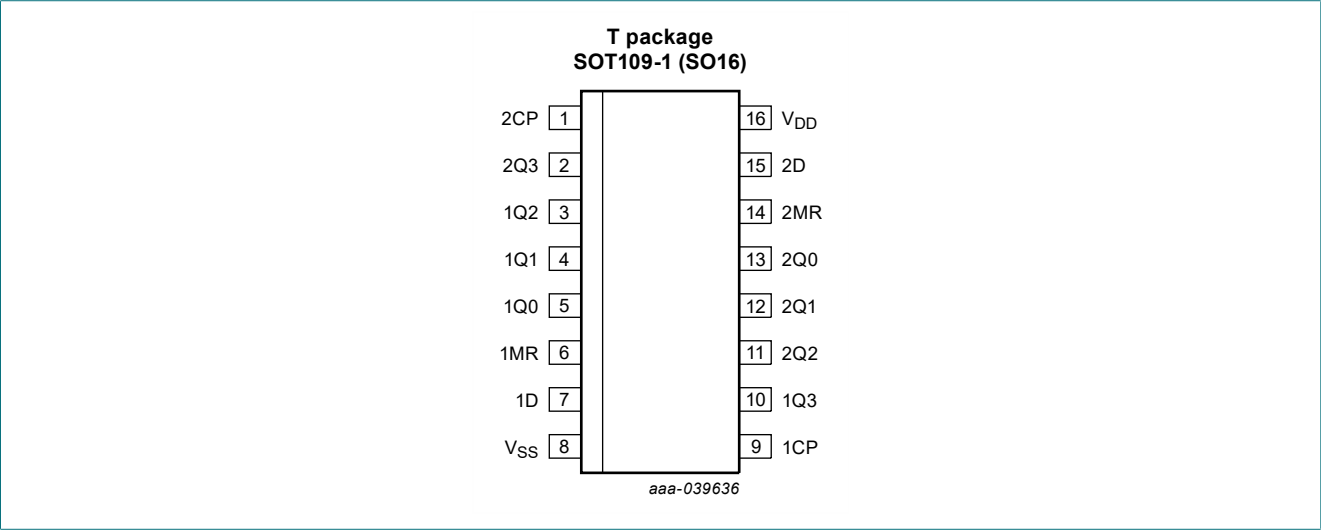


Fig. 2. Logic diagram for one register

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1Q0, 1Q1, 1Q2, 1Q3	5, 4, 3, 10	parallel output
2Q0, 2Q1, 2Q2, 2Q3	13, 12, 11, 2	parallel output
1MR, 2MR	6, 14	master reset input (active HIGH)
1D, 2D	7, 15	serial data input
V _{SS}	8	ground supply voltage
1CP, 2CP	9, 1	clock input (LOW-to-HIGH edge-triggered)
V _{DD}	16	supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Dn = either HIGH or LOW;
↑ = positive-going transition; ↓ = negative-going transition.

number of clock pulse transitions	Input			Output			
	CP	D	MR	Q0	Q1	Q2	Q3
1	↑	D1	L	D1	X	X	X
2	↑	D2	L	D2	D1	X	X
3	↑	D3	L	D3	D2	D1	X
4	↑	D4	L	D4	D3	D2	D1
	↓	X	L	no change	no change	no change	no change
	X	X	H	L	L	L	L

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD}	supply voltage		-0.5	+18	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{DD} + 0.5 V	-	±10	mA
V _I	input voltage		-0.5	V _{DD} + 0.5	V
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{DD} + 0.5 V	-	±10	mA
I _{I/O}	input/output current		-	±10	mA
I _{DD}	supply current		-	50	mA
T _{stg}	storage temperature		-65	+150	°C
T _{amb}	ambient temperature		-40	+85	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +85 °C	-	500	mW
P	power dissipation	per output	-	100	mW

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DD}	supply voltage		3	-	15	V
V _I	input voltage		0	-	V _{DD}	V
T _{amb}	ambient temperature	in free air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	V _{DD} = 5 V	-	-	3.75	μs/V
		V _{DD} = 10 V	-	-	0.5	μs/V
		V _{DD} = 15 V	-	-	0.08	μs/V

10. Static characteristics

Table 6. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V _{DD}	T _{amb} = -40 °C		T _{amb} = 25 °C		T _{amb} = 85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level input voltage	I _O < 1 μA	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V _{IL}	LOW-level input voltage	I _O < 1 μA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V _{OH}	HIGH-level output voltage	I _O < 1 μA	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V _{OL}	LOW-level output voltage	I _O < 1 μA	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I _{OH}	HIGH-level output current	V _O = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		V _O = 4.6 V	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		V _O = 9.5 V	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		V _O = 13.5 V	15 V	-	-3.6	-	-3.0	-	-2.4	mA
I _{OL}	LOW-level output current	V _O = 0.4 V	5 V	0.52	-	0.44	-	0.36	-	mA
		V _O = 0.5 V	10 V	1.3	-	1.1	-	0.9	-	mA
		V _O = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mA
I _I	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	μA
I _{DD}	supply current	I _O = 0 A	5 V	-	20	-	20	-	150	μA
			10 V	-	40	-	40	-	300	μA
			15 V	-	80	-	80	-	600	μA
C _I	input capacitance		-	-	-	-	7.5	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

$V_{SS} = 0\text{ V}$; $C_L = 50\text{ pF}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; for test circuit see Fig. 6.

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula [1]	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	nCP to Qn; see Fig. 3	5 V	$103\text{ ns} + (0.55\text{ ns/pF})C_L$	-	130	260	ns
			10 V	$44\text{ ns} + (0.23\text{ ns/pF})C_L$	-	55	110	ns
			15 V	$32\text{ ns} + (0.16\text{ ns/pF})C_L$	-	40	80	ns
		nMR to Qn; see Fig. 5	5 V	$78\text{ ns} + (0.55\text{ ns/pF})C_L$	-	105	210	ns
			10 V	$34\text{ ns} + (0.23\text{ ns/pF})C_L$	-	45	90	ns
			15 V	$27\text{ ns} + (0.16\text{ ns/pF})C_L$	-	35	70	ns
t_{PLH}	LOW to HIGH propagation delay	nCP to Qn; see Fig. 3	5 V	$93\text{ ns} + (0.55\text{ ns/pF})C_L$	-	120	240	ns
			10 V	$44\text{ ns} + (0.23\text{ ns/pF})C_L$	-	55	110	ns
			15 V	$32\text{ ns} + (0.16\text{ ns/pF})C_L$	-	40	80	ns
t_t	transition time	see Fig. 3	5 V	$10\text{ ns} + (1.00\text{ ns/pF})C_L$	-	60	120	ns
			10 V	$9\text{ ns} + (0.42\text{ ns/pF})C_L$	-	30	60	ns
			15 V	$6\text{ ns} + (0.28\text{ ns/pF})C_L$	-	20	40	ns
t_{su}	set-up time	nD to nCP; see Fig. 4	5 V		+25	-15	-	ns
			10 V		+25	-10	-	ns
			15 V		+20	-5	-	ns
t_h	hold time	nD to nCP; see Fig. 4	5 V		40	20	-	ns
			10 V		20	10	-	ns
			15 V		15	8	-	ns
t_W	pulse width	nCP LOW; minimum width; see Fig. 4	5 V		60	30	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
		nMR HIGH; minimum width; see Fig. 5	5 V		80	40	-	ns
			10 V		30	15	-	ns
			15 V		24	12	-	ns
t_{rec}	recovery time	pin nMR; see Fig. 5	5 V		50	20	-	ns
			10 V		30	10	-	ns
			15 V		20	5	-	ns
f_{max}	maximum frequency	see Fig. 4	5 V		7	15	-	MHz
			10 V		15	30	-	MHz
			15 V		22	44	-	MHz

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

Table 8. Dynamic power dissipation P_D

P_D can be calculated from the formulas shown. $V_{SS} = 0\text{ V}$; $t_r = t_f \leq 20\text{ ns}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Symbol	Parameter	V_{DD}	Typical formula for P_D (μW)	where:
P_D	dynamic power dissipation	5 V	$P_D = 1500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF; V_{DD} = supply voltage in V; $\Sigma(C_L \times f_o)$ = sum of the outputs.
		10 V	$P_D = 6300 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 17000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	

11.1. Waveforms and test circuit

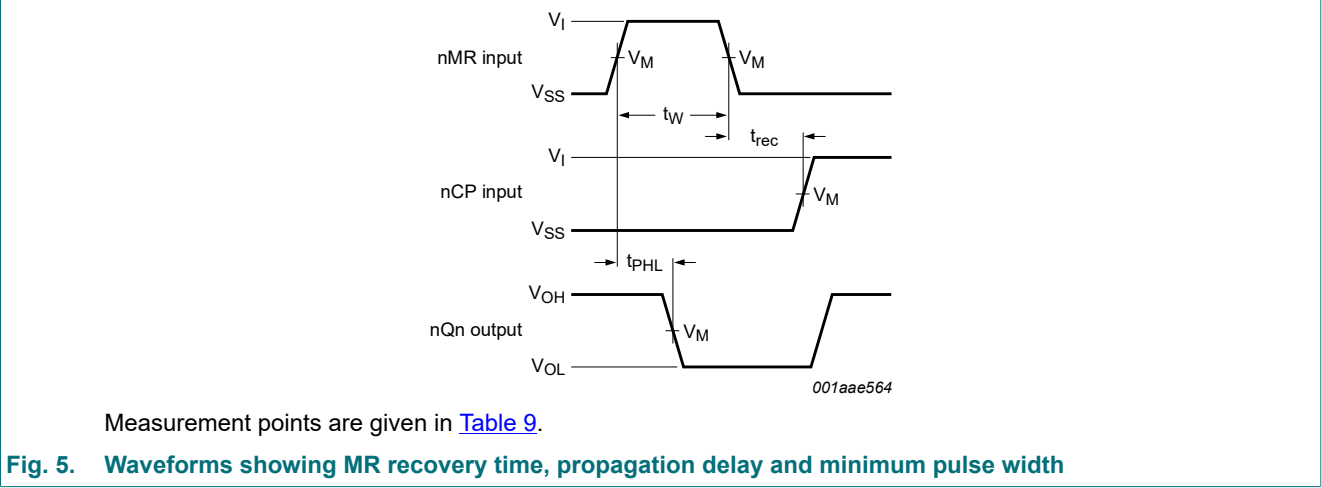
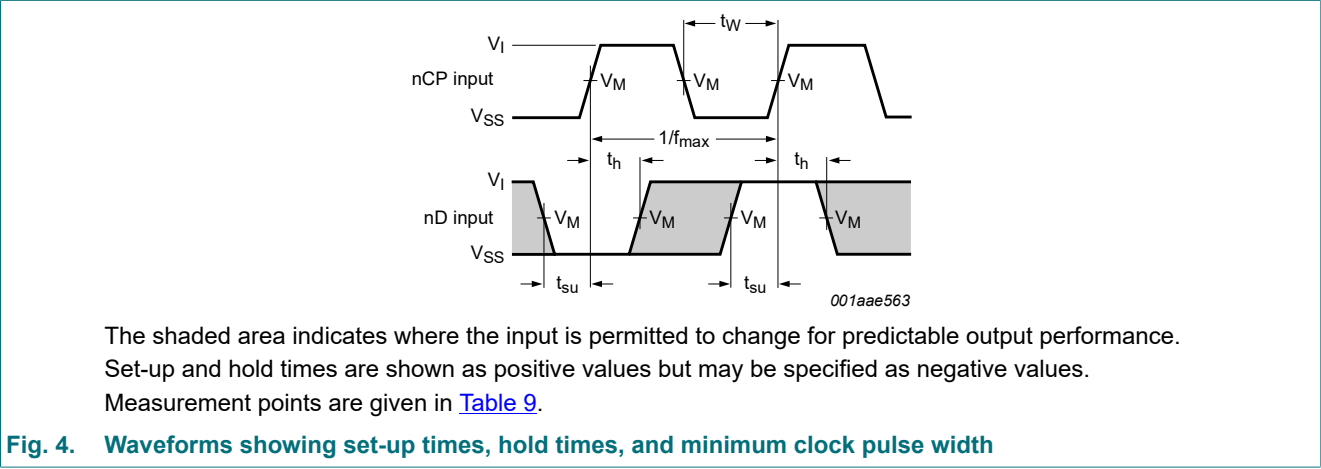
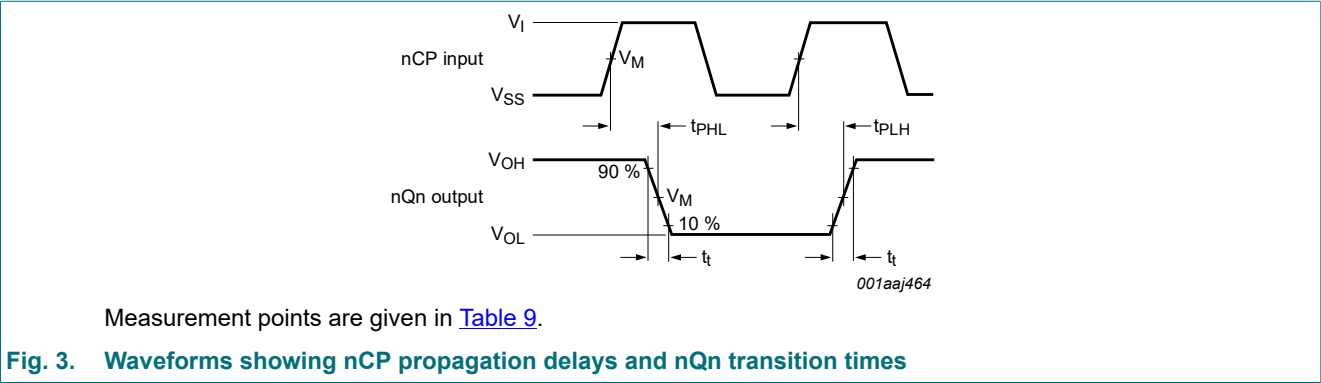


Table 9. Measurement points

Supply voltage	Input	Output
V _{DD}	V _M	V _M
5 V to 15 V	0.5V _{DD}	0.5V _{DD}

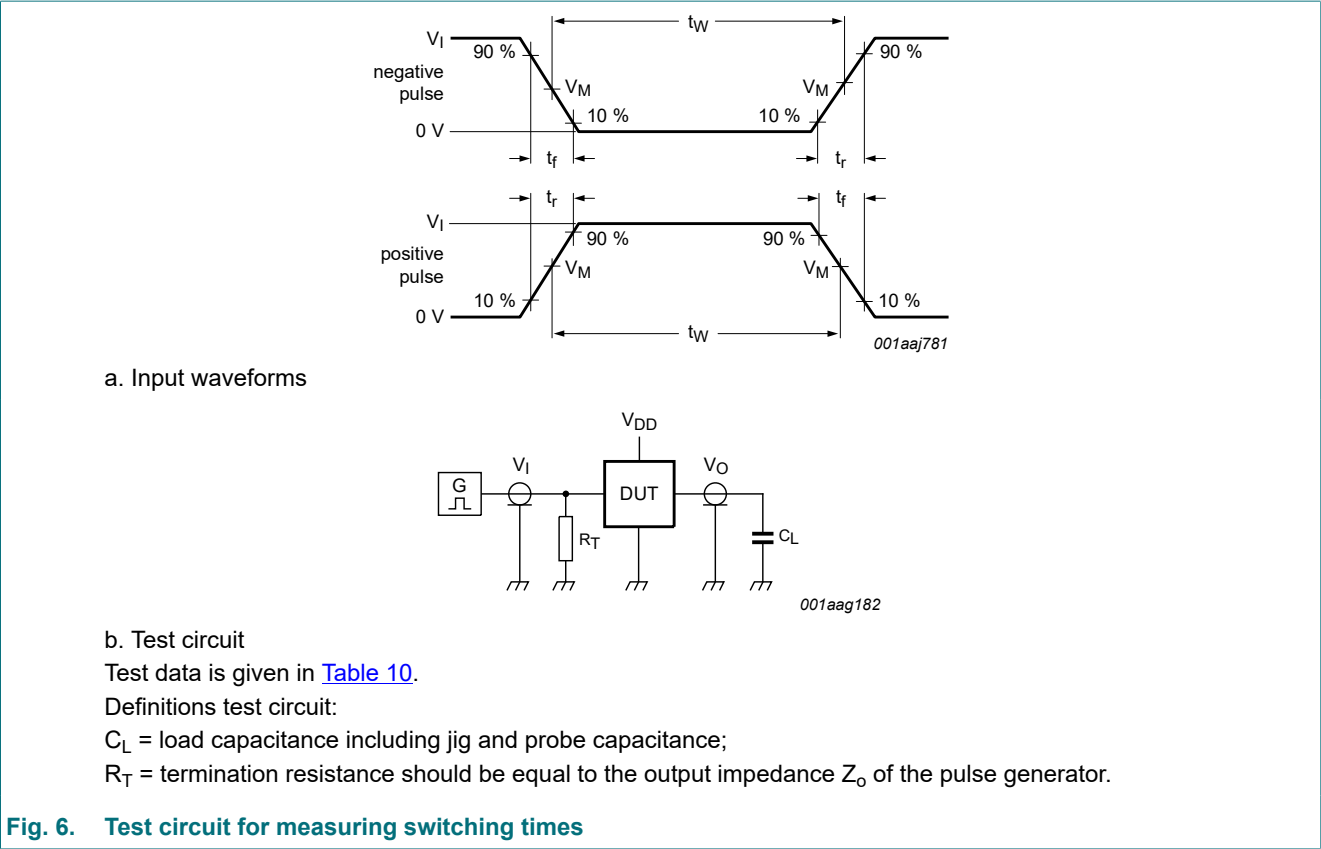


Table 10. Test data

Supply voltage	Input		Load
V_{DD}	V_I	t_r, t_f	C_L
5 V to 15 V	V_{SS} or V_{DD}	≤ 20 ns	50 pF

12. Package outline

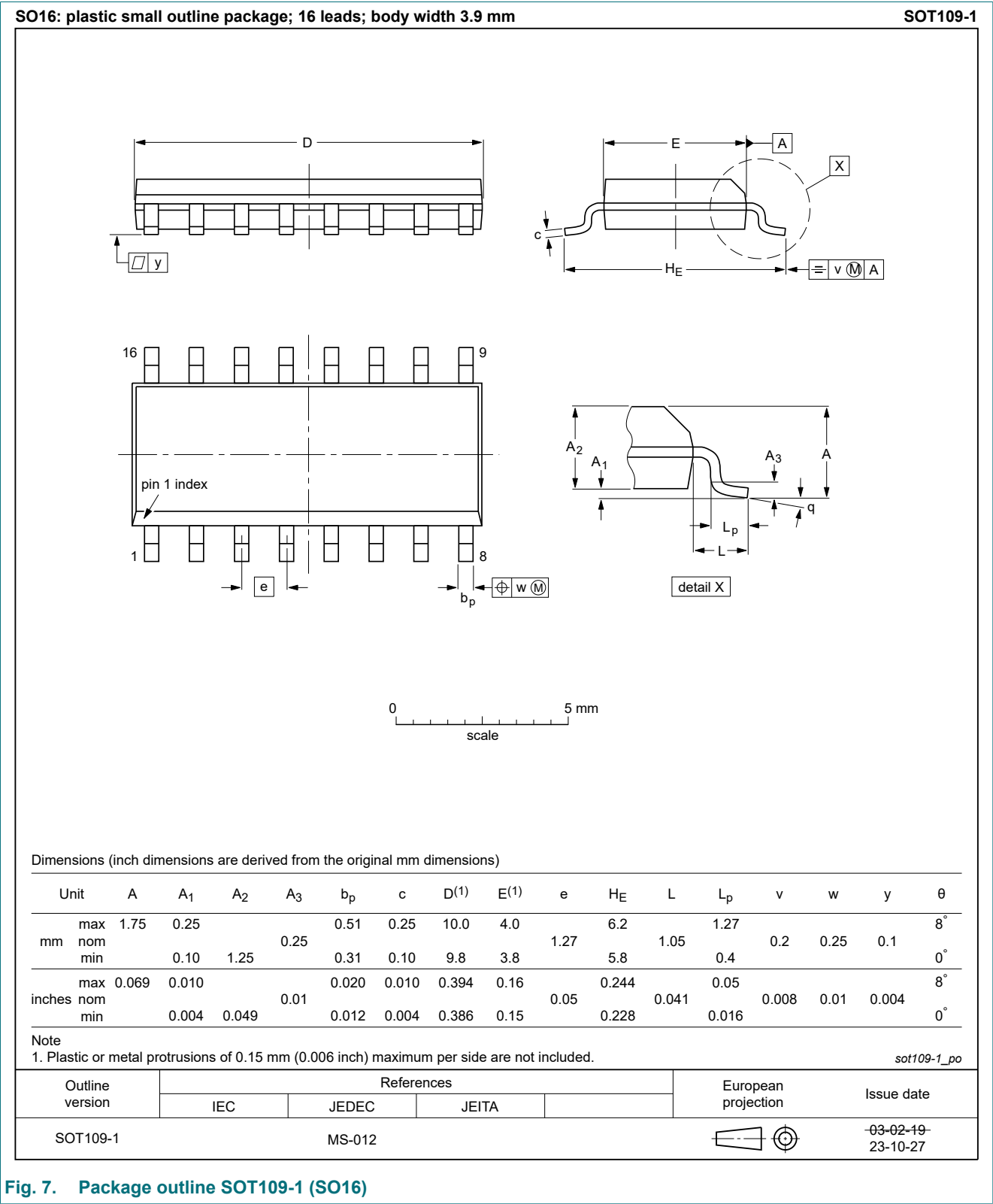


Fig. 7. Package outline SOT109-1 (SO16)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4015B v.11	20240808	Product data sheet	-	HEF4015B v.10
Modifications:	- Section 2: ESD specification updated according to the latest JEDEC standard. - Fig. 7: Aligned SO package outline drawing to JEDEC MS-012			
HEF4015B v.10	20211126	Product data sheet	-	HEF4015B v.9
Modifications:	Section 1 and Section 2 updated.			
HEF4015B v.9	20160321	Product data sheet	-	HEF4015B v.8
Modifications:	Type number HEF4015BP (SOT38-4) removed.			
HEF4015B v.8	20111121	Product data sheet	-	HEF4015B v.7
Modifications:	- Legal pages updated. - Changes in "General description" and "Features and benefits".			
HEF4015B v.7	20110914	Product data sheet	-	HEF4015B v.6
HEF4015B v.6	20091103	Product data sheet	-	HEF4015B v.5
HEF4015B v.5	20090624	Product data sheet	-	HEF4015B v.4
HEF4015B v.4	20090127	Product data sheet	-	HEF4015B_CNV v.3
HEF4015B_CNV v.3	19950101	Product specification	-	HEF4015B_CNV v.2
HEF4015B_CNV v.2	19950101	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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Date of release: 8 August 2024