

# 74HC574

## Octal 3-State Noninverting D Flip-Flop

### High-Performance Silicon-Gate CMOS

The 74HC574 is identical in pinout to the LS574. The device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

Data meeting the set-up time is clocked to the outputs with the rising edge of the Clock. The Output Enable input does not affect the states of the flip-flops but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be stored even when the outputs are not enabled.

The HC574 is identical in function to the HC374A but has the flip-flop inputs on the opposite side of the package from the outputs to facilitate PC board layout.

#### Features

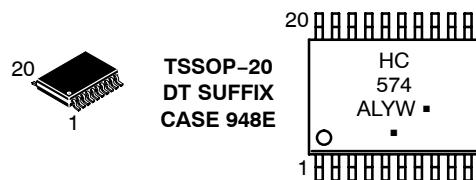
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 266 FETs or 66.5 Equivalent Gates
- This is a Pb-Free Device



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#### MARKING DIAGRAMS



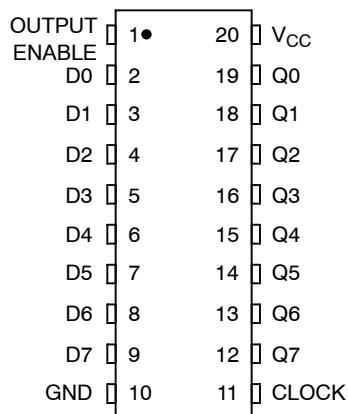
HC574 = Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

# 74HC574



FUNCTION TABLE

| Inputs |       | Output |           |
|--------|-------|--------|-----------|
| OE     | Clock | D      | Q         |
| L      | /     | H      | H         |
| L      | /     | L      | L         |
| L      | L,H,~ | X      | No Change |
| H      | X     | X      | Z         |

X = Don't Care

Z = High Impedance

Figure 1. Pin Assignment

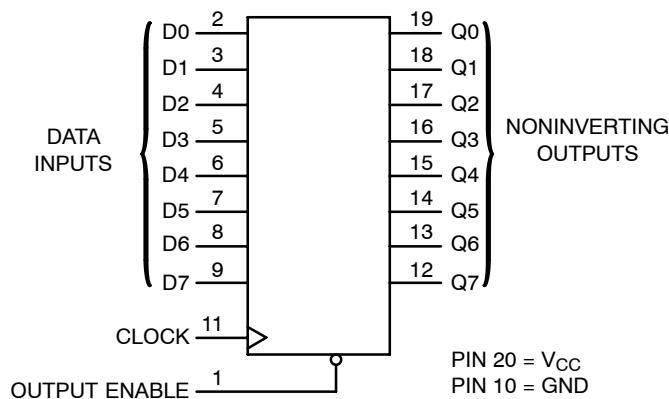


Figure 2. Logic Diagram

| Design Criteria                 | Value  | Units |
|---------------------------------|--------|-------|
| Internal Gate Count*            | 66.5   | ea.   |
| Internal Gate Propagation Delay | 1.5    | ns    |
| Internal Gate Power Dissipation | 5.0    | µW    |
| Speed Power Product             | 0.0075 | pJ    |

\*Equivalent to a two-input NAND gate.

## MAXIMUM RATINGS

| Symbol        | Parameter  | Value                 | Unit |
|---------------|--|-----------------------|------|
| $V_{CC}$      | DC Supply Voltage  | –0.5 to +7.0          | V    |
| $V_I$         | DC Input Voltage   | –0.5 to $V_{CC}$ +0.5 | V    |
| $V_O$         | DC Output Voltage<br>(Note 1)  | –0.5 to $V_{CC}$ +0.5 | V    |
| $I_{IK}$      | DC Input Diode Current   | ±20                   | mA   |
| $I_{OK}$      | DC Output Diode Current  | ±35                   | mA   |
| $I_O$         | DC Output Sink Current   | ±35                   | mA   |
| $I_{CC}$      | DC Supply Current per Supply Pin   | ±75                   | mA   |
| $I_{GND}$     | DC Ground Current per Ground Pin   | ±75                   | mA   |
| $T_{STG}$     | Storage Temperature Range  | –65 to +150           | °C   |
| $T_L$         | Lead Temperature, 1 mm from Case for 10 Seconds                              | 260                   | °C   |
| $T_J$         | Junction Temperature under Bias  | +150                  | °C   |
| $\theta_{JA}$ | Thermal Resistance<br>TSSOP  | 128                   | °C/W |
| $P_D$         | Power Dissipation in Still Air at 85°C<br>TSSOP                              | 450                   | mW   |
| MSL           | Moisture Sensitivity   | Level 1               |      |
| $F_R$         | Flammability Rating<br>Oxygen Index: 30% – 35%                               | UL 94 V-0 @ 0.125 in  |      |
| $V_{ESD}$     | ESD Withstand Voltage<br>Human Body Model (Note 2)<br>Machine Model (Note 3) | >2000<br>>200         | V    |
| $I_{Latchup}$ | Latchup Performance<br>Above $V_{CC}$ and Below GND at 85°C (Note 4)         | ±300                  | mA   |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1.  $I_O$  absolute maximum rating must be observed.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to EIA/JESD78.
5. For high frequency or heavy load considerations, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

## RECOMMENDED OPERATING CONDITIONS

| Symbol     | Parameter   | Min         | Max                | Unit |
|------------|---|-------------|--------------------|------|
| $V_{CC}$   | DC Supply Voltage<br>(Referenced to GND)  | 2.0         | 6.0                | V    |
| $V_I, V_O$ | DC Input Voltage, Output Voltage<br>(Referenced to GND)   | 0           | $V_{CC}$           | V    |
| $T_A$      | Operating Temperature, All Package Types  | –55         | +125               | °C   |
| $t_r, t_f$ | Input Rise and Fall Time (Figure 3)<br>$V_{CC} = 2.0$ V<br>$V_{CC} = 4.5$ V<br>$V_{CC} = 6.0$ V | 0<br>0<br>0 | 1000<br>500<br>400 | ns   |

6. Unused inputs may not be left open. All inputs must be tied to a high- or low-logic input voltage level.

## ORDERING INFORMATION

| Device       | Package   | Shipping <sup>†</sup> |
|--------------|-----------|-----------------------|
| 74HC574DTR2G | TSSOP-20* | 2500 / Tape & Reel    |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol          | Parameter                                      | Test Conditions   | V <sub>CC</sub> (V)      | Guaranteed Limit          |                           |                           | Unit |
|-----------------|--|---|--------------------------|---------------------------|---------------------------|---------------------------|------|
|                 |  |   |                          | –55 to 25°C               | ≤ 85°C                    | ≤ 125°C                   |      |
| V <sub>IH</sub> | Minimum High-Level Input Voltage               | V <sub>out</sub> = V <sub>CC</sub> – 0.1 V<br> I <sub>out</sub>   ≤ 20 µA   | 2.0<br>3.0<br>4.5<br>6.0 | 1.5<br>2.1<br>3.15<br>4.2 | 1.5<br>2.1<br>3.15<br>4.2 | 1.5<br>2.1<br>3.15<br>4.2 | V    |
| V <sub>IL</sub> | Maximum Low-Level Input Voltage                | V <sub>out</sub> = 0.1 V<br> I <sub>out</sub>   ≤ 20 µA   | 2.0<br>3.0<br>4.5<br>6.0 | 0.5<br>0.9<br>1.35<br>1.8 | 0.5<br>0.9<br>1.35<br>1.8 | 0.5<br>0.9<br>1.35<br>1.8 | V    |
| V <sub>OH</sub> | Minimum High-Level Output Voltage              | V <sub>in</sub> = V <sub>IH</sub><br> I <sub>out</sub>   ≤ 20 µA  | 2.0<br>4.5<br>6.0        | 1.9<br>4.4<br>5.9         | 1.9<br>4.4<br>5.9         | 1.9<br>4.4<br>5.9         | V    |
| V <sub>OH</sub> | Minimum High-Level Output Voltage              | V <sub>in</sub> = V <sub>IH</sub><br> I <sub>out</sub>   ≤ 2.4 mA<br> I <sub>out</sub>   ≤ 6.0 mA<br> I <sub>out</sub>   ≤ 7.8 mA   | 3.0<br>4.5<br>6.0        | 2.48<br>3.98<br>5.48      | 2.34<br>3.84<br>5.34      | 2.2<br>3.7<br>5.2         | V    |
| V <sub>OL</sub> | Maximum Low-Level Output Voltage               | V <sub>in</sub> = V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 µA  | 2.0<br>4.5<br>6.0        | 0.1<br>0.1<br>0.1         | 0.1<br>0.1<br>0.1         | 0.1<br>0.1<br>0.1         | V    |
|                 |  | V <sub>in</sub> = V <sub>IL</sub><br> I <sub>out</sub>   ≤ 2.4 mA<br> I <sub>out</sub>   ≤ 6.0 mA<br> I <sub>out</sub>   ≤ 7.8 mA   | 3.0<br>4.5<br>6.0        | 0.26<br>0.26<br>0.26      | 0.33<br>0.33<br>0.33      | 0.4<br>0.4<br>0.4         |      |
| I <sub>in</sub> | Maximum Input Leakage Current                  | V <sub>in</sub> = V <sub>CC</sub> or GND  | 6.0                      | ± 0.1                     | ± 1.0                     | ± 1.0                     | µA   |
| I <sub>OZ</sub> | Maximum Three-State Leakage Current            | Output in High-Impedance State<br>V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>V <sub>out</sub> = V <sub>CC</sub> or GND | 6.0                      | ± 0.5                     | ± 5.0                     | ± 10                      | µA   |
| I <sub>CC</sub> | Maximum Quiescent Supply Current (per Package) | V <sub>in</sub> = V <sub>CC</sub> or GND<br>I <sub>out</sub> = 0 µA   | 6.0                      | 4.0                       | 40                        | 40                        | µA   |

7. Information on typical parametric values can be found in the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

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## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50 \text{ pF}$ ; Input $t_r = t_f = 6.0 \text{ ns}$ )

| Symbol             | Parameter  | V <sub>CC</sub> (V)      | Guaranteed Limit       |                        |                        | Unit |
|--------------------|--|--------------------------|------------------------|------------------------|------------------------|------|
|                    |  |                          | –55 to 25°C            | ≤ 85°C                 | ≤ 125°C                |      |
| $f_{\max}$         | Maximum Clock Frequency (50% Duty Cycle)<br>(Figures 3 and 6)          | 2.0<br>3.0<br>4.5<br>6.0 | 6.0<br>15<br>30<br>35  | 4.8<br>10<br>24<br>28  | 4.0<br>8.0<br>20<br>24 | MHz  |
| $t_{PLH}, t_{PHL}$ | Maximum Propagation Delay, Clock to Q<br>(Figures 3 and 6)             | 2.0<br>3.0<br>4.5<br>6.0 | 160<br>105<br>32<br>27 | 200<br>145<br>40<br>34 | 240<br>190<br>48<br>41 | ns   |
| $t_{PLZ}, t_{PHZ}$ | Maximum Propagation Delay, Output Enable to Q<br>(Figures 4 and 7)     | 2.0<br>3.0<br>4.5<br>6.0 | 150<br>100<br>30<br>26 | 190<br>125<br>38<br>33 | 225<br>150<br>45<br>38 | ns   |
| $t_{PZL}, t_{PZH}$ | Maximum Propagation Delay, Output Enable to Q<br>(Figures 4 and 7)     | 2.0<br>3.0<br>4.5<br>6.0 | 140<br>90<br>28<br>24  | 175<br>120<br>35<br>30 | 210<br>140<br>42<br>36 | ns   |
| $t_{TLH}, t_{THL}$ | Maximum Output Transition Time, any Output<br>(Figures 3 and 6)        | 2.0<br>3.0<br>4.5<br>6.0 | 60<br>27<br>12<br>10   | 75<br>32<br>15<br>13   | 90<br>36<br>18<br>15   | ns   |
| $C_{in}$           | Maximum Input Capacitance  |                          | 10                     | 10                     | 10                     | pF   |
| $C_{out}$          | Maximum Three-State Output Capacitance, Output in High-Impedance State |                          | 15                     | 15                     | 15                     | pF   |

8. For propagation delays with loads other than 50 pF, and information on typical parametric values, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

| C <sub>PD</sub> | Power Dissipation Capacitance (Per Enabled Output)* | Typical @ 25°C, V <sub>CC</sub> = 5.0 V |    | pF |
|-----------------|---|---|----|----|
|                 |   | 24                                      | 24 |    |

\*Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ . For load considerations, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

## TIMING REQUIREMENTS ( $C_L = 50 \text{ pF}$ ; Input $t_r = t_f = 6.0 \text{ ns}$ )

| Symbol     | Parameter                         | Figure | V <sub>CC</sub> (V)      | Guaranteed Limit         |                           |                          |                           |                          |                           | Unit |  |
|------------|-----------------------------------|--------|--------------------------|--------------------------|---------------------------|--------------------------|---------------------------|--------------------------|---------------------------|------|--|
|            |                                   |        |                          | –55 to 25°C              |                           | ≤ 85°C                   |                           | ≤ 125°C                  |                           |      |  |
|            |                                   |        |                          | Min                      | Max                       | Min                      | Max                       | Min                      | Max                       |      |  |
| $t_{su}$   | Minimum Setup Time, Data to Clock | 5      | 2.0<br>3.0<br>4.6<br>6.0 | 50<br>40<br>10<br>9.0    |                           | 65<br>50<br>13<br>11     |                           | 75<br>60<br>15<br>13     |                           | ns   |  |
| $t_h$      | Minimum Hold Time, Clock to Data  | 5      | 2.0<br>3.0<br>4.5<br>6.0 | 5.0<br>5.0<br>5.0<br>5.0 |                           | 5.0<br>5.0<br>5.0<br>5.0 |                           | 5.0<br>5.0<br>5.0<br>5.0 |                           | ns   |  |
| $t_w$      | Minimum Pulse Width, Clock        | 3      | 2.0<br>3.0<br>4.5<br>6.0 | 75<br>60<br>15<br>13     |                           | 95<br>80<br>19<br>16     |                           | 110<br>90<br>22<br>19    |                           | ns   |  |
| $t_r, t_f$ | Maximum Input Rise and Fall Times | 3      | 2.0<br>3.0<br>4.5<br>6.0 |                          | 1000<br>800<br>500<br>400 |                          | 1000<br>800<br>500<br>400 |                          | 1000<br>800<br>500<br>400 | ns   |  |

SWITCHING WAVEFORMS

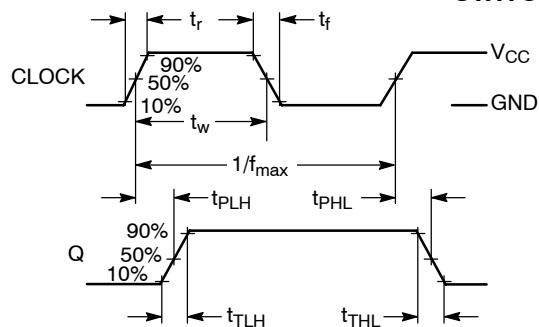


Figure 3.

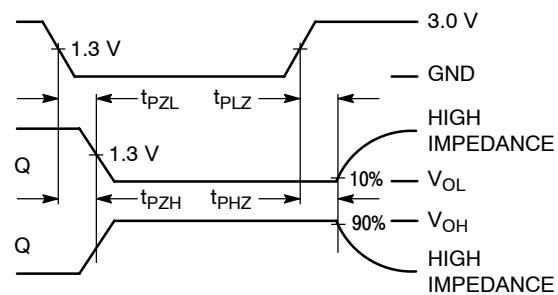


Figure 4.

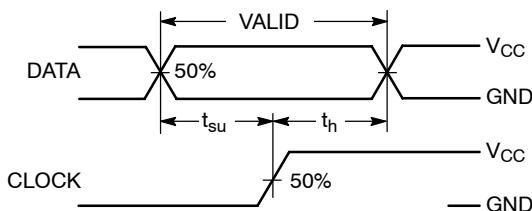
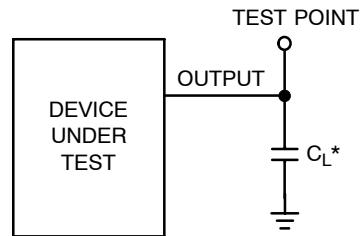
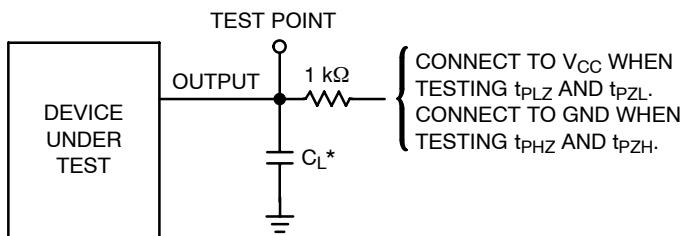


Figure 5.



\*Includes all probe and jig capacitance.

Figure 6.



\*Includes all probe and jig capacitance.

Figure 7. Test Circuit

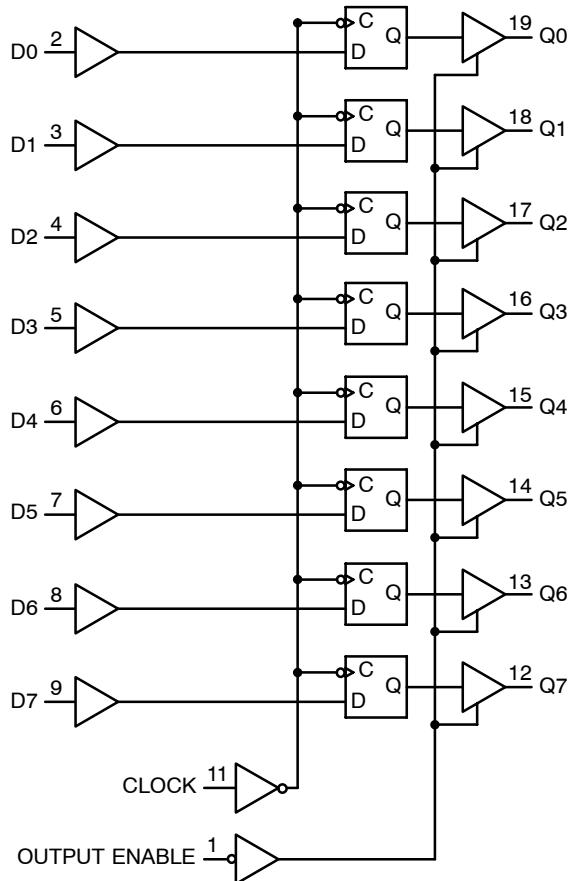
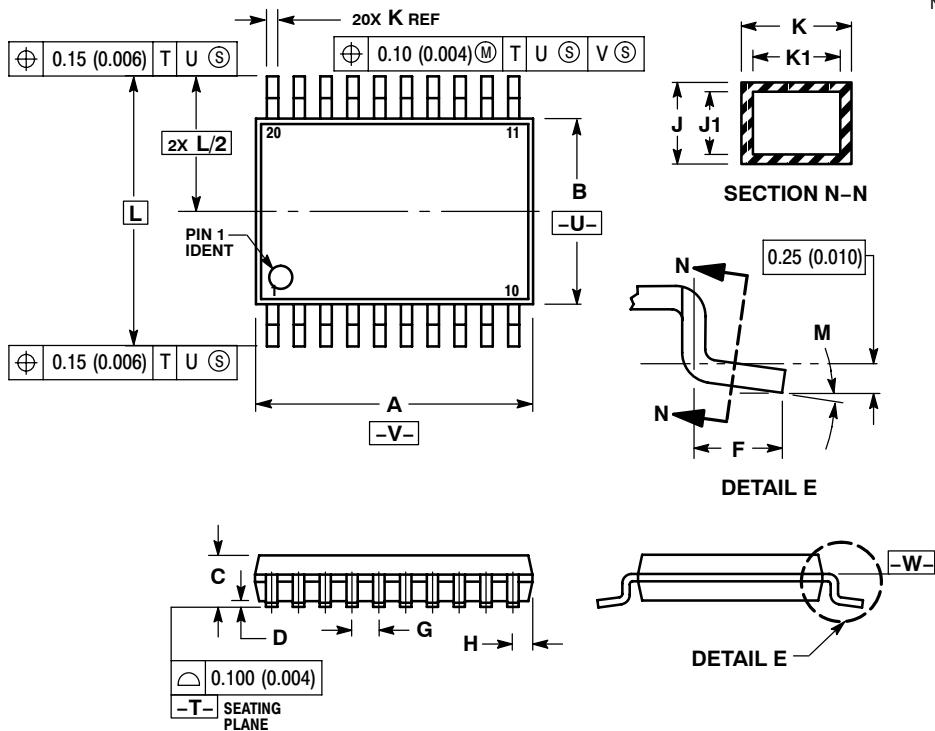


Figure 8. Expanded Logic Diagram

## PACKAGE DIMENSIONS

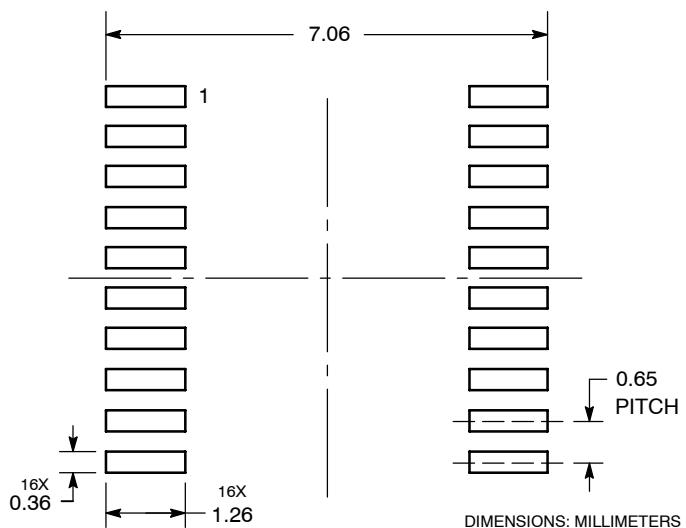
TSSOP-20  
CASE 948E-02  
ISSUE C

## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 6.40        | 6.60 | 0.252     | 0.260 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.27        | 0.37 | 0.011     | 0.015 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

## SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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