

74LVC377

Octal D-type flip-flop with data enable; positive-edge trigger

Rev. 8 — 28 August 2023

Product data sheet

1. General description

The 74LVC377 is an octal positive-edge triggered D-type flip-flop. The device features clock (CP) and data enable (E) inputs. When E is LOW, the outputs Qn will assume the state of their corresponding D inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. Input E must be stable one set-up time prior to the LOW-to-HIGH transition for predictable operation. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

2. Features and benefits

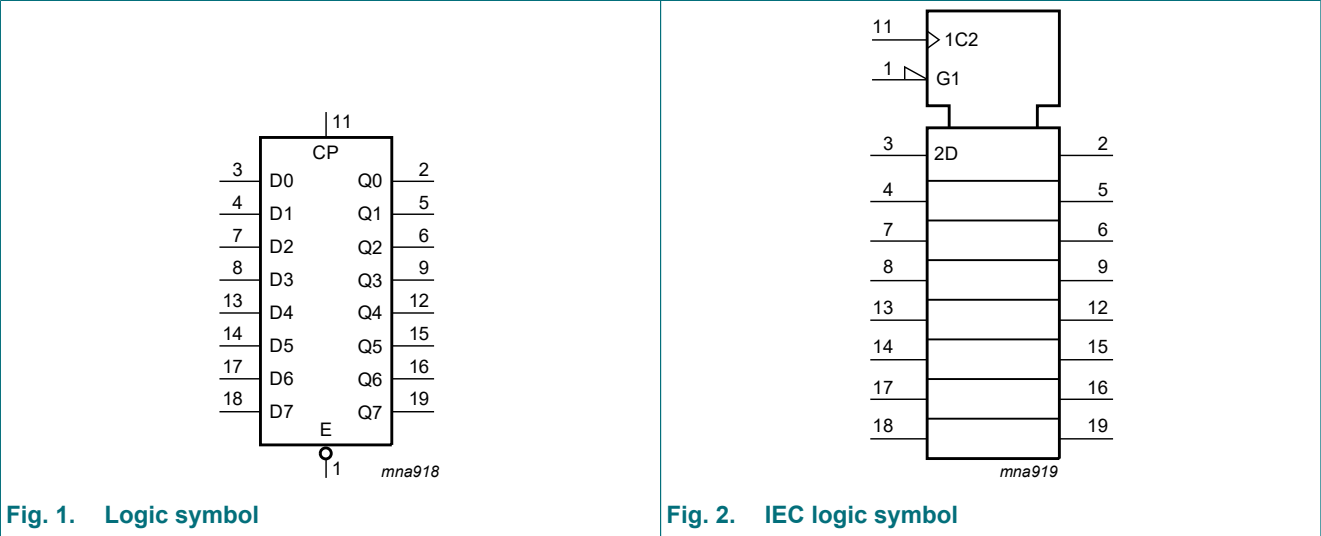
- Wide supply voltage range from 1.2 V to 3.6 V
- Overvoltage tolerant inputs to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Output drive capability 50 Ω transmission lines at 125 °C
- Complies with JEDEC standard:
 - JESD8-7A (1.65 V to 1.95 V)
 - JESD8-5A (2.3 V to 2.7 V)
 - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

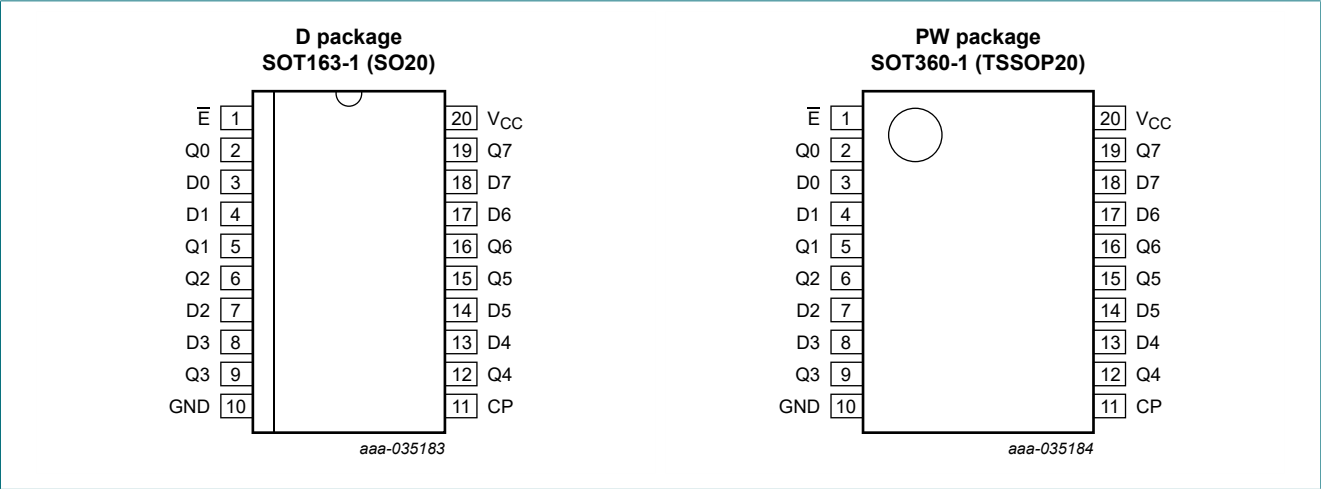
Type number	Package			
	Temperature range	Name	Description	Version
74LVC377D	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVC377PW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
E	1	data enable input (active LOW)
CP	11	clock input (LOW to HIGH; edge-triggered)
D0, D1, D2, D3, D4, D5, D6, D7	3, 4, 7, 8, 13, 14, 17, 18	data input
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	2, 5, 6, 9, 12, 15, 16, 19	flip-flop output
GND	10	ground (0 V)
V _{CC}	20	power supply

6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW to HIGH CP transition

L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW to HIGH CP transition

↑ = LOW to HIGH CP transition; NC = no change; X = don't care

Operating mode	Control		Input	Output
	CP	E	Dn	Qn
Load 1	↑	l	h	H
Load 0	↑	l	l	L
Hold	↑	h	X	NC
Do nothing	X	H	X	NC

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
V _I	input voltage	[1]	-0.5	+5.5	V
V _O	output voltage	[2]	-0.5	V _{CC} + 0.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [3]	-	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SOT163-1 (SO20) package: P_{tot} derates linearly with 12.3 mW/K above 109 °C.
For SOT360-1 (TSSOP20) package: P_{tot} derates linearly with 10.0 mW/K above 100 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V _I	input voltage		0	-	5.5	V
V _O	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
		V _{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V _{CC} = 1.65 V to 1.95 V	0.65V _{CC}	-	-	0.65V _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V _{CC} = 1.65 V to 1.95 V	-	-	0.35V _{CC}	-	0.35V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -100 µA; V _{CC} = 1.65 V to 3.6 V	V _{CC} - 0.2	-	-	V _{CC} - 0.3	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I _O = -18 mA; V _{CC} = 3.0 V	2.4	-	-	2.25	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.2	-	-	2.0	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 100 µA; V _{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.8	V
I _I	input leakage current	V _{CC} = 3.6 V; V _I = 5.5 V or GND	-	±0.1	±5	-	±20	µA
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.1	10	-	40	µA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	5	500	-	5000	µA
C _I	input capacitance	V _{CC} = 0 V to 3.6 V; V _I = GND to V _{CC}	-	5.0	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 5.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t_{pd}	propagation delay	CP to Qn; see Fig. 3 [2]						
		$V_{CC} = 1.2\text{ V}$	-	15	-	-	-	ns
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	2.5	7.4	14.5	2.5	15.5	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.8	4.4	8.5	1.8	9.1	ns
		$V_{CC} = 2.7\text{ V}$	1.5	4.3	7.9	1.5	10.0	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.5	4.0	7.6	1.5	9.5	ns
t_W	pulse width	clock HIGH or LOW; see Fig. 3						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	6.0	-	-	6.0	-	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	5.0	-	-	5.0	-	ns
		$V_{CC} = 2.7\text{ V}$	5.0	1.6	-	5.0	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	4.0	1.0	-	4.0	-	ns
t_{su}	set-up time	$\bar{E}$ to CP; see Fig. 4						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	5.5	-	-	5.5	-	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	4.5	-	-	4.5	-	ns
		$V_{CC} = 2.7\text{ V}$	4.0	0.6	-	4.0	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	3.0	0.2	-	3.0	-	ns
		Dn to CP; see Fig. 4						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	5.5	-	-	5.5	-	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	4.5	-	-	4.5	-	ns
		$V_{CC} = 2.7\text{ V}$	3.0	1.0	-	3.0	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	2.0	0.7	-	2.0	-	ns
t_h	hold time	$\bar{E}$ to CP; see Fig. 4						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	1.5	-	-	1.5	-	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.5	-	-	0.5	-	ns
		$V_{CC} = 2.7\text{ V}$	0.0	-1.0	-	0.0	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.0	0	-	1.0	-	ns
		Dn to CP; see Fig. 4						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	1.5	-	-	1.5	-	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.5	-	-	0.5	-	ns
		$V_{CC} = 2.7\text{ V}$	0.0	-1.1	-	0.0	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	0.0	-1.0	-	0.0	-	ns
f_{max}	maximum frequency	see Fig. 3						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	80	-	-	64	-	MHz
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	100	-	-	80	-	MHz
		$V_{CC} = 2.7\text{ V}$	150	-	-	120	-	MHz
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	150	330	-	120	-	MHz
$t_{sk(o)}$	output skew time	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [3]	-	-	1.0	-	1.5	ns

Octal D-type flip-flop with data enable; positive-edge trigger

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
C _{PD}	power dissipation capacitance	per flip-flop; V _I = GND to V _{CC} [4]						
		V _{CC} = 1.65 V to 1.95 V	-	12.1	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	15.8	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	19.0	-	-	-	pF

- [1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
- [4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; f_o = output frequency in MHz
C_L = output load capacitance in pF
V_{CC} = supply voltage in Volts
N = number of inputs switching
Σ(C_L × V_{CC}² × f_o) = sum of the outputs

10.1. Waveforms and test circuit

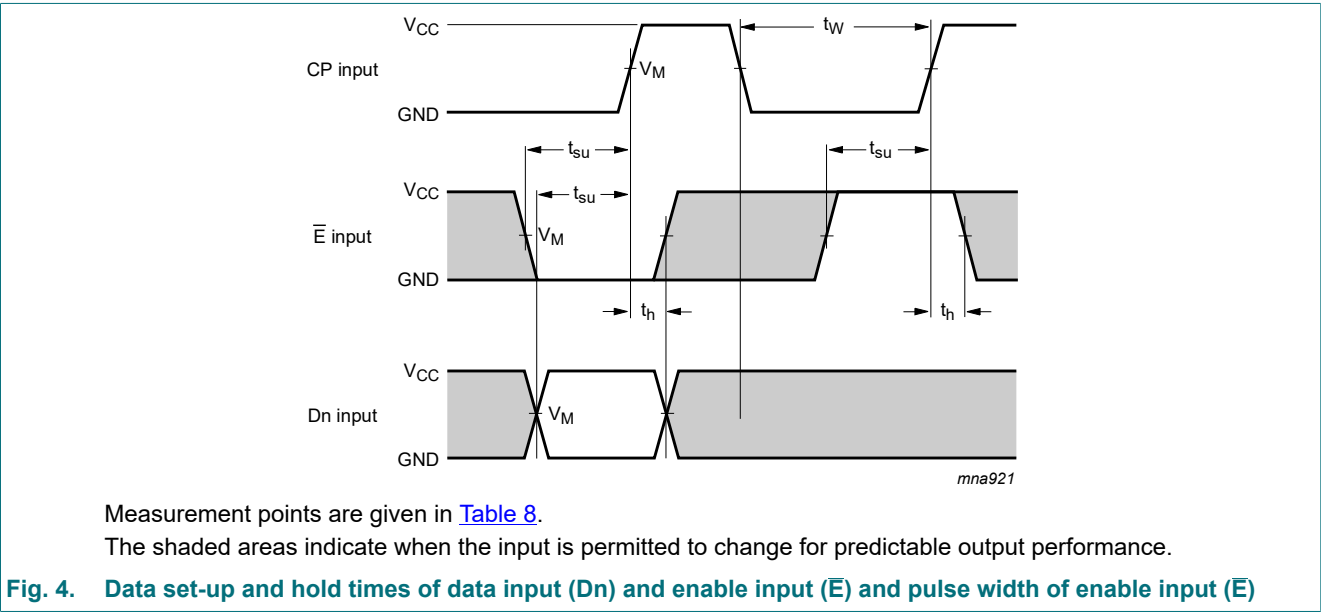
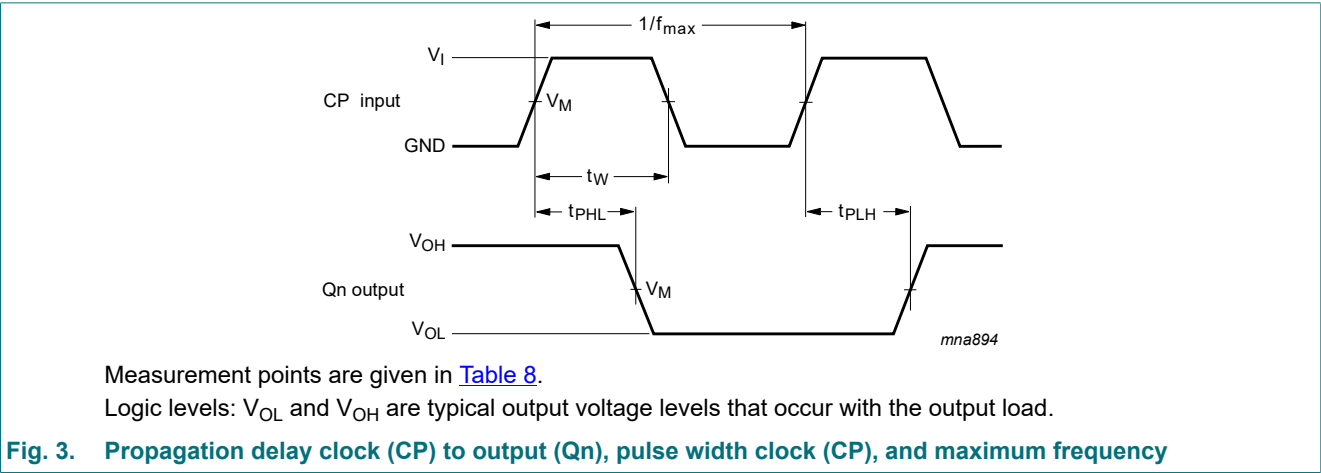


Table 8. Measurement points

Supply voltage	Input	Output
V _{CC}	V _M	V _M
1.2 V	0.5 × V _{CC}	0.5 × V _{CC}
1.65 V to 1.95 V	0.5 × V _{CC}	0.5 × V _{CC}
2.3 V to 2.7 V	0.5 × V _{CC}	0.5 × V _{CC}
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V

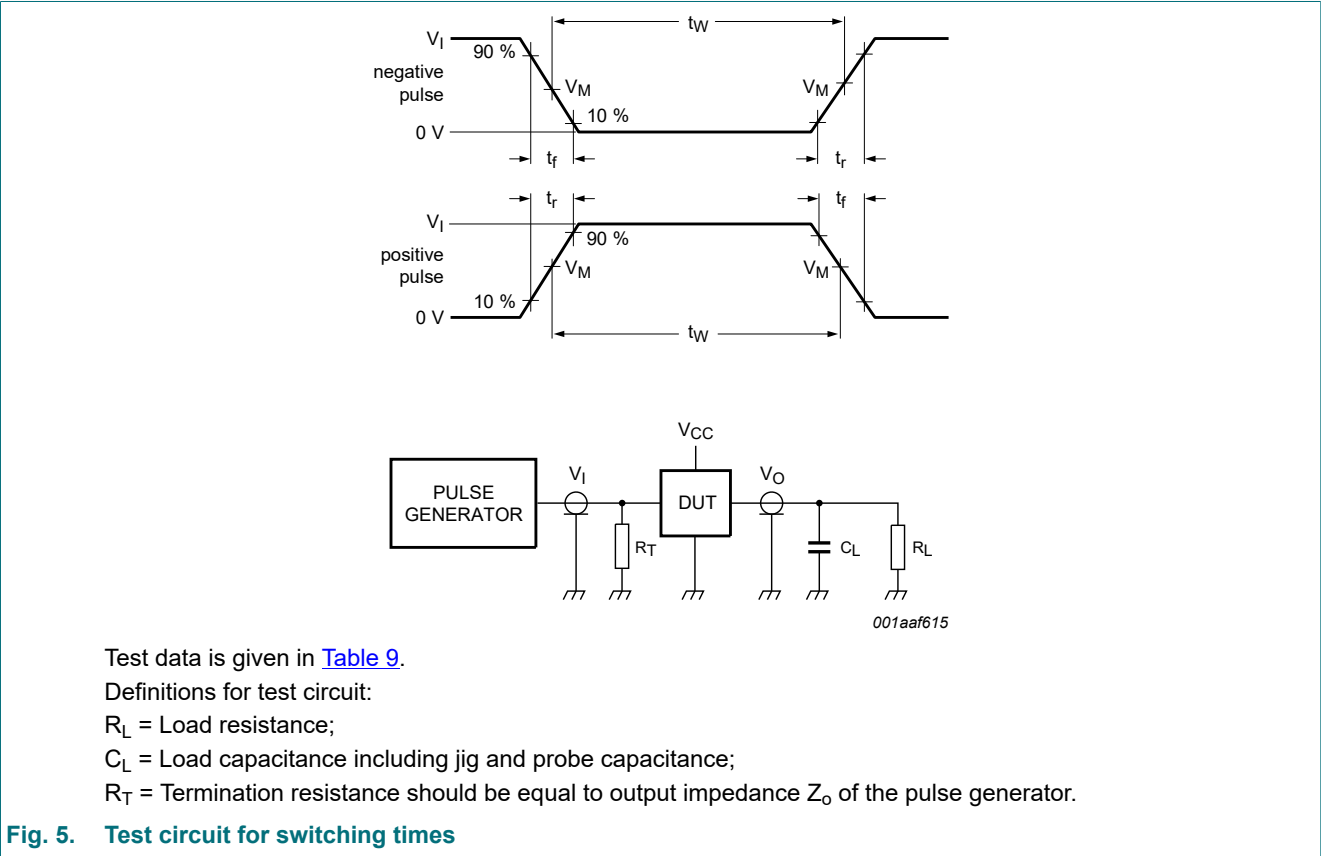


Fig. 5. Test circuit for switching times

Table 9. Test data

Supply voltage	Input		Load	
	V _I	t _r , t _f	C _L	R _L
1.2 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ
1.65 V to 1.95 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ
2.3 V to 2.7 V	V _{CC}	≤ 2 ns	30 pF	500 Ω
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

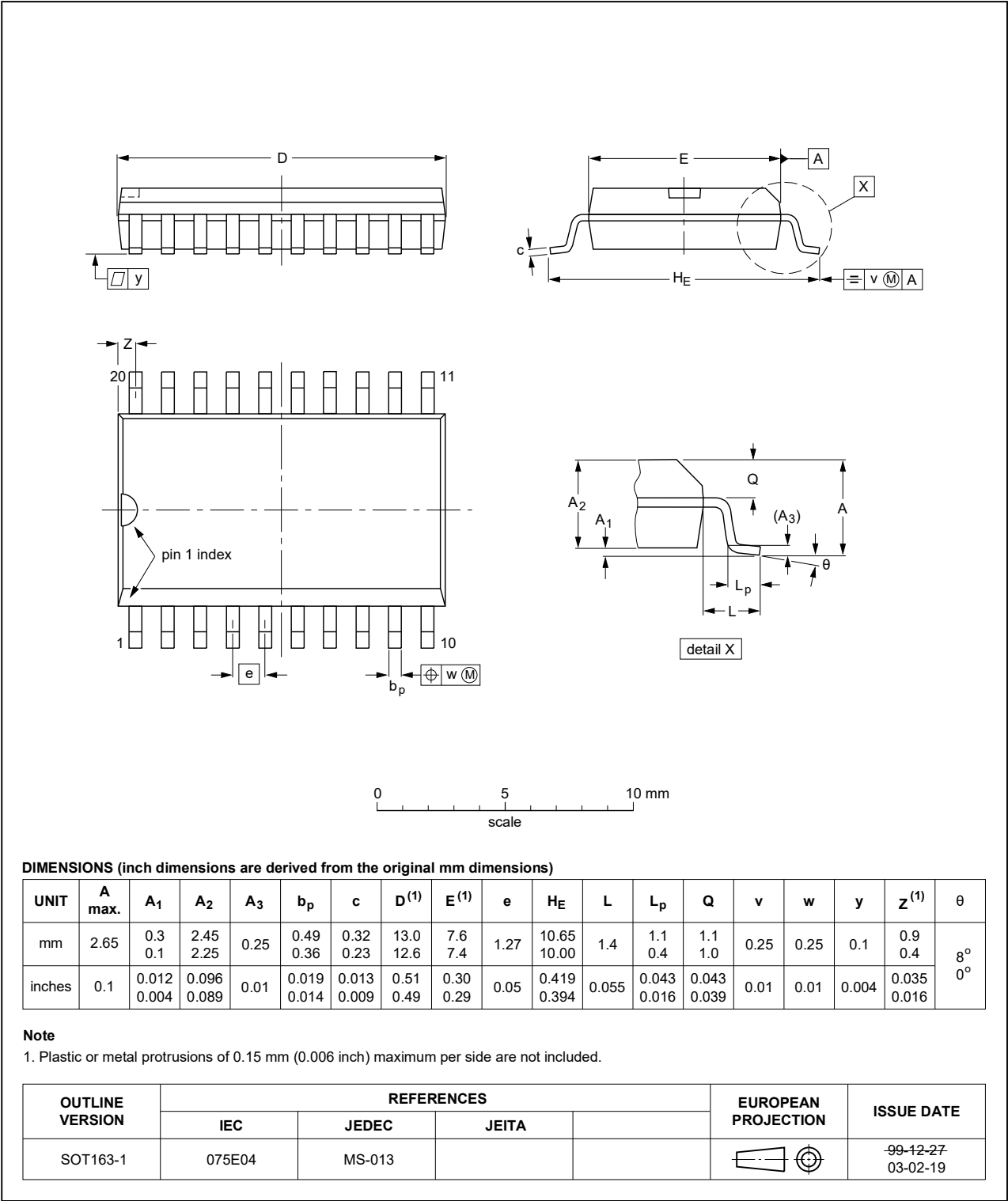


Fig. 6. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

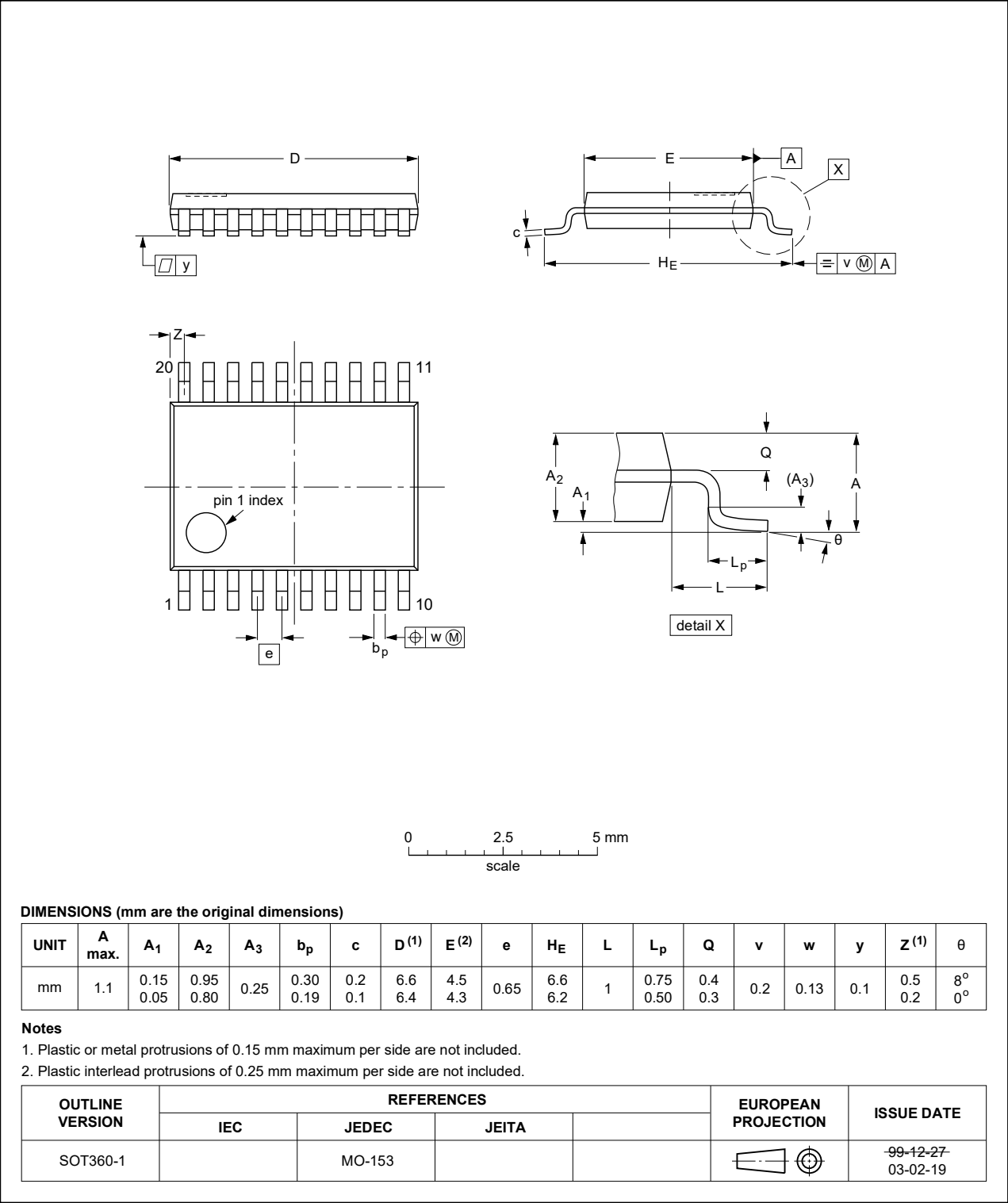


Fig. 7. Package outline SOT360-1 (TSSOP20)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC377 v.8	20230828	Product data sheet	-	74LVC377 v.7
Modifications:	Section 2: ESD specification updated according to the latest JEDEC standard.			
74LVC377 v.7	20210827	Product data sheet	-	74LVC377 v.6
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate. Section 1 updated. - Type number 74LVC377DB (SOT339-1/SSOP20) removed. Section 7: Derating values for P_{tot} total power dissipation updated.			
74LVC377 v.6	20121120	Product data sheet	-	74LVC377 v.5
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate. Table 4, Table 5, Table 6, Table 7, Table 8, and Table 9: values added for lower voltage ranges.			
74LVC377 v.5	20050221	Product specification	-	74LVC377 v.4
74LVC377 v.4	20040528	Product specification	-	74LVC377 v.3
74LVC377 v.3	20021023	Product specification	-	74LVC377 v.2
74LVC377 v.2	19980729	Product specification	-	74LVC377 v.1
74LVC377 v.1	19990606	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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