

DS90CP02 1.5 Gbps 2x2 LVDS Crosspoint Switch

Check for Samples: [DS90CP02](#)

FEATURES

- 1.5 Gbps per Channel
- Low Power: 70 mA in Dual Repeater Mode @1.5 Gbps
- Low Output Jitter
- Non-Blocking Architecture Allows 1:2 Splitter, 2:1 Mux, Crossover, and Dual Buffer Configurations
- Flow-Through Pinout
- LVDS/BLVDS/CML/LVPECL Inputs, LVDS Outputs
- Single 3.3V Supply
- Separate Control of Inputs and Outputs Allows for Power Savings
- Industrial -40 to +85°C Temperature Range
- 28-lead UQFN-28 Space Saving Package

DESCRIPTION

The DS90CP02 is a 1.5 Gbps 2 x 2 LVDS crosspoint switch optimized for high-speed signal routing and switching over lossy FR-4 printed circuit board backplanes and balanced cables. Fully differential signal paths ensure exceptional signal integrity and noise immunity. The non-blocking architecture allows connections of any input to any output or outputs.

Wide input common mode range allows the switch to accept signals with LVDS, CML and LVPECL levels; the output levels are LVDS. A very small package footprint requires a minimal space on the board while the flow-through pinout allows easy board layout. The 3.3V supply, CMOS process, and LVDS I/O ensure high performance at low power over the entire industrial -40 to +85°C temperature range.

Block Diagram

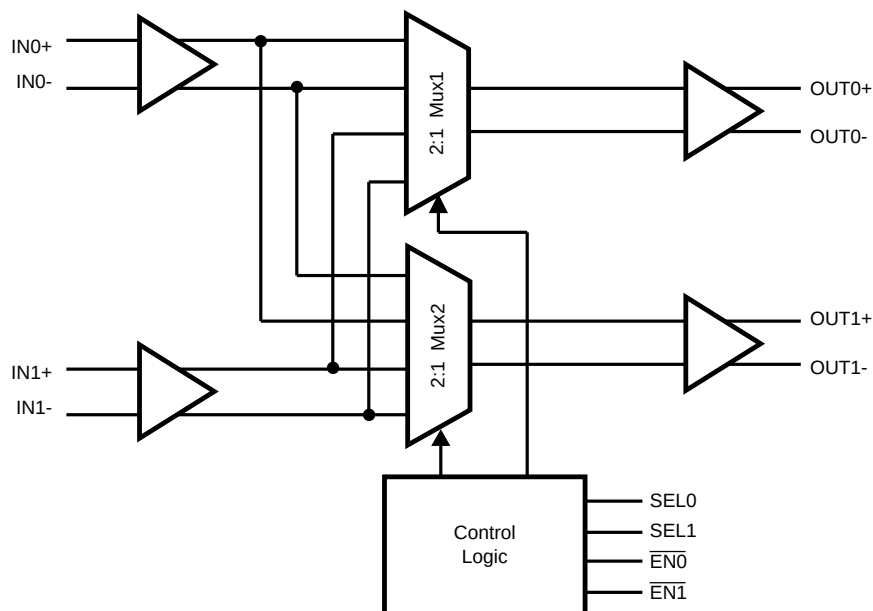


Figure 1. DS90CP02 Block Diagram



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Table 1. PIN DESCRIPTIONS

Pin Name	Pin Number	I/O, Type	Description
DIFFERENTIAL INPUTS COMMON TO ALL MUXES			
IN0+ IN0–	9 10	I, LVDS	Inverting and non-inverting differential inputs. LVDS, Bus LVDS, CML, or LVPECL compatible.
IN1+ IN1–	12 13	I, LVDS	Inverting and non-inverting differential inputs. LVDS, Bus LVDS, CML, or LVPECL compatible.
SWITCHED DIFFERENTIAL OUTPUTS			
OUT0+ OUT0–	27 26	O, LVDS	Inverting and non-inverting differential outputs. OUT0± can be connected to any one pair IN0±, or IN1±. LVDS compatible .
OUT1+ OUT1–	24 23	O, LVDS	Inverting and non-inverting differential outputs. OUT1± can be connected to any one pair IN0±, or IN1±. LVDS compatible .
DIGITAL CONTROL INTERFACE			
SEL0, SEL1	6 5	I, LVTTTL	Select Control Inputs
EN0, EN1	7 15	I, LVTTTL	Output Enable Inputs
N/C	8, 20, 28		Not Connected
POWER			
V _{DD}	11, 14, 16, 18, 19, 22, 25	I, Power	V _{DD} = 3.3V ±0.3V. At least 4 low ESR 0.01 µF bypass capacitors should be connected from V _{DD} to GND plane.
GND	DAP, 1, 2, 3, 4, 17, 21	I, Power	Ground reference to LVDS and CMOS circuitry. For the UQFN package, the DAP is used as the primary GND connection to the device. The DAP is the exposed metal contact at the bottom of the UQFN-28 package. It should be connected to the ground plane with at least 4 vias for optimal AC and thermal performance.

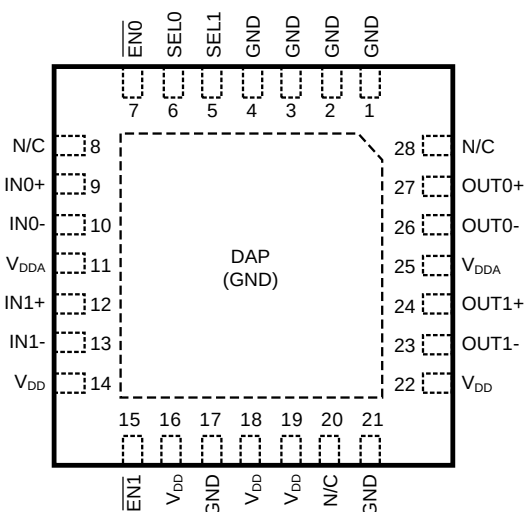
Connection Diagram

Figure 2. UQFN Top View
DAP = GND
See Package Number NJD0028A

Configuration Select Truth Table

SEL0	SEL1	$\overline{\text{EN0}}$	$\overline{\text{EN1}}$	OUT0	OUT1	Mode
0	0	0	0	IN0	IN0	1:2 Splitter (IN1 powered down)
0	1	0	0	IN0	IN1	Dual Channel Repeater
1	0	0	0	IN1	IN0	Dual Channel Switch
1	1	0	0	IN1	IN1	1:2 Splitter (IN0 powered down)
0	1	0	1	IN0	PD	Single Channel Repeater (Channel 1 powered down)
1	1	0	1	IN1	PD	Single Channel Switch (IN0 and OUT1 powered down)
0	0	1	0	PD	IN0	Single Channel Switch (IN1 and OUT0 powered down)
0	1	1	0	PD	IN1	Single Channel Repeater (Channel 0 powered down)
X	X	1	1	PD	PD	Both Channels in Power Down Mode
0	0	0	1			Invalid State*
1	0	0	1			Invalid State*
1	0	1	0			Invalid State*
1	1	1	0			Invalid State*

APPLICATION INFORMATION

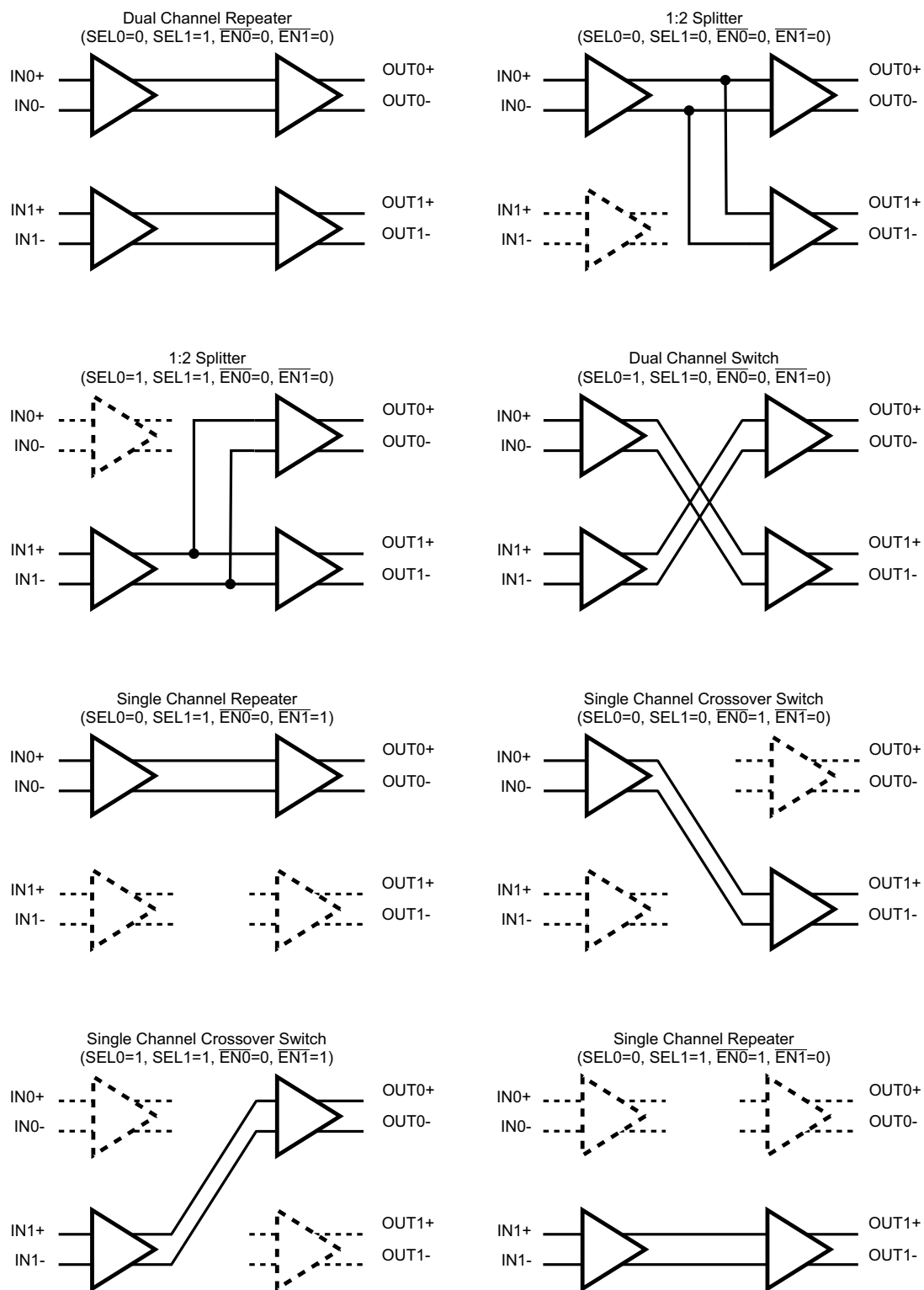


Figure 3. DS90CP02 Configuration Select Decode



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings ⁽¹⁾⁽²⁾

Supply Voltage (V_{DD})	–0.3V to +4.0V
CMOS Input Voltage	–0.3V to ($V_{DD} + 0.3V$)
LVDS Receiver Input Voltage	–0.3V to +3.6V
LVDS Driver Output Voltage	–0.3V to +3.6V
LVDS Output Short Circuit Current	40mA
Junction Temperature	+150°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 4sec.)	+260°C
Maximum Package Power Dissipation at 25°C	
UQFN-28	4.31 W
Derating above 25°C	
UQFN-28	34.5 mW/°C
Thermal Resistance, θ_{JA}	
UQFN-28	29°C/W
ESD Rating	
HBM, 1.5 k Ω , 100 pF	6.5 kV
EIAJ, 0 Ω , 200 pF	>250V

- (1) "Absolute Maximum Ratings" are the ratings beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

Recommended Operating Conditions

	Min	Typ	Max	Unit
Supply Voltage (V_{DD} – GND)	3.0	3.3	3.6	V
Receiver Input Voltage	0		3.6	V
Operating Free Air Temperature	–40	25	85	°C
Junction Temperature			150	°C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ (1)	Max	Units
LVTTTL DC SPECIFICATIONS (SEL0, SEL1, EN1, EN2)						
V _{IH}	High Level Input Voltage		2.0		V _{DD}	V
V _{IL}	Low Level Input Voltage		GND		0.8	V
I _{IH}	High Level Input Current	V _{IN} = V _{DD} = V _{DDMAX}	−10		+10	μA
I _{IL}	Low Level Input Current	V _{IN} = V _{SS} , V _{DD} = V _{DDMAX}	−10		+10	μA
C _{IN1}	Input Capacitance	Any Digital Input Pin to V _{SS}		3.5		pF
V _{CL}	Input Clamp Voltage	I _{CL} = −18 mA	−1.5	−0.8		V
LVDS INPUT DC SPECIFICATIONS (IN0±, IN1±)						
V _{TH}	Differential Input High Threshold ⁽²⁾	V _{CM} = 0.8V or 1.2V or 3.55V, V _{DD} = 3.6V		0	100	mV
V _{TL}	Differential Input Low Threshold	V _{CM} = 0.8V or 1.2V or 3.55V, V _{DD} = 3.6V	−100	0		mV
V _{ID}	Differential Input Voltage	V _{CM} = 0.8V to 3.55V, V _{DD} = 3.6V	100			mV
V _{CMR}	Common Mode Voltage Range	V _{ID} = 150 mV, V _{DD} = 3.6V	0.05		3.55	V
C _{IN2}	Input Capacitance	IN+ or IN− to V _{SS}		3.5		pF
I _{IN}	Input Current	V _{IN} = 3.6V, V _{DD} = V _{DDMAX} or 0V	−10		+10	μA
		V _{IN} = 0V, V _{DD} = V _{DDMAX} or 0V	−10		+10	μA
LVDS OUTPUT DC SPECIFICATIONS (OUT0±, OUT1±)						
V _{OD}	Differential Output Voltage, 0% Pre-emphasis ⁽²⁾	R _L = 100Ω between OUT+ and OUT−	250	400	575	mV
ΔV _{OD}	Change in V _{OD} between Complementary States		−35		35	mV
V _{OS}	Offset Voltage ⁽³⁾		1.09	1.25	1.475	V
ΔV _{OS}	Change in V _{OS} between Complementary States		−35		35	mV
I _{OS}	Output Short Circuit Current, One Complementary Output	OUT+ or OUT− Short to GND		−60	−90	mA
C _{OUT}	Output Capacitance	OUT+ or OUT− to GND when TRI-STATE		5.5		pF
SUPPLY CURRENT (Static)						
I _{CC0}	Supply Current	All inputs and outputs enabled and active, terminated with differential load of 100Ω between OUT+ and OUT−.		42	60	mA
I _{CC1}	Supply Current - one channel powered down	Single channel crossover switch or single channel repeater modes (1 channel active, one channel in power down mode)		22	30	mA
I _{CC2}	Supply Current - one input powered down	Splitter mode (One input powered down, both outputs active)		30	40	mA
I _{CCZ}	TRI-STATE Supply Current	Both input/output Channels in Power Down Mode		1.4	2.5	mA
SWITCHING CHARACTERISTICS—LVDS OUTPUTS (Figure 4, Figure 5)						
t _{LHT}	Differential Low to High Transition Time	Use an alternating 1 and 0 pattern at 200 Mb/s, measure between 20% and 80% of V _{OD} .	70	150	215	ps
t _{HLT}	Differential High to Low Transition Time		50	135	180	ps
t _{PLHD}	Differential Low to High Propagation Delay	Use an alternating 1 and 0 pattern at 200 Mb/s, measure at 50% V _{OD} between input to output.	0.5	2.4	3.5	ns
t _{PHLD}	Differential High to Low Propagation Delay		0.5	2.4	3.5	ns
t _{SKD1}	Pulse Skew	t _{PLHD} − t _{PHLD}		55	120	ps

(1) Typical parameters are measured at $V_{DD} = 3.3\text{V}$, $T_A = 25^\circ\text{C}$. They are for reference purposes, and are not production-tested.

(2) Differential output voltage V_{OD} is defined as $\text{ABS}(OUT+ - OUT-)$. Differential input voltage V_{ID} is defined as $\text{ABS}(IN+ - IN-)$.

(3) Output offset voltage V_{OS} is defined as the average of the LVDS single-ended output voltages at logic high and logic low states.

Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ (1)	Max	Units
t_{SKCC}	Output Channel to Channel Skew	Difference in propagation delay (t_{PLHD} or t_{PHLD}) among all output channels in Splitter mode (any one input to all outputs).	0	130	315	ps
t_{JIT}	Jitter (4)	RJ - Clock Pattern 750 MHz (5)		1.4	2.5	psrms
		DJ - K28.5 Pattern 1.5 Gbps (6)		42	75	psp-p
		TJ - PRBS $2^{23}-1$ Pattern 1.5 Gbps (7)		93	126	psp-p
t_{ON}	LVDS Output Enable Time	Time from $\overline{ENx}$ to $OUT\pm$ change from TRI-STATE to active.	50	110	150	ns
t_{OFF}	LVDS Output Disable Time	Time from $\overline{ENx}$ to $OUT\pm$ change from active to TRI-STATE.		5	12	ns
t_{SW}	LVDS Switching Time SELx to $OUT\pm$	Time from configuration select (SELx) to new switch configuration effective for $OUT\pm$.		110	150	ns

(4) Jitter is not production tested, but guaranteed through characterization on a sample basis.

(5) Random Jitter, or RJ, is measured RMS with a histogram including 1500 histogram window hits. The input voltage = $V_{ID} = 500mV$, 50% duty cycle at 750MHz, $t_r = t_f = 50ps$ (20% to 80%).

(6) Deterministic Jitter, or DJ, is measured to a histogram mean with a sample size of 350 hits. The input voltage = $V_{ID} = 500mV$, K28.5 pattern at 1.5 Gbps, $t_r = t_f = 50ps$ (20% to 80%). The K28.5 pattern is repeating bit streams of (0011111010 1100000101).

(7) Total Jitter, or TJ, is measured peak to peak with a histogram including 3500 window hits. Stimulus and fixture jitter has been subtracted. The input voltage = $V_{ID} = 500mV$, $2^{23}-1$ PRBS pattern at 1.5 Gbps, $t_r = t_f = 50ps$ (20% to 80%).

Timing Diagrams

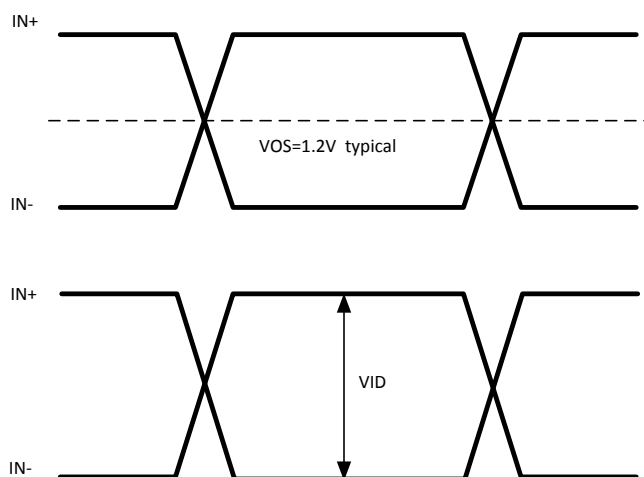


Figure 4. LVDS Signals

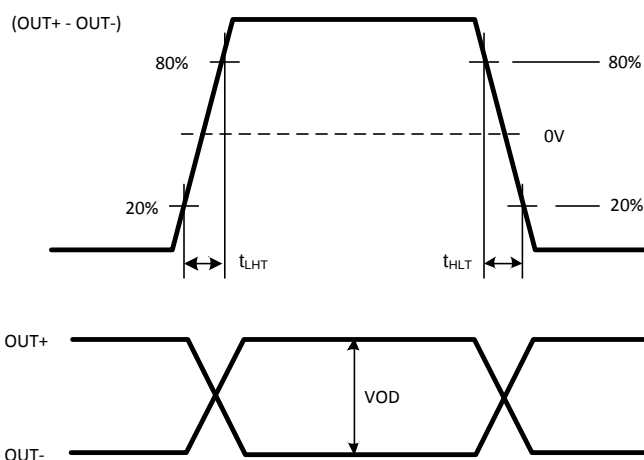


Figure 5. LVDS Output Transition Time

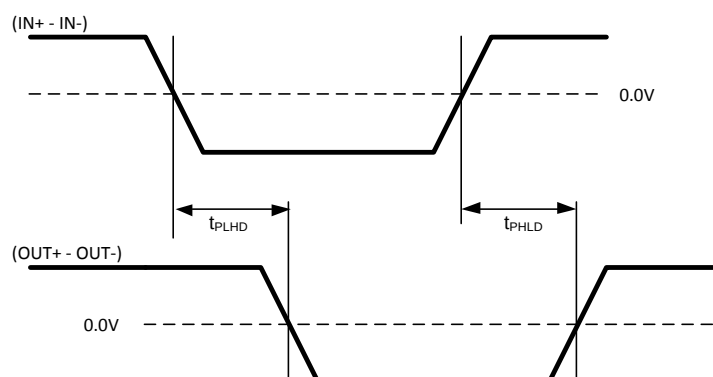


Figure 6. LVDS Output Propagation Delay

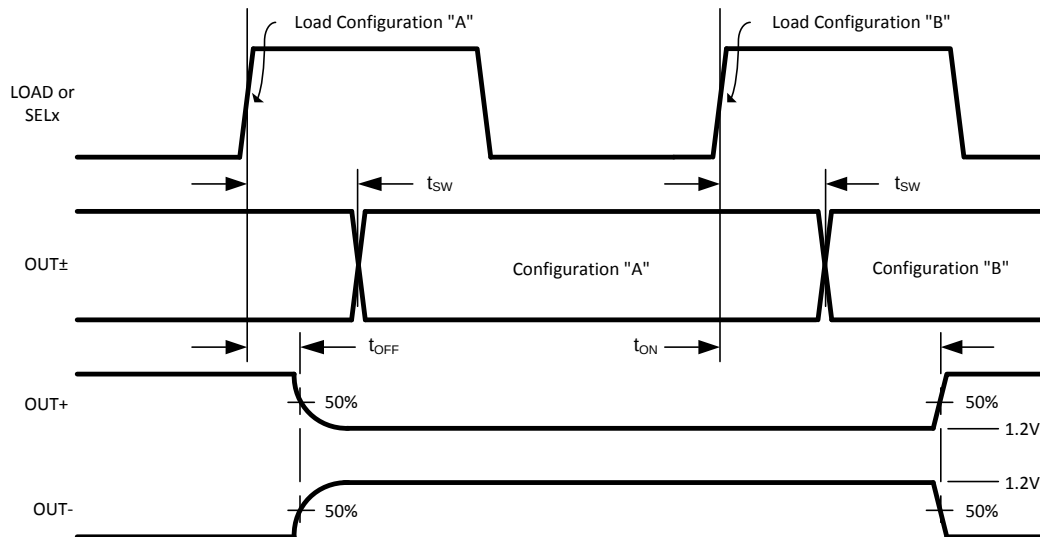
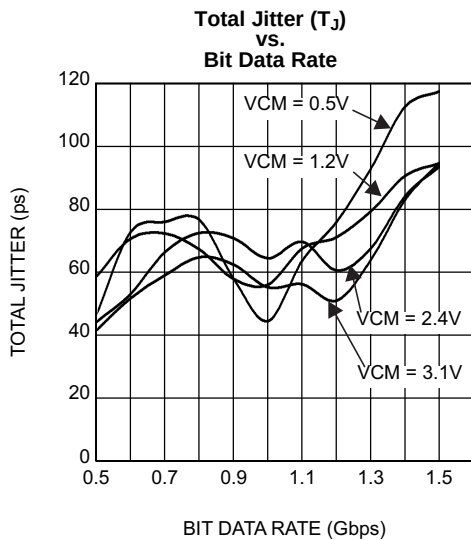


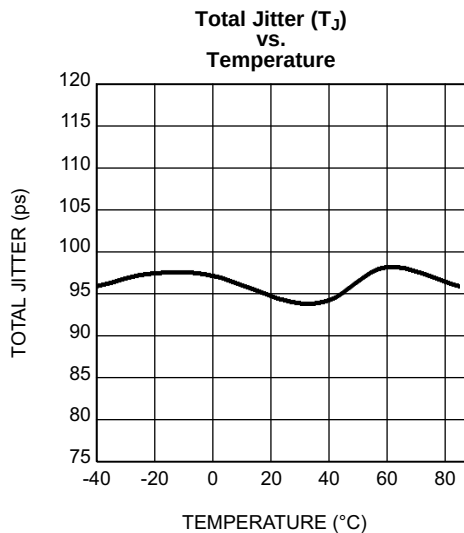
Figure 7. Configuration and Output Enable/Disable Timing

Typical Performance



Total Jitter measured at 0V differential while running a PRBS $2^{23}-1$ pattern in single channel repeater mode. $V_{CC} = 3.3V$, $T_A = +25^\circ C$, $V_{ID} = 0.5V$

Figure 8.



Total Jitter measured at 0V differential while running a PRBS $2^{23}-1$ pattern in dual channel repeater mode. $V_{CC} = 3.3V$, $V_{ID} = 0.5V$, $V_{CM} = 1.2V$, 1.5 Gbps data rate

Figure 9.

REVISION HISTORY

Changes from Original (March 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	9

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS90CP02SP/NOPB	Active	Production	UQFN (NJD) 28	1000 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	CP02SP
DS90CP02SP/NOPB.A	Active	Production	UQFN (NJD) 28	1000 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	CP02SP

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

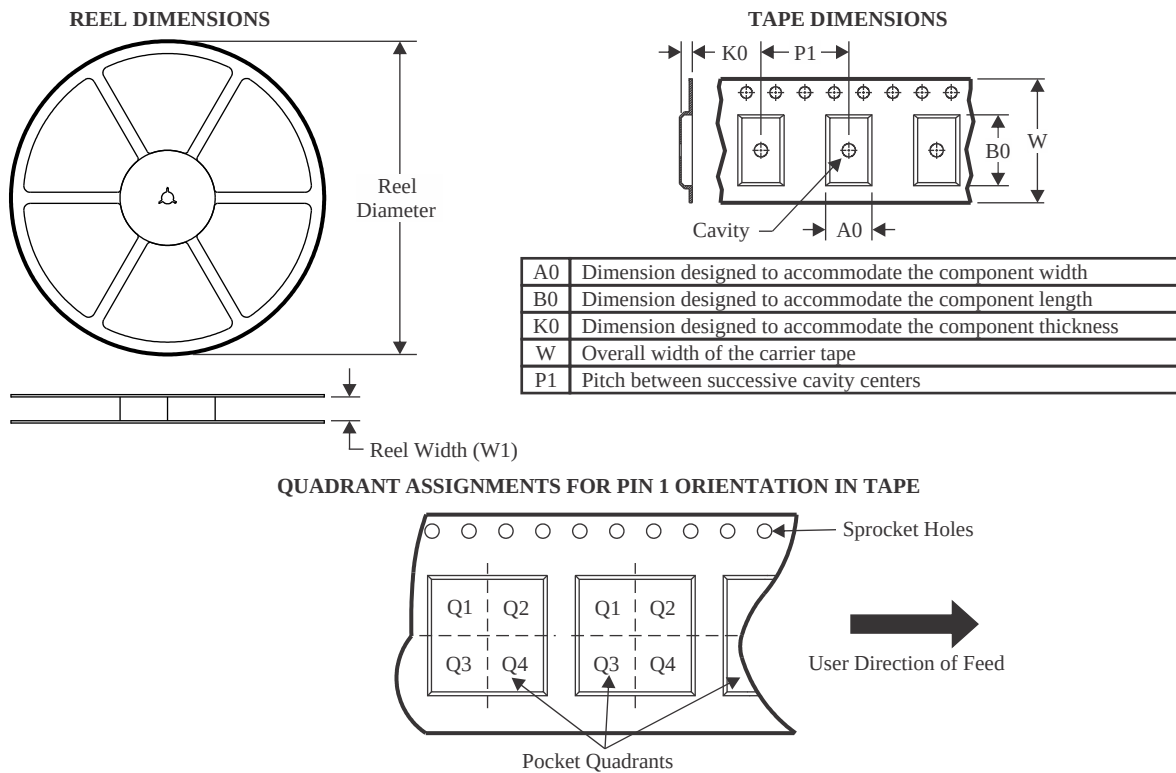
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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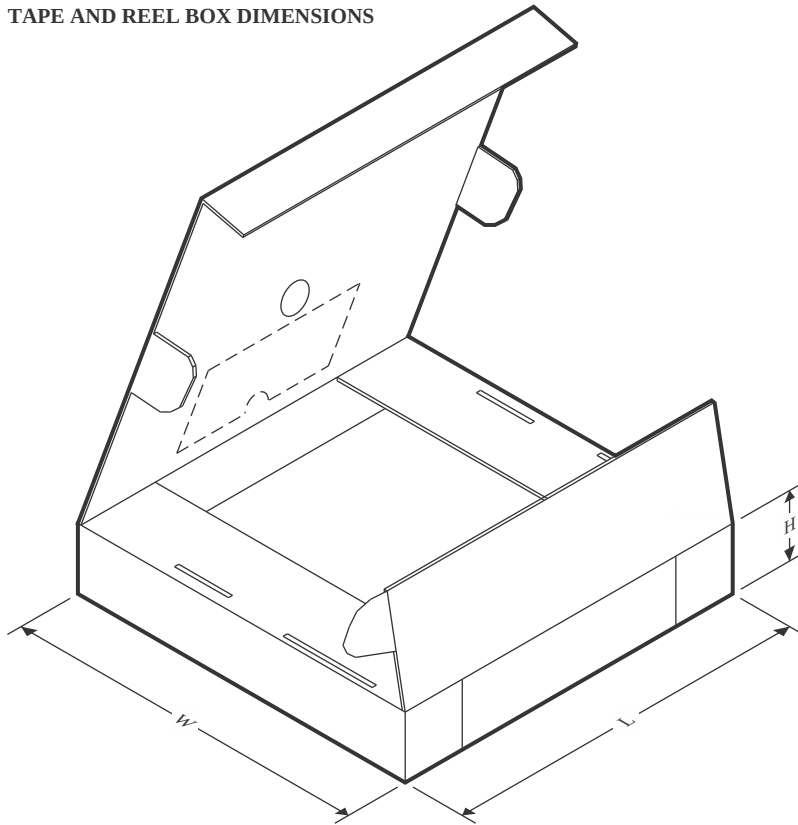
TAPE AND REEL INFORMATION



*All dimensions are nominal

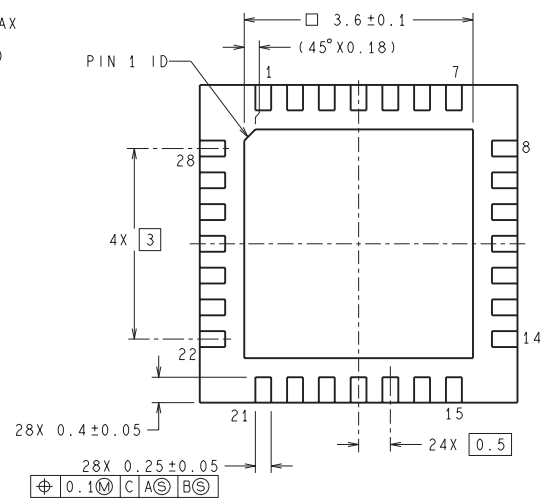
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90CP02SP/NOPB	UQFN	NJD	28	1000	177.8	12.4	5.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90CP02SP/NOPB	UQFN	NJD	28	1000	208.0	191.0	35.0



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