



74HC157; 74HCT157

Quad 2-input multiplexer

Rev. 10 — 28 May 2024

Product data sheet

1. General description

The 74HC157; 74HCT157 is a quad 2-input multiplexer. The device features select (S) and enable $\bar{E}$ inputs. A HIGH on S selects data source 1, a LOW data source 0. A HIGH on $\bar{E}$ forces all the outputs (1Y to 4Y) LOW. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

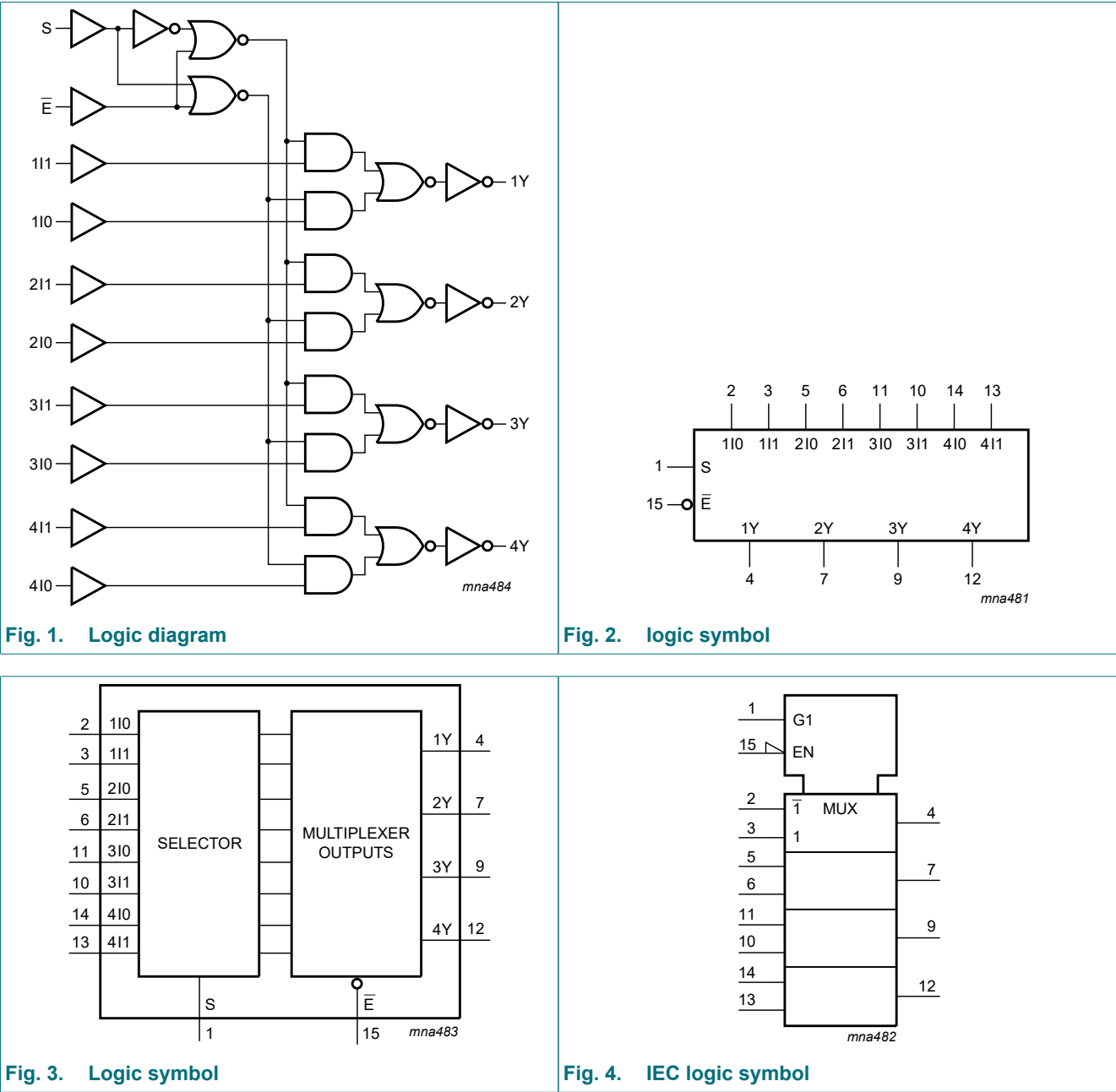
- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- Input levels:
 - For 74HC157: CMOS level
 - For 74HCT157: TTL level
- Non-inverting data path
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

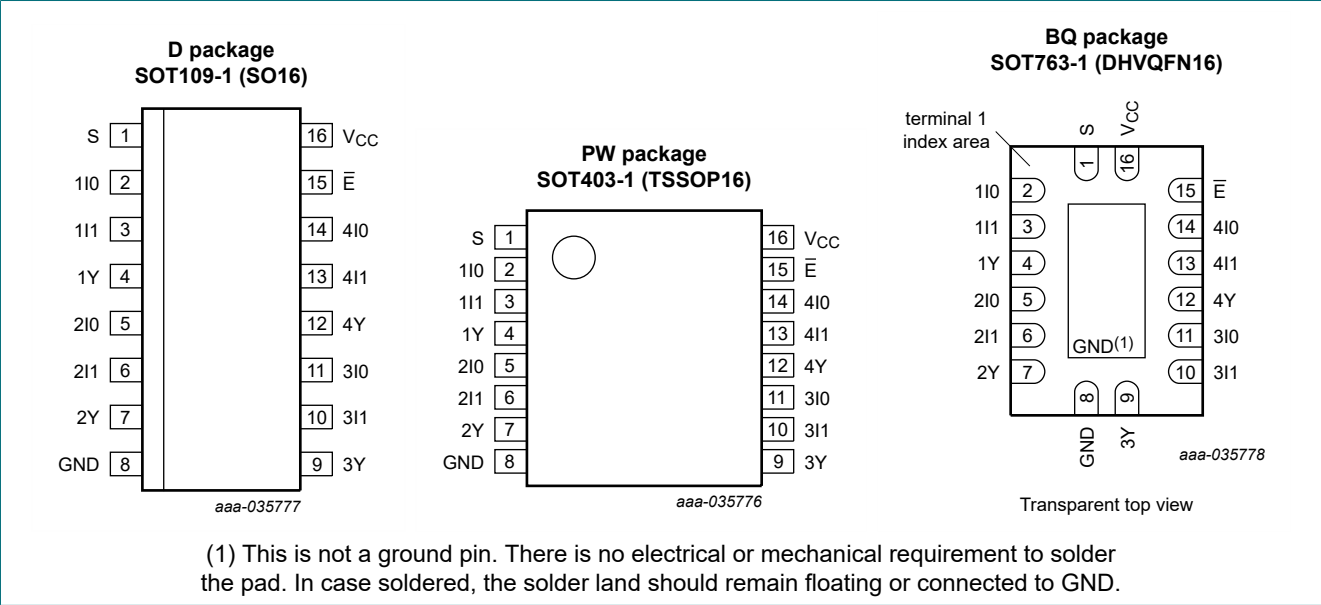
Type number	Package			
	Temperature range	Name	Description	Version
74HC157D 74HCT157D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC157PW 74HCT157PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC157BQ 74HCT157BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
S	1	common data select input
1I0 to 4I0	2, 5, 11, 14	data inputs from source 0
1I1 to 4I1	3, 6, 10, 13	data inputs from source 1
1Y to 4Y	4, 7, 9, 12	multiplexer outputs
GND	8	ground (0 V)
$\overline{E}$	15	enable input (active LOW)
V _{CC}	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input				Output
$\overline{E}$	S	nI0	nI1	nY
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	-	±20	mA
I _O	output current	V _O = -0.5 V to V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	+50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [1]	-	500	mW

- [1] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC157			74HCT157			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +85 °C		T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC157										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -20 µA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 µA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 µA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80	-	160	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +85 °C		T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT157										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	8.0	-	80	-	160	µA
ΔI _{CC}	additional supply current	V _I = V _{CC} - 2.1 V; I _O = 0 A; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V								
		per input pin; nI0, nI1 inputs	-	100	360	-	450	-	490	µA
		per input pin; $\overline{E}$ input	-	60	216	-	270	-	294	µA
		per input pin; S input	-	100	360	-	450	-	490	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

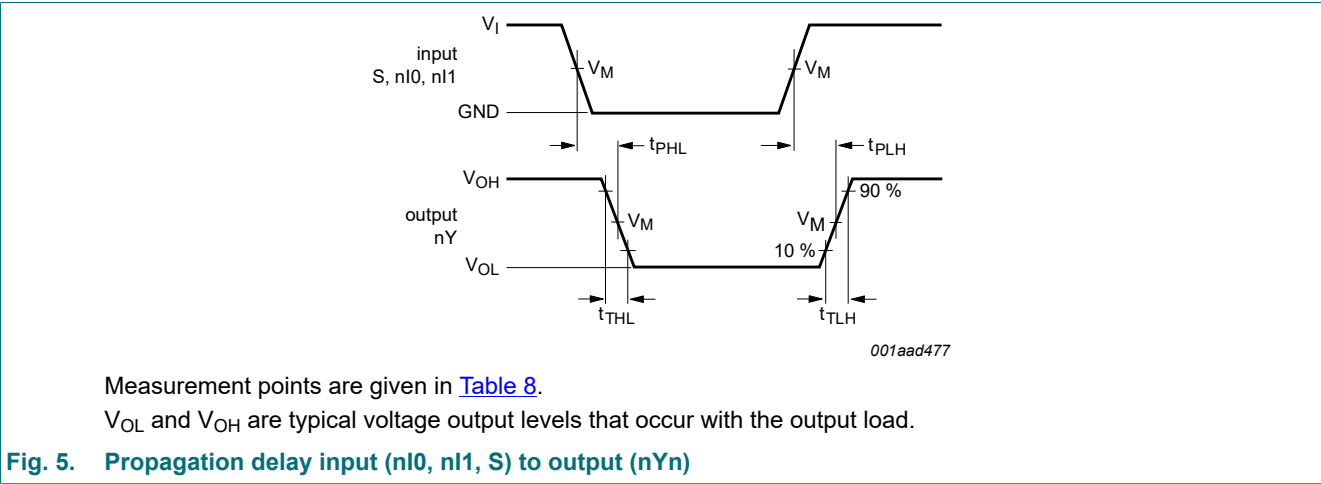
Voltages are referenced to GND (ground = 0 V); $C_L = 50\text{ pF}$ unless otherwise specified; for test circuit see Fig. 7.

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +85 °C		T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC157										
t _{pd}	propagation delay	nI0, nI1 to nY; see Fig. 5 [1]								
		V _{CC} = 2.0 V	-	36	125	-	155	-	190	ns
		V _{CC} = 4.5 V	-	13	25	-	31	-	38	ns
		V _{CC} = 5 V; C _L = 15 pF	-	11	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	10	21	-	26	-	32	ns
		S to nY; see Fig. 5 [1]								
		V _{CC} = 2.0 V	-	41	125	-	155	-	190	ns
		V _{CC} = 4.5 V	-	15	25	-	31	-	38	ns
		V _{CC} = 5 V; C _L = 15 pF	-	12	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	12	21	-	26	-	32	ns
		$\bar{E}$ to nY; see Fig. 6 [1]								
		V _{CC} = 2.0 V	-	39	115	-	145	-	175	ns
		V _{CC} = 4.5 V	-	14	23	-	29	-	35	ns
		V _{CC} = 5 V; C _L = 15 pF	-	11	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	11	20	-	25	-	30	ns
t _t	transition time	nY; see Fig. 5 [2]								
		V _{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	16	-	19	ns
C _{PD}	power dissipation capacitance	C _L = 50 pF; f = 1 MHz; V _I = GND to V _{CC} [3]	-	70	-	-	-	-	-	pF

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +85 °C		T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT157										
t _{pd}	propagation delay	nI0, nI1 to nY; see Fig. 5 [1]								
		V _{CC} = 4.5 V	-	16	27	-	34	-	41	ns
		V _{CC} = 5 V; C _L = 15 pF	-	13	-	-	-	-	-	ns
		S to nY; see Fig. 5 [1]								
		V _{CC} = 4.5 V	-	22	37	-	46	-	56	ns
		V _{CC} = 5 V; C _L = 15 pF	-	19	-	-	-	-	-	ns
		E to nY; see Fig. 6 [1]								
		V _{CC} = 4.5 V	-	15	26	-	33	-	39	ns
	V _{CC} = 5 V; C _L = 15 pF	-	12	-	-	-	-	-	ns	
t _t	transition time	nY; see Fig. 5 [2]								
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
C _{PD}	power dissipation capacitance	C _L = 50 pF; f = 1 MHz; V _I = GND to V _{CC} - 1.5 V [3]	-	70	-	-	-	-	-	pF

- [1] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [2] t_t is the same as t_{THL} and t_{TLH}.
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit



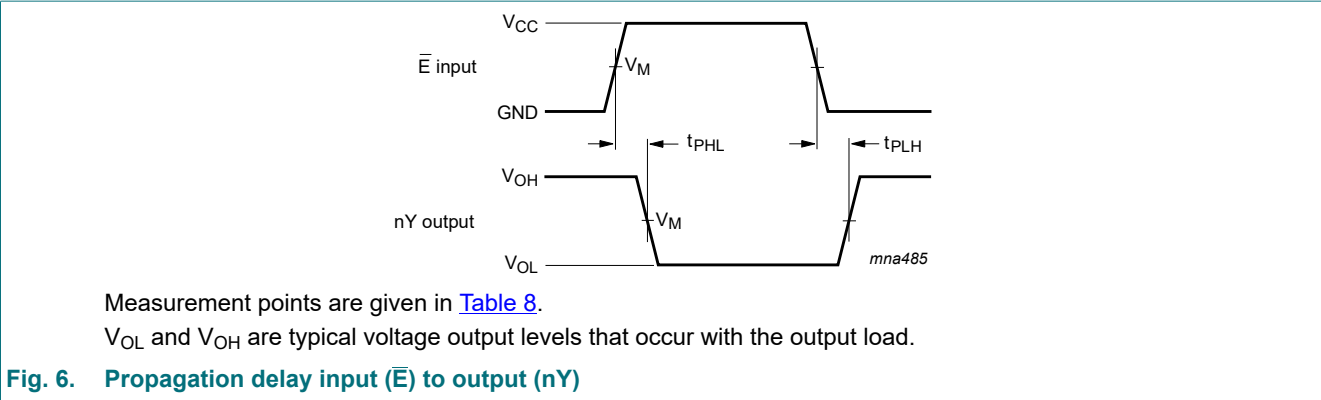


Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74HC157	$0.5V_{CC}$	$0.5V_{CC}$
74HCT157	1.3 V	1.3 V

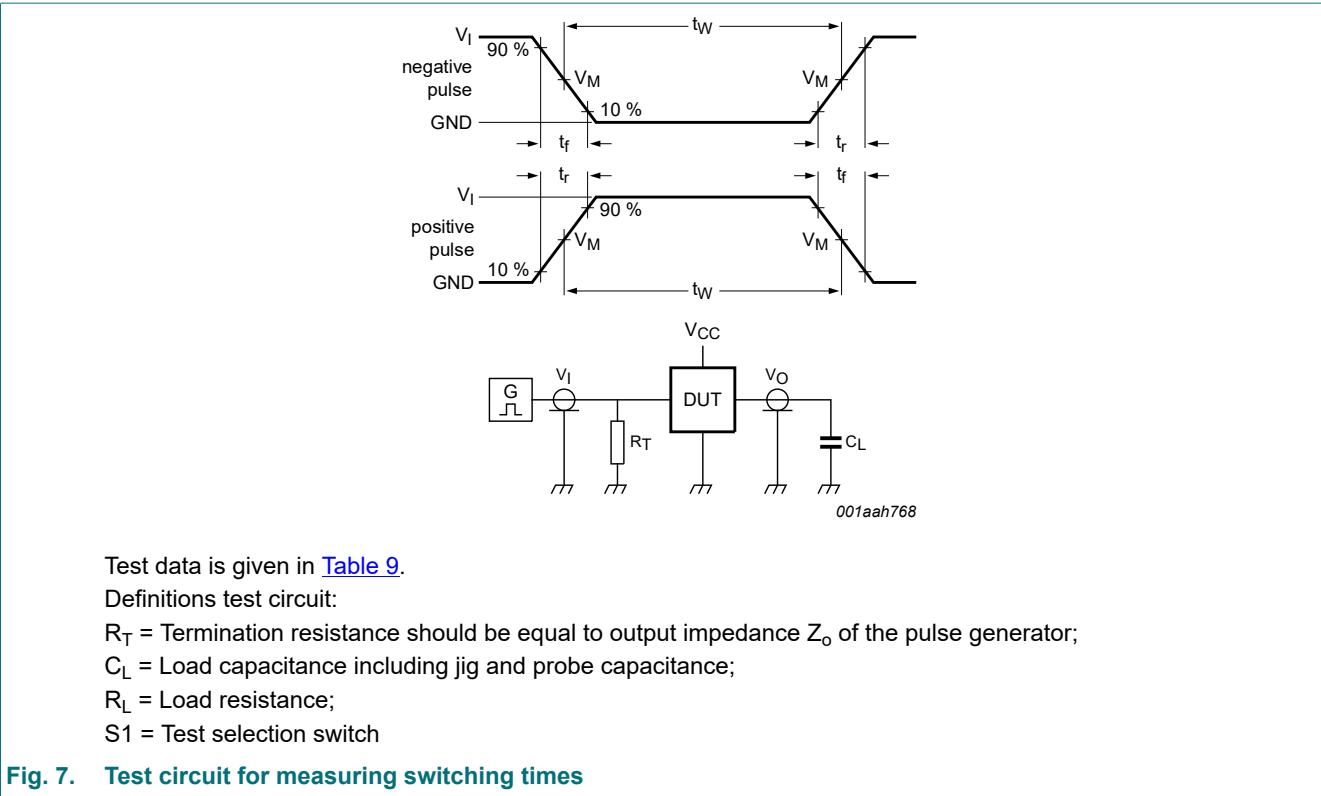


Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74HC157	V_{CC}	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74HCT157	3.0 V	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

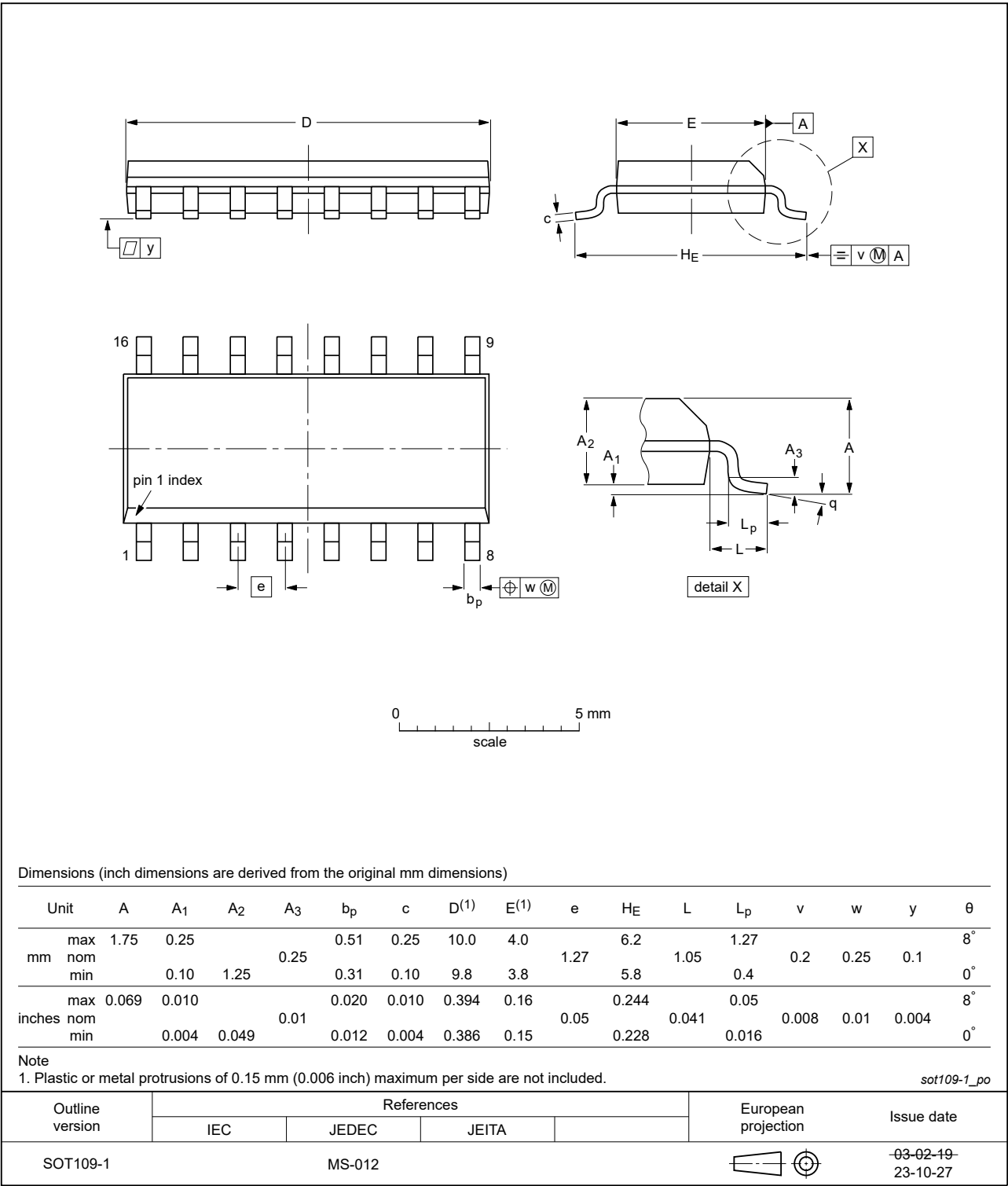


Fig. 8. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

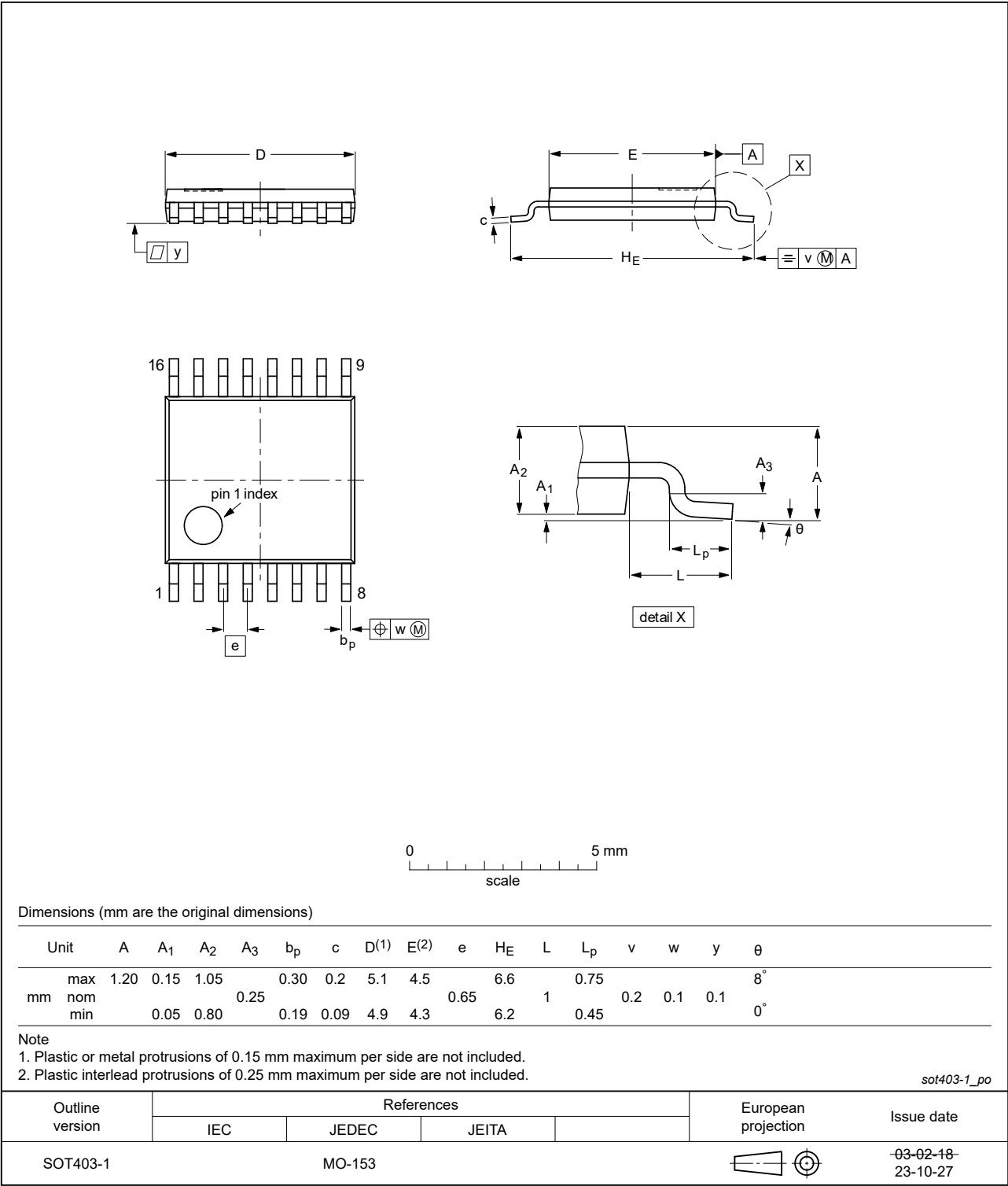


Fig. 9. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

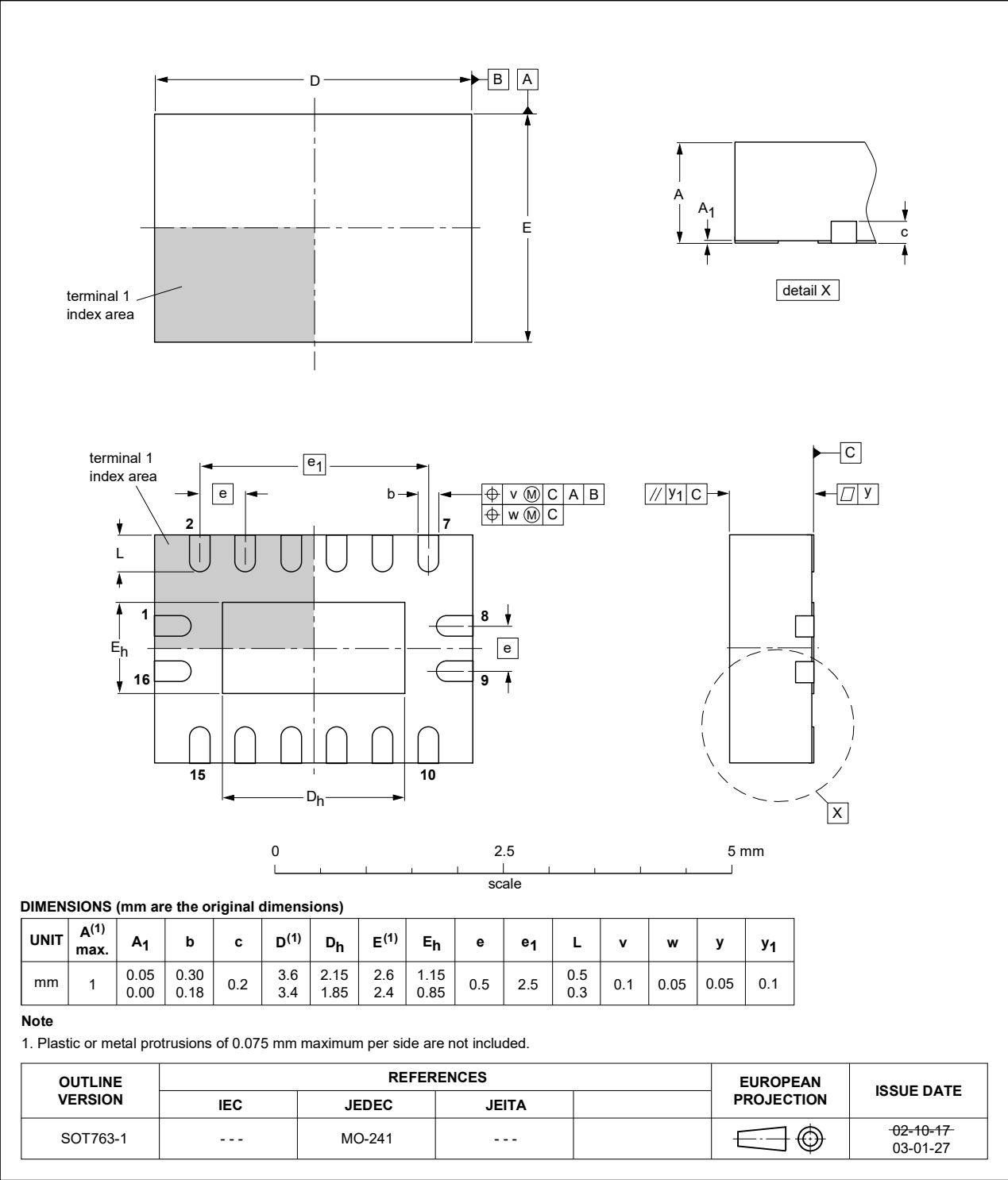


Fig. 10. Package outline SOT763-1 (DHVQFN16)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT157 v.10	20240528	Product data sheet	-	74HC_HCT157 v.9
Modifications:	Fig. 8, Fig. 9: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153. Section 2: ESD specification updated according to the latest JEDEC standard.			
74HC_HCT157 v.9	20200724	Product data sheet	-	74HC_HCT157 v.8
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate. - Type number 74HC157DB and 74HCT157DB (SOT338-1/SSOP16) removed. Section 1 and Section 2 updated. Table 4: Derating values for P_{tot} total power dissipation have been updated.			
74HC_HCT157 v.8	20151228	Product data sheet	-	74HC_HCT157 v.7
Modifications:	Type numbers 74HC157N and 74HCT157N (SOT38-4) removed.			
74HC_HCT157 v.7	20150121	Product data sheet	-	74HC_HCT157 v.6
Modifications:	Table 7: Power dissipation capacitance condition for 74HCT157 is corrected.			
74HC_HCT157 v.6	20120827	Product data sheet	-	74HC_HCT157 v.5
Modifications:	Package outline drawing DIP16 added.			
74HC_HCT157 v.5	20120425	Product data sheet	-	74HC_HCT157 v.4
Modifications:	Fig. 5 updated with transition times.			
74HC_HCT157 v.4	20111219	Product data sheet	-	74HC_HCT157 v.3
74HC_HCT157 v.3	20101231	Product data sheet	-	74HC_HCT157_CNV v.2
74HC_HCT157_CNV v.2	19970827	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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