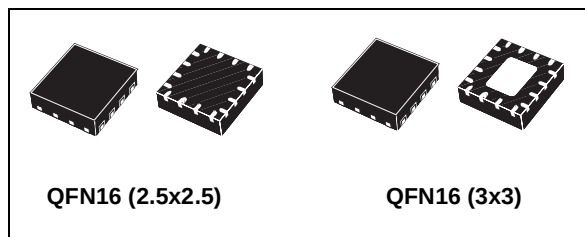


LOW VOLTAGE 0.5Ω MAX QUAD SPDT SWITCH WITH BREAK-BEFORE-MAKE FEATURE

- **HIGH SPEED:**
 $t_{PD} = 1.5\text{ns}$ (TYP.) at $V_{CC} = 3.0\text{V}$
 $t_{PD} = 1.5\text{ns}$ (TYP.) at $V_{CC} = 2.3\text{V}$
- **ULTRA LOW POWER DISSIPATION:**
 $I_{CC} = 0.2\mu\text{A}$ (MAX.) at $T_A = 85^\circ\text{C}$
- **LOW "ON" RESISTANCE $V_{IN}=0\text{V}$:**
 $R_{ON} = 0.5\Omega$ (MAX. $T_A = 25^\circ\text{C}$) at $V_{CC} = 2.7\text{V}$
 $R_{ON} = 0.7\Omega$ (MAX. $T_A = 25^\circ\text{C}$) at $V_{CC} = 2.3\text{V}$
 $R_{ON} = 1.5\Omega$ (MAX. $T_A = 25^\circ\text{C}$) at $V_{CC} = 1.8\text{V}$
- **WIDE OPERATING VOLTAGE RANGE:**
 V_{CC} (OPR) = 1.65V to 4.3V SINGLE SUPPLY
- **4.3V TOLERANT AND 1.8V COMPATIBLE THRESHOLD ON DIGITAL CONTROL INPUT** at $V_{CC} = 2.3$ to 3.0V
- **LATCH-UP PERFORMANCE EXCEEDS 300mA** (JESD 17)



Order Codes

PACKAGE	T & R
QFN16 (2.5x2.5)	STG3699AUTR
QFN16 (3x3)	STG3699AQTR

DESCRIPTION

The STG3699A is a high-speed CMOS low voltage quad analog S.P.D.T. (Single Pole/Dual Throw) switch or 2:1 Multiplexer/Demultiplexer Switch fabricated in silicon gate C²MOS technology. It is designed to operate from 1.65V to 4.3V, making this device ideal for portable applications.

It offers very low ON-Resistance ($R_{ON} < 0.5\Omega$) at $V_{CC} = 3.0\text{V}$. The n_{IN} inputs are provided to control the switches. The switches $nS1$ are ON (they are connected to common Ports D_n) when the n_{IN} input is held high and OFF (high impedance state exists

between the two ports) when n_{IN} is held low; the switches $nS2$ are ON (they are connected to common Ports D_n) when the n_{IN} input is held low and OFF (high impedance state exists between the two ports) when IN is held high. Additional key features are fast switching speed, Break-Before-Make delay time and ultra low power consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage. It is available in the commercial temperature range (-40 to 125°C) in QFN16 3x3mm, 2.5x2.5mm.

Table 1: Pin Connection (top through view)

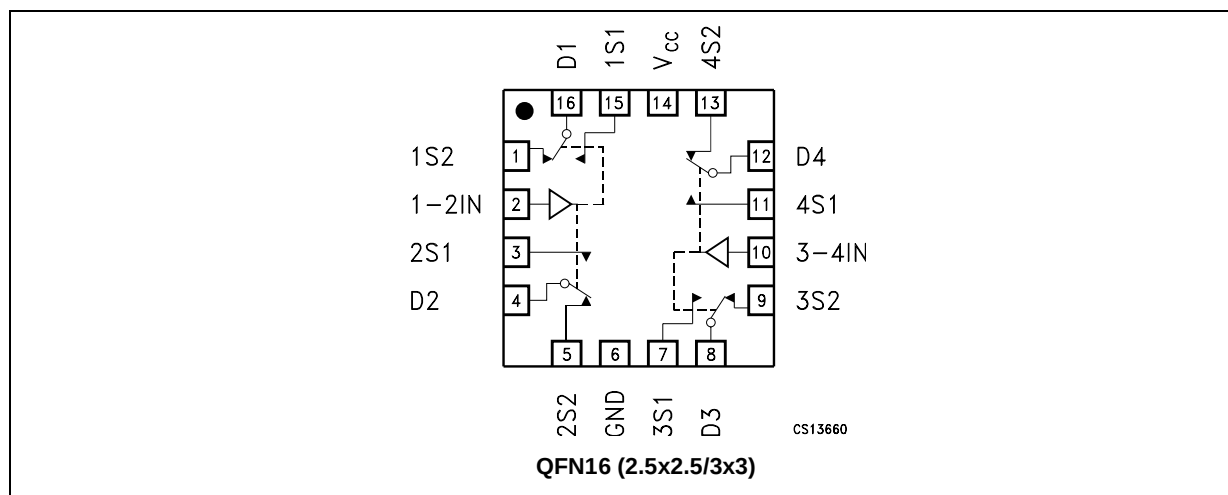


Figure 2: Input Equivalent Circuit

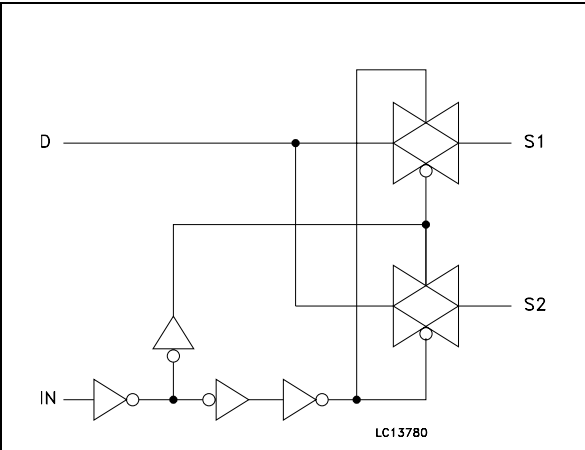


Table 2: Pin Description

PIN ⁽¹⁾ N°	SYMBOL	NAME AND FUNCTION
15, 3, 7, 11, 1, 5, 9, 13	1S1 to 4S1, 1S2 to 4S2	Independent Channels
16, 4, 8, 12	D1 to D4	Common Channels
2, 10	1-2IN, 3-4IN	Controls
14	V _{CC}	Positive Supply Voltage
6	GND	Ground (0V)

1. Exposed pad must be soldered to a floating plane. Do NOT connect to power or ground.

Table 3: Truth Table

1-2IN	3-4IN	ON Switches
L	-	1S2-D1, 2S2-D2
H	-	1S1-D1, 2S1-D2
-	L	3S2-D3, 4S2-D4
-	H	3S1-D3, 4S1-D4

Table 4: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to 5.5	V
V _I	DC Input Voltage	-0.5 to V _{CC} + 0.5	V
V _{IC}	DC Control Input Voltage	-0.5 to 5.5	V
V _O	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IKC}	DC Input Diode Current on control pin (V _{IN} < 0V)	- 50	mA
I _{IK}	DC Input Diode Current (V _{IN} < 0V)	± 50	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Current	± 300	mA
I _{OP}	DC Output Current Peak (pulse at 1ms, 10% duty cycle)	± 500	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 100	mA
P _D	Power Dissipation at T _a = 70°C (1)	1120	mW
T _{stg}	Storage Temperature	-65 to 150	°C
T _L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions not implied.

(1) Derate above 70°C: by 18.5mW/°C.

Table 5: Recommended Operating Conditions

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage (note 1)	1.65 to 4.3	V
V _I	Input Voltage	0 to V _{CC}	V
V _{IC}	Control Input Voltage	0 to 4.3	V
V _O	Output Voltage	0 to V _{CC}	V
T _{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time Control Input	V _{CC} = 1.65V to 2.7V	0 to 20
		V _{CC} = 3.0V to 4.3V	0 to 10

1) Truth Table guaranteed: 1.2V to 4.3V.

Table 6: DC Specifications

Symbol	Parameter	Test Conditions		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{IH}	High Level Input Voltage	1.65-1.95		0.65V _{CC}			0.65V _{CC}		0.65V _{CC}		V
		2.3-2.5		1.2			1.2		1.2		
		2.7-3.0		1.3			1.3		1.3		
		3.3		1.4			1.4		1.4		
		3.6		1.5			1.5		1.5		
		4.3		1.6			1.6		1.6		
V _{IL}	Low Level Input Voltage	1.65-1.95				0.25		0.25		0.25	V
		2.3-2.5				0.25		0.25		0.25	
		2.7-3.0				0.25		0.25		0.25	
		3.3				0.30		0.30		0.30	
		3.6				0.30		0.30		0.30	
		4.3				0.40		0.40		0.40	
R _{ON}	Switch ON Resistance	4.3	V _S =0V to V _{CC} I _S =100mA		0.35	0.45		0.50			Ω
		3.0			0.40	0.50		0.60			
		2.7			0.40	0.50		0.60			
		2.3			0.45	0.70		0.80			
		1.8			0.55	1.5		2.0			
		1.65			0.65	1.5		2.0			
ΔR _{ON}	ON Resistance Match between channels (1)	2.7	V _S @ R _{ON} Max I _S =100mA		0.06						Ω
R _{FLAT}	ON Resistance FLATNESS (2)	4.3	V _S =0V to V _{CC} I _S =100mA		0.15	0.20		0.20			Ω
		3.0			0.15	0.20		0.20			
		2.7			0.15	0.20		0.20			
		2.3			0.20	0.25		0.25			
		1.65			0.30	0.35		0.35			
I _{OFF}	OFF State Leakage Current (nSn), (Dn)	4.3	V _S =0.3 or 4V			±20		± 100			nA
I _{IN}	Input Leakage Current	0 - 4.3	V _{IN} = 0 to 4.3V			±0.1		± 1			μA
I _{CC}	Quiescent Supply Current	1.65-4.3	V _{IN} =V _{CC} or GND			±0.05		±0.2		±1	μA
I _{CCLV}	Quiescent Supply Current Low Voltage Driving	4.3	V _{1-2IN} , V _{3-4IN} = 1.65V		±37	±50		±100			μA
			V _{1-2IN} , V _{3-4IN} = 1.80V		±33	±40		±50			
			V _{1-2IN} , V _{3-4IN} = 2.60V		±12	±20		±30			

Note 1: ΔR_{ON} = R_{ON(MAX)} - R_{ON(MIN)}.

Note 2: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.



Table 7: AC Electrical Characteristics ($C_L = 35\text{pF}$, $R_L = 50\Omega$, $t_r = t_f \leq 5\text{ns}$)

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t _{PLH} , t _{PHL}	Propagation Delay	1.65-1.95	V _I =OPEN		0.45						ns
		2.3-2.7			0.40						
		3.0-3.3			0.30						
		3.6-4.3			0.30						
t _{ON}	TURN-ON time	1.65-1.95	V _S =0.8V		120						ns
		2.3-2.7	V _S =1.5V		45	55		65			
		3.0-3.3			42	55		65			
		3.6-4.3			40	55		65			
t _{OFF}	TURN-OFF time	1.65-1.95	V _S =0.8V		22						ns
		2.3-2.7	V _S =1.5V		18	30		40			
		3.0-3.3			16	30		40			
		3.6-4.3			15	30		40			
t _D	Break Before Make Time Delay	1.65-1.95	C _L =35pF R _L = 50Ω V _S =1.5V	10	80						ns
		2.3-2.7		10	60						
		3.0-3.3		10	55						
		3.6-4.3		10	50						
Q	Charge injection	1.65-1.95	C _L = 100pF		50						pC
		2.3-2.7	R _L = 1MΩ		40						
		3.0-3.3	V _{GEN} = 0V		35						
		3.6-4.3	R _{GEN} = 0Ω		35						

Table 8: Analog Switch Characteristics ($C_L = 5\text{pF}$, $R_L = 50\Omega$, $T_A = 25^\circ\text{C}$)

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
OIRR	Off Isolation (1)	1.65-4.3	V _S = 1V _{RMS} f= 100KHz		-64						dB
Xtalk	Crosstalk	1.65-4.3	V _S = 1V _{RMS} f= 100KHz		-54						dB
THD	Total Harmonic Distortion	2.3-4.3	R _L = 600Ω V _{IN} = 2V _{PP} f= 20Hz to 20kHz		0.03						%
BW	-3dB Bandwidth	1.65-4.3	R _L = 50Ω		50						MHz
C _{IN}	Control Pin Input Capacitance				5						pF
C _{Sn}	Sn Port Capacitance	3.3	f= 1MHz		30						
C _D	D Port Capacitance when Switch is Enabled	3.3	f= 1MHz		84						

Note 1: Off Isolation = $20\text{Log}_{10}(V_D/V_S)$, V_D = output. V_S = input to off switch

Figure 3: ON Resistance

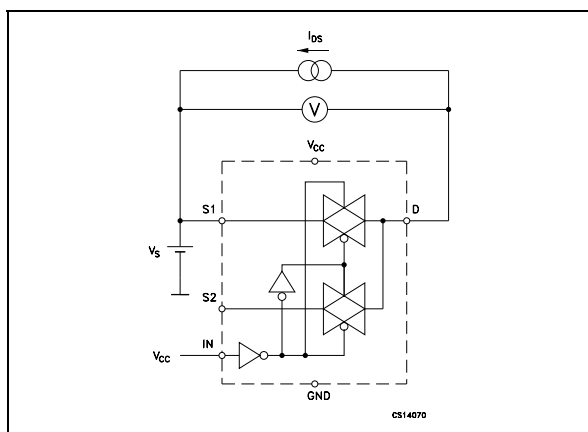


Figure 6: Bandwidth

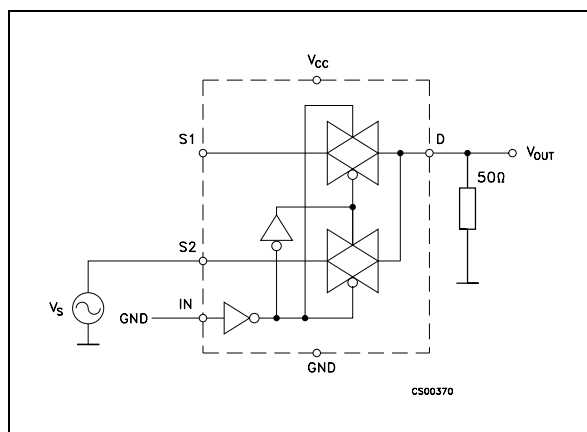


Figure 4: Off Leakage

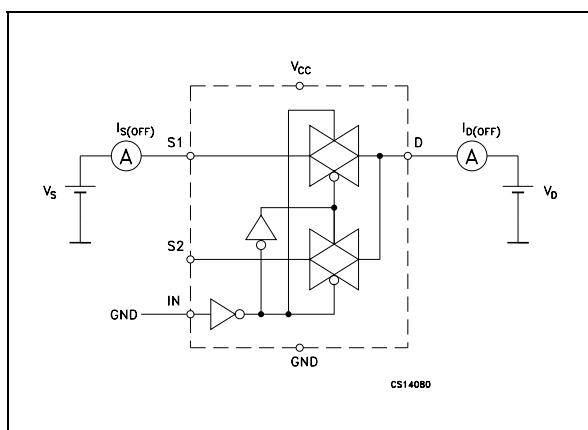


Figure 7: Channel To Channel Crosstalk

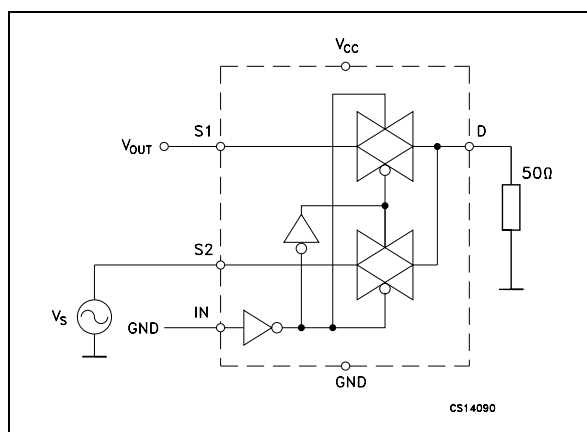


Figure 5: Off Isolation

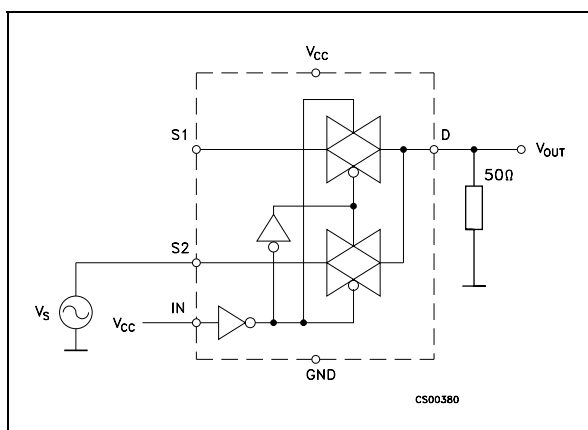
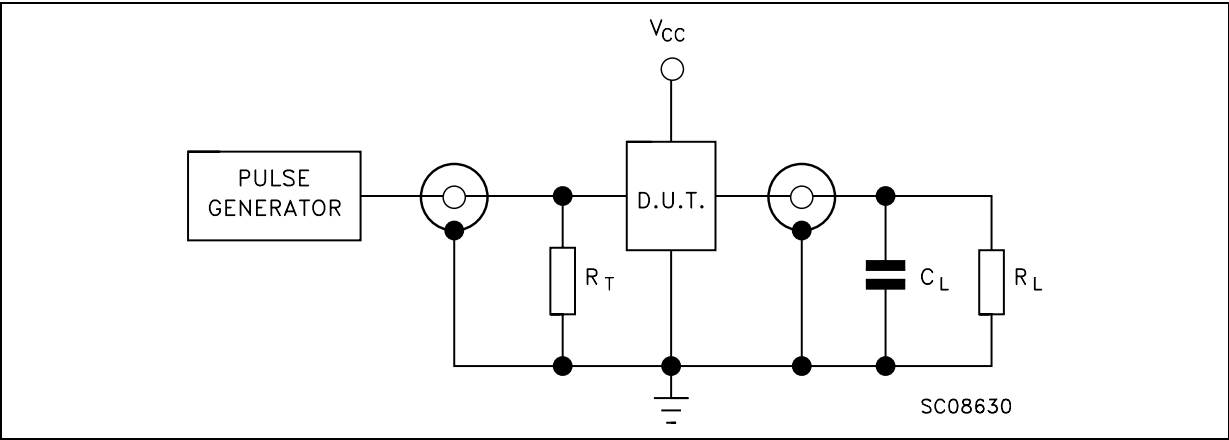


Figure 8: Test Circuit



$C_L = 5/35\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_L = 50\Omega$ or equivalent
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 9: Break-before-make Time Delay

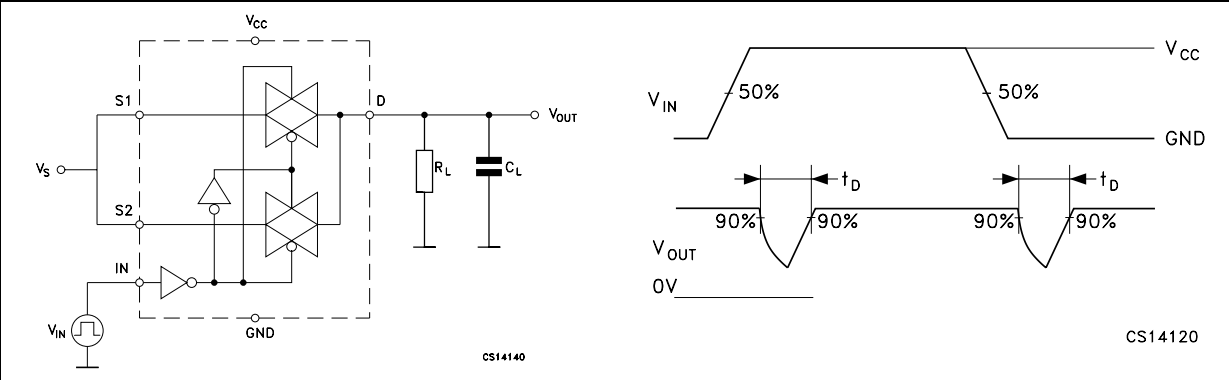


Figure 10: Switching Time and Charge Injection ($V_{GEN}=0\text{V}$, $R_{GEN}=0\Omega$, $R_L=1\text{M}\Omega$, $C_L=100\text{pF}$)

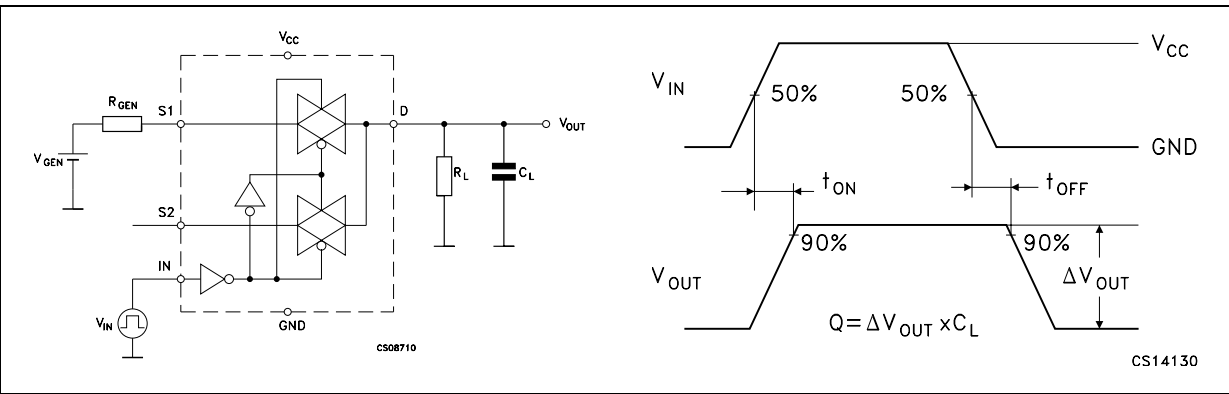
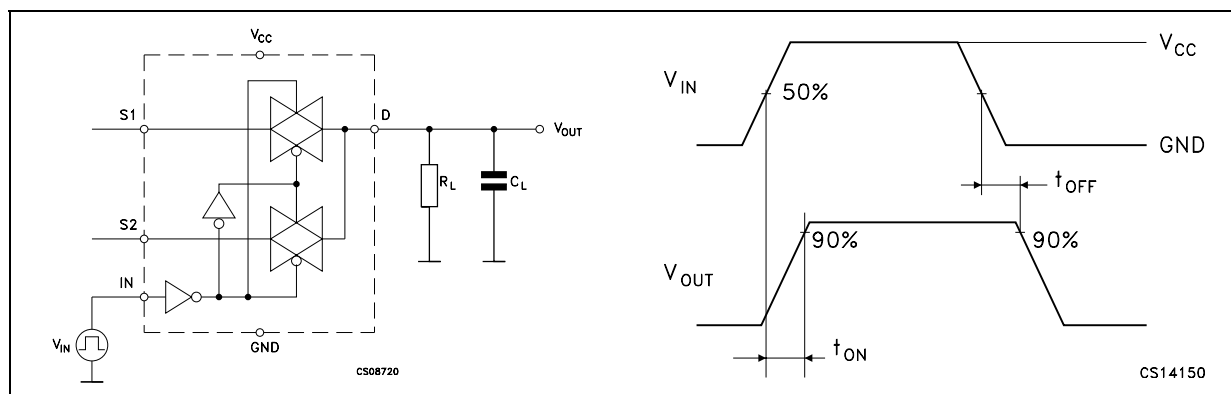


Table 9: Turn On, Turn Off Delay Time

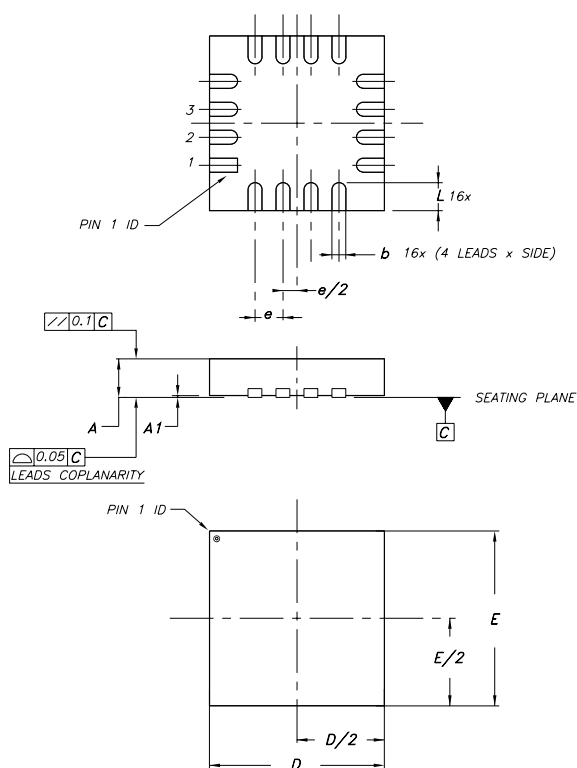


Package Mechanical Data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

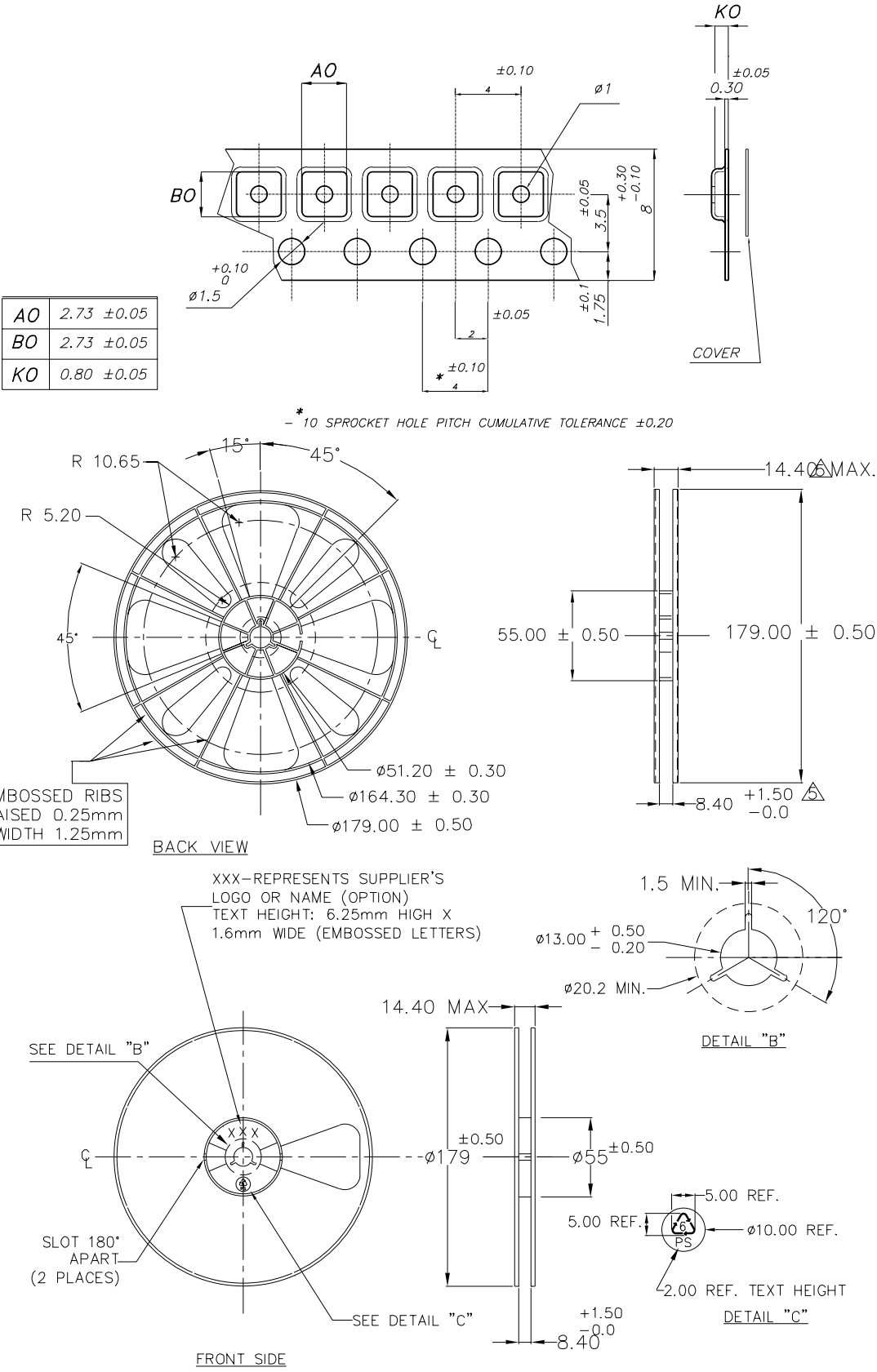
QFN16 (2.5x2.5) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1		0.02	0.05		0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
D	2.40	2.50	2.60	0.094	0.098	0.102
E	2.40	2.50	2.60	0.094	0.098	0.102
e		0.40			0.016	
L	0.35	0.40	0.45	0.014	0.016	0.018



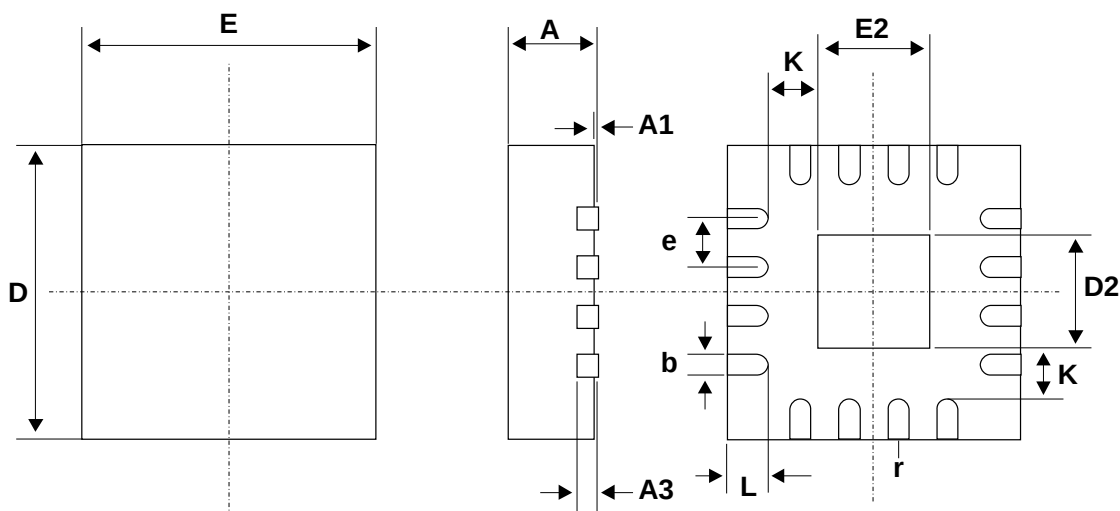
7815712A

QFN16 (2.5 x 2.5) Tape and Reel



QFN16 (3x3) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.80	0.90	1.00	0.032	0.035	0.039
A1		0.02	0.05		0.001	0.002
A3		0.20			0.008	
b	0.18	0.25	0.30	0.007	0.010	0.012
D		3.00			0.118	
D2	1.55	1.70	1.80	0.061	0.067	0.071
E		3.00			0.118	
E2	1.55	1.70	1.80	0.061	0.067	0.071
e		0.50			0.020	
K		0.20			0.008	
L	0.30	0.40	0.50	0.012	0.016	0.020
r	0.09			0.006		



Tape & Reel QFNxx/DFNxx (3x3) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			18.4			0.724
Ao		3.3			0.130	
Bo		3.3			0.130	
Ko		1.1			0.043	
Po		4			0.157	
P		8			0.315	

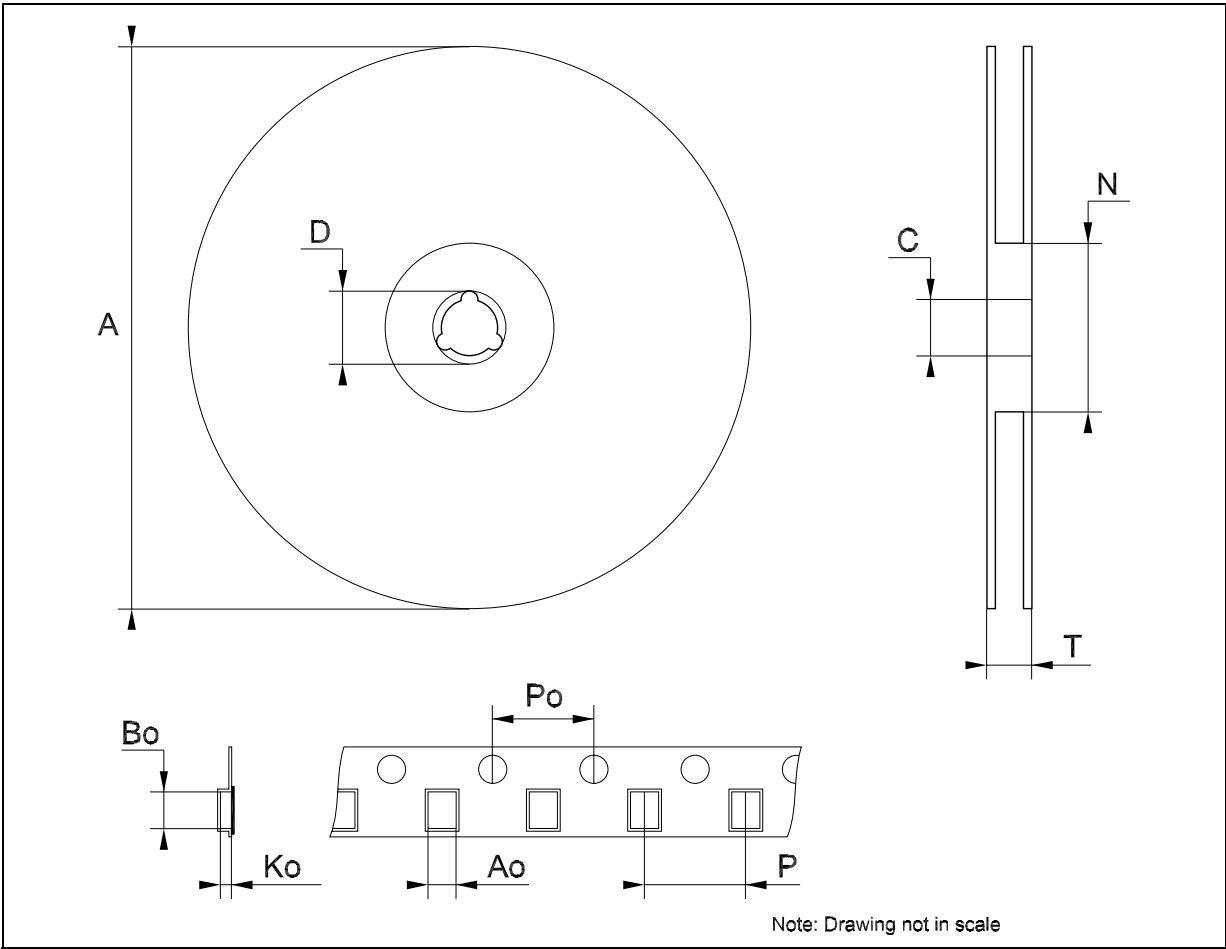


Table 10: Revision History

Date	Revision	Description of Changes
24-Nov-2004	1	First Release.
13-Jan-2005	2	I_{CCLV} is changed on Table 6
23-Mar-2005	3	Table 3 has been updated and V_{CC} is changed on Table 4
31-May-2005	4	Add New Package QFN16 (2.5x2.5).
04-Jul-2005	5	The Q Values on Table 7 has been updated.
19-Jul-2005	6	Add New Package QFN16 (2.6x1.8).
03-Aug-2005	7	The V_{CC} and V_{IC} values on Table 4 has been updated.
10-Oct-2005	8	Removed all the information about the QFN16L 2.6X1.8 package
21-Nov-2005	9	Modified the label in Table 1
21-Dec-2005	10	Few Updates, added tape and reel QFN16 (2.5 x 2.5)

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