

FUNCTIONAL DIAGRAM

Octal D-Type Flip-Flop, 3-State Positive-Edge-Triggered

CD54/74AC/ACT564 - Inverting

CD54/74AC/ACT574 - Non-Inverting

Type Features:

- Buffered inputs
- Typical propagation delay:
6.5 ns @ $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$

The RCA-CD54/74AC564 and CD54/74AC574 and the CD54/74ACT564 and CD54/74ACT574 octal D-type, 3-state, positive-edge-triggered flip-flops use the RCA ADVANCED CMOS technology. The eight flip-flops enter data into their registers on the LOW-to-HIGH transition of the clock (CP). The Output Enable ($\overline{OE}$) controls the 3-state outputs and is independent of the register operation. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high-impedance state. The CD54/74AC/ACT564 and CD54/74AC/ACT574 share the same pin configurations; the CD54/74AC/ACT564, however, has inverted outputs and the CD54/74AC/ACT574 has non-inverted outputs.

The CD74AC/ACT564 and CD74AC/ACT574 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to $+85^\circ\text{C}$); and Extended Industrial/Military (-55 to $+125^\circ\text{C}$).

The CD54AC/ACT564 and CD54AC/ACT574, available in chip form (H suffix), are operable over the -55 to $+125^\circ\text{C}$ temperature range.

Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$ output drive current
 - Fanout to 15 FAST* ICs
 - Drives 50-ohm transmission lines

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

INPUTS			OUTPUTS	
			564 $\overline{Q_n}$	574 Q_n
$\overline{OE}$	CP	D_n		
L		H	L	H
L		L	H	L
L	L	X	$\overline{QO}$	QO
H	X	X	Z	Z

H = High level (steady state)

L = Low level (steady state)

X = Don't care

= Transition from low to high level

QO = The level of Q before the indicated steady-state input conditions were established

$\overline{QO}$ = The level of $\overline{Q}$ before the indicated steady-state input conditions were established.

Z = High impedance

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CD54/74AC564, CD54/74AC574 CD54/74ACT564, CD54/74ACT574

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE (V_{CC})	-0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	± 50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	± 50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND})	± 100 mA*
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -55$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	-55 to $+125^\circ\text{C}$
STORAGE TEMPERATURE (T_{stg})	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. (1.59 mm) with solder contacting lead tips only	$+300^\circ\text{C}$

*For up to 4 outputs per device; add ± 25 mA for each additional output.

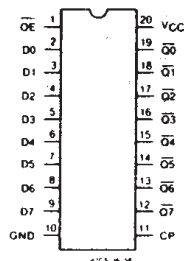
RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

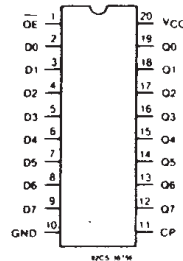
CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC} *: (For T_A = Full Package-Temperature Range) AC Types ACT Types	1.5 4.5	5.5 5.5	V V
DC Input or Output Voltage, V_I , V_O	0	V_{CC}	V
Operating Temperature, T_A :	-55	+125	$^\circ\text{C}$
Input Rise and Fall Slew Rate, dt/dv at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	0 0 0	50 20 10	ns/V ns/V ns/V

*Unless otherwise specified, all voltages are referenced to ground.

TERMINAL ASSIGNMENT DIAGRAMS



CD54/74AC/ACT564



CD54/74AC/ACT574

Technical Data

CD54/74AC564, CD54/74AC574 CD54/74ACT564, CD54/74ACT574

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V _I (V)	I _O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V _{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V _{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V _{OH}	V _{IH} or V _{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, * {	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V _{OL}	V _{IH} or V _{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, * {	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I _I	V _{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I _{OZ}	V _{IH} or V _{IL} V _O = V _{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I _{CC}	V _{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C. 75 ohms at +125°C.

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CD54/74AC564, CD54/74AC574 **CD54/74ACT564, CD54/74ACT574**

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS		TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
					+25		-40 to +85		-55 to +125		
		V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	V_{OH}	V_{IH} or V_{IL} #, *	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V_{OL}	V_{IH} or V_{IL} #, *	0.05	4.5	—	±0.1	—	±1	—	±1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I_i	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current	I_{OZ}	V_{IH} or V_{IL} $V_O = V_{CC}$ or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI_{CC}	$V_{CC}-2.1$		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*
D, OE	0.7
CP	1.17

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

CD54/74AC564, CD54/74AC574

CD54/74ACT564, CD54/74ACT574

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Clock Pulse Width	t _w	1.5 3.3* 5†	44 4.9 3.5	— — —	50 5.6 4	— — —	ns
Setup Time Data to Clock	t _{su}	1.5 3.3 5	2 2 2	— — —	2 2 2	— — —	ns
Hold Time Data to Clock	t _h	1.5 3.3 5	2 2 2	— — —	2 2 2	— — —	ns
Maximum Clock Frequency	f _{max}	1.5 3.3 5	11 101 143	— — —	10 89 125	— — —	MHz

*3.3 V: min. is @ 3 V

†5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A) -°C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Clock to Q AC574	t _{PLH} t _{PHL}	1.5 3.3* 5†	— 4 2.9	123 13.7 9.8	— 3.8 2.7	135 15.1 10.8	ns
Clock to $\bar{Q}$ AC564	t _{PLH} t _{PHL}	1.5 3.3 5	— 4.1 2.9	128 14.4 10.3	— 4 2.8	141 15.8 11.3	ns
Output Enable to Q, $\bar{Q}$	t _{PZL} t _{PZH}	1.5 3.3 5	— 5.6 3.7	165 19.2 13.2	— 5.5 3.6	181 21.8 14.5	ns
Output Disable to Q, $\bar{Q}$	t _{PLZ} t _{PHZ}	1.5 3.3 5	— 4.7 3.7	165 16.5 13.2	— 4.5 3.6	181 18.1 14.5	ns
Power Dissipation Capacitance	C _{PD} §	—	67 Typ.		67 Typ.		pF
Min. (Valley) V _{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V _{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V _{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V _{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C _I	—	—	10	—	10	pF
3-State Output Capacitance	C _O	—	—	15	—	15	pF

*3.3 V: min. is @ 3.6 V

max. is @ 3 V

†5 V: min. is @ 5.5 V

max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per flip flop.

$P_D = C_{PD} V_{CC}^2 f_i + \sum V_{CC}^2 f_o C_L$ where f_i = input frequency
 f_o = output frequency
 C_L = output load capacitance
 V_{CC} = supply voltage.

CD54/74AC564, CD54/74AC574 **CD54/74ACT564, CD54/74ACT574**

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A) -°C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Clock Pulse Width	t _w	5†	3.9	—	4.5	—	ns
Setup Time Data to Clock	t _{su}	5	2	—	2	—	ns
Hold Time Data to Clock	t _h	5	2.6	—	3	—	ns
Maximum Clock Frequency	f _{max}	5	125	—	110	—	MHz

†5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A) -°C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Clock to Q ACT574	t _{PLH} t _{PHL}	5†	2.9	10.2	2.8	11.2	ns
Clock to $\bar{Q}$ ACT564	t _{PLH} t _{PHL}	5	3	10.6	2.9	11.7	ns
Output Enable and Disable to Q ACT574	t _{PLZ} t _{PHZ} t _{PZL} t _{PZH}	5	3.7	13.2	3.6	14.5	ns
Output Enable and Disable to $\bar{Q}$ ACT564	t _{PLZ} t _{PHZ} t _{PZL} t _{PZH}	5	3.7	13.2	3.6	14.5	ns
Power Dissipation Capacitance	C _{PD} §	—	67 Typ.		67 Typ.		pF
Min. (Valley) V _{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V _{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V _{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V _{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C _I	—	—	10	—	10	pF
3-State Output Capacitance	C _O	—	—	15	—	15	pF

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per flip flop.

$$P_D = C_{PD} V_{CC}^2 f_i + \sum V_{CC}^2 f_o C_L + V_{CC} \Delta I_{CC} \text{ where } f_i = \text{input frequency}$$

$$f_o = \text{output frequency}$$

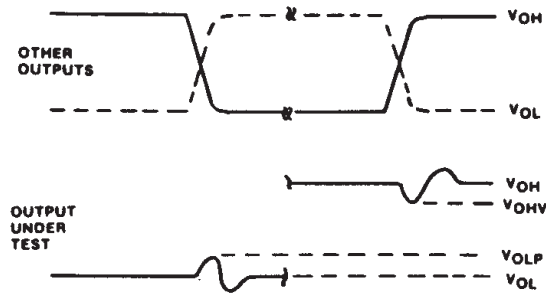
$$C_L = \text{output load capacitance}$$

$$V_{CC} = \text{supply voltage.}$$

Technical Data

CD54/74AC564, CD54/74AC574 CD54/74ACT564, CD54/74ACT574

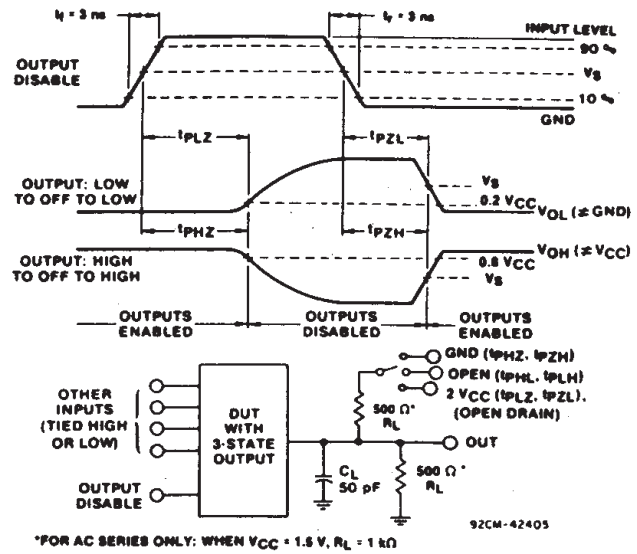
PARAMETER MEASUREMENT INFORMATION



NOTES:

1. V_{OHV} AND V_{OLP} ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS:
 $PRR \leq 1 \text{ MHz}$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$, SKEW 1 ns .
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED.
 IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH $0.1 \mu\text{F}$ CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

92CS-42406

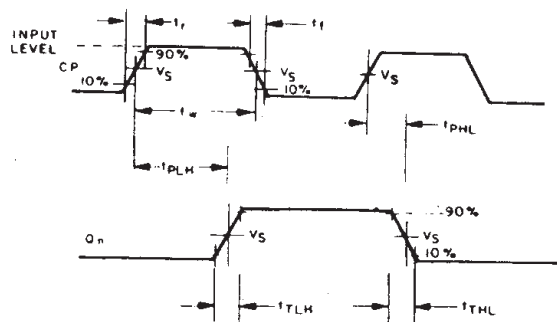


*FOR AC SERIES ONLY: WHEN $V_{CC} = 1.5 \text{ V}$, $R_L = 1 \text{ k}\Omega$

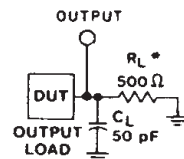
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Fig. 1 - Simultaneous switching transient waveforms.

Fig. 2 - Three-state propagation delay waveforms and test circuit.



92CS-38404 R1



*FOR AC SERIES ONLY: WHEN
 $V_{CC} = 1.5 \text{ V}$, $R_L = 1 \text{ k}\Omega$

92LS-42189

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	$0.5 V_{CC}$	1.5 V
Output Switching Voltage, V_S	$0.5 V_{CC}$	$0.5 V_{CC}$

Fig. 3 - Propagation delays times and test circuit.

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