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LM114 & LM115 Transistor Pairs

GENERAL DESCRIPTION

These devices contain a pair of junction-isolated NPN transistors fabricated on a single silicon substrate. This monolithic structure makes possible extremely-tight parameter matching at low cost. Further, advanced processing techniques yield exceptionally high current gains at low collector currents, virtual elimination of 'popcorn noise', low leakages and improved long-term stability.

FEATURES

Low offset voltage—0.5mV maximum

Low drift— $2\mu\text{V}/^\circ\text{C}$ maximum from -55°C to 125°C

High current gain—500 minimum at $10\mu\text{A}$

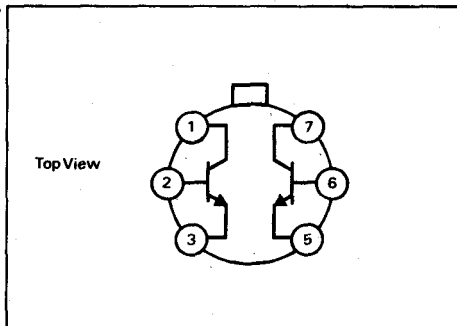
Tight beta match—10% maximum

High breakdown voltage—to 60V

Matching guaranteed over a 0V to 45V collector-base voltage range.

Although designed primarily for high breakdown voltage and exceptional DC characteristics, these transistors have surprisingly good high-frequency performance. The gain-bandwidth product is 450 MHz with 1mA collector current and 5V collector-base voltage and 22 MHz with $10\mu\text{A}$ collector current. Collector base-capacitance is only 1.3pF at 5V.

CONNECTION DIAGRAM



See outline drawing No. 96 for dimensions.

REFERENCE TABLE

Code	Stock No.
LM114H	31123R
LM114AH	31124G
LM115H	31125E
LM115AH	31126C

ABSOLUTE MAXIMUM RATINGS

	LM114 LM114A	LM115 LM115A
Collector-base voltage (BV _{CBO})	45V	60V
Collector-Emitter voltage (BV _{CER})	45V	60V
Collector-collector voltage	45V	60V
Emitter-emitter voltage	45V	60V
Emitter-base voltage (BV _{EBO})	60V	
Collector current	20mA	

Total power dissipation (Note 1)	1.8W
Operating junction Temperature	-55°C to 150°C
Storage temperature	-65°C to 150°C
Lead temperature (soldering, 10 sec)	300°C

Note 1: The maximum dissipation given is for a 25°C case temperature. For operation under other conditions, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of $70^\circ\text{C}/\text{W}$ junction to case or $230^\circ\text{C}/\text{W}$ junction to ambient.