



High-Performance, Fully-Differential AUDIO OPERATIONAL AMPLIFIER

Check for Samples: [OPA1632](#)

FEATURES

- **SUPERIOR SOUND QUALITY**
- **ULTRA LOW DISTORTION: 0.000022%**
- **LOW NOISE: $1.3\text{nV}/\sqrt{\text{Hz}}$**
- **HIGH SPEED:**
 - Slew Rate: $50\text{V}/\mu\text{s}$
 - Gain Bandwidth: 180MHz
- **FULLY DIFFERENTIAL ARCHITECTURE:**
 - Balanced Input and Output Converts Single-Ended Input to Balanced Differential Output
- **WIDE SUPPLY RANGE: $\pm 2.5\text{V}$ to $\pm 16\text{V}$**
- **SHUTDOWN TO CONSERVE POWER**

APPLICATIONS

- **AUDIO ADC DRIVER**
- **BALANCED LINE DRIVER**
- **BALANCED RECEIVER**
- **ACTIVE FILTER**
- **PREAMPLIFIER**

DESCRIPTION

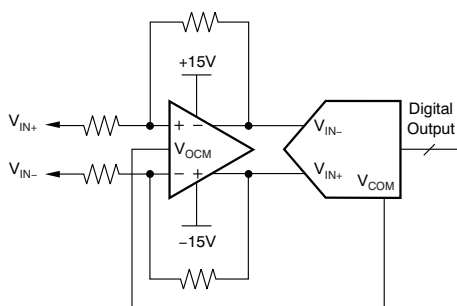
The OPA1632 is a fully-differential amplifier designed for driving high-performance audio analog-to-digital converters (ADCs). It provides the highest audio quality, with very low noise and output drive characteristics optimized for this application. The OPA1632's excellent gain bandwidth of 180MHz and very fast slew rate of $50\text{V}/\mu\text{s}$ produce exceptionally low distortion. Very low input noise of $1.3\text{nV}/\sqrt{\text{Hz}}$ further ensures maximum signal-to-noise ratio and dynamic range.

The flexibility of the fully differential architecture allows for easy implementation of a single-ended to fully-differential output conversion. Differential output reduces even-order harmonics and minimizes common-mode noise interference. The OPA1632 provides excellent performance when used to drive high-performance audio ADCs such as the [PCM1804](#). A shutdown feature also enhances the flexibility of this amplifier.

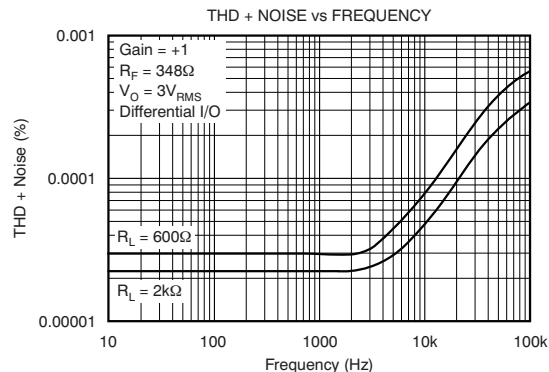
The OPA1632 is available in an SO-8 package and a thermally-enhanced MSOP-8 PowerPAD™ package.

RELATED PRODUCTS

PRODUCT	DESCRIPTION
OPAx134	High-Performance Audio Amplifiers
OPA627/OPA637	Precision High-Speed DiFET Amplifiers
OPAx227/OPAx228	Low-Noise Bipolar Amplifiers



Typical ADC Circuit



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All other trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION⁽¹⁾

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA1632	SO-8	D	–40°C to +85°C	OPA1632	OPA1632D	Rails, 100
					OPA1632DR	Tape and Reel, 2500
	MSOP-8 PowerPAD	DGK	–40°C to +85°C	1632	OPA1632DGN	Rails, 100
					OPA1632DGNR	Tape and Reel, 2500

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

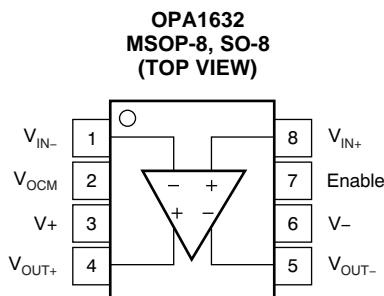
ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾

Over operating free-air temperature range (unless otherwise noted).

		OPA1632	UNIT
Supply Voltage, $\pm V_S$		± 16.5	V
Input Voltage, V_I		$\pm V_S$	V
Output Current, I_O		150	mA
Differential Input Voltage, V_{ID}		± 3	V
Maximum Junction Temperature, T_J		+150	°C
Operating Free-Air Temperature Range		–40 to +85	°C
Storage Temperature Range, T_{STG}		–65 to +150	°C
ESD Ratings	Human Body Model (HBM)	1	kV
	Charged Device Model (CDM)	500	V
	Machine Model (MM)	200	V

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
- (2) The OPA1632 MSOP-8 package version incorporates a PowerPAD on the underside of the chip. This acts as a heatsink and must be connected to a thermally-dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature, which can permanently damage the device. See TI technical brief [SLMA002](#) for more information about using the PowerPAD thermally-enhanced package.

PIN CONFIGURATION



ELECTRICAL CHARACTERISTICS: $V_S = \pm 15V$

At $V_S = \pm 15V$; $R_F = 390\Omega$, $R_L = 800\Omega$, and $G = +1$, unless otherwise noted.

PARAMETER	CONDITIONS	OPA1632			UNIT
		MIN	TYP	MAX	
OFFSET VOLTAGE					
Input Offset Voltage			± 0.5	± 3	mV
vs Temperature	dV_{OS}/dT		± 5		$\mu V/^{\circ}C$
vs Power Supply, dc	PSRR	316	13		$\mu V/V$
INPUT BIAS CURRENT					
Input Bias Current	I_B		2	6	μA
Input Offset Current	I_{OS}		± 100	± 500	nA
NOISE					
Input Voltage Noise	$f = 10\text{ kHz}$		1.3		nV/\sqrt{Hz}
Input Current Noise	$f = 10\text{ kHz}$		0.4		pA/\sqrt{Hz}
INPUT VOLTAGE					
Common-Mode Input Range		$(V-) + 1.5$		$(V+) - 1$	V
Common-Mode Rejection Ratio, dc		74	90		dB
INPUT IMPEDANCE					
Input Impedance (each input pin)			$34 \parallel 4$		$M\Omega \parallel pF$
OPEN-LOOP GAIN					
Open-Loop Gain, dc		66	78		dB
FREQUENCY RESPONSE					
Small-Signal Bandwidth	$G = +1$, $R_F = 348\Omega$		180		MHz
$(V_O = 100mV_{PP}$, Peaking < 0.5 dB)	$G = +2$, $R_F = 602\Omega$		90		MHz
	$G = +5$, $R_F = 1.5k\Omega$		36		MHz
	$G = +10$, $R_F = 3.01k\Omega$		18		MHz
Bandwidth for 0.1dB Flatness	$G = +1$, $V_O = 100mV_{PP}$		40		MHz
Peaking at a Gain of 1	$V_O = 100mV_{PP}$		0.5		dB
Large-Signal Bandwidth	$G = +2$, $V_O = 20V_{PP}$		800		kHz
Slew Rate (25% to 75%)	$G = +1$		50		V/ μs
Rise and Fall Time	$G = +1$, $V_O = 5V$ Step		100		ns
Settling Time to 0.1%	$G = +1$, $V_O = 2V$ Step		75		ns
0.01%	$G = +1$, $V_O = 2V$ Step		200		ns
Total Harmonic Distortion + Noise	$G = +1$, $f = 1kHz$, $V_O = 3V_{RMS}$				
Differential Input/Output	$R_L = 600\Omega$		0.0003		%
Differential Input/Output	$R_L = 2k\Omega$		0.000022		%
Single-Ended In/Differential Out	$R_L = 600\Omega$		0.000059		%
Single-Ended In/Differential Out	$R_L = 2k\Omega$		0.000043		%
Intermodulation Distortion	$G = +1$, SMPTE/DIN, $V_O = 2V_{PP}$				
Differential Input/Output	$R_L = 600\Omega$		0.00008		%
Differential Input/Output	$R_L = 2k\Omega$		0.00005		%
Single-Ended In/Differential Out	$R_L = 600\Omega$		0.0001		%
Single-Ended In/Differential Out	$R_L = 2k\Omega$		0.0007		%
Headroom	THD < 0.01%, $R_L = 2k\Omega$		20.0		V_{PP}
OUTPUT					
Voltage Output Swing	$R_L = 2k\Omega$	$(V+) - 1.9$		$(V-) + 1.9$	V
	$R_L = 800\Omega$	$(V+) - 4.5$		$(V-) + 4.5$	V
Short-Circuit Current	Sourcing/Sinking	+50/-60	85		mA
Closed-Loop Output Impedance	$G = +1$, $f = 100kHz$		0.3		Ω

ELECTRICAL CHARACTERISTICS: $V_S = \pm 15V$ (continued)At $V_S = \pm 15V$; $R_F = 390\Omega$, $R_L = 800\Omega$, and $G = +1$, unless otherwise noted.

PARAMETER	CONDITIONS	OPA1632			UNIT
		MIN	TYP	MAX	
POWER-DOWN ⁽¹⁾					
Enable Voltage Threshold	$V_{ENABLE} = -15V$ Time for I_Q to Reach 50% Time for I_Q to Reach 50%		(V-) + 2		V
Disable Voltage Threshold			(V-) + 0.8		V
Shutdown Current			0.85		mA
Turn-On Delay			2		μs
Turn-Off Delay			2		μs
POWER SUPPLY					
Specified Operating Voltage	I_Q Per Channel	±2.5	±15	±16	V
Operating Voltage					V
Quiescent Current			14	17.1	mA
TEMPERATURE RANGE					
Specified Range	θ_{JA}	−40		+85	°C
Operating Range		−40		+125	°C
Storage Range		−65		+150	°C
Thermal Resistance					
SO-8, MSOP-8				200	°C/W

(1) Amplifier has internal 50k Ω pull-up resistor to V_{CC+} pin. This enables the amplifier with no connection to shutdown pin.

TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, and $R_L = 2\text{k}\Omega$, unless otherwise noted.

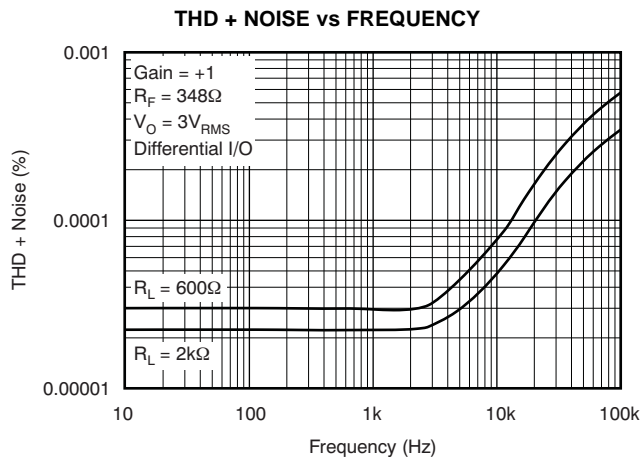


Figure 1.

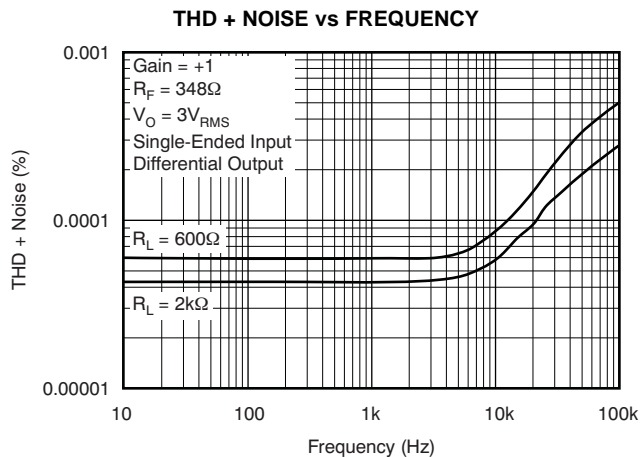


Figure 2.

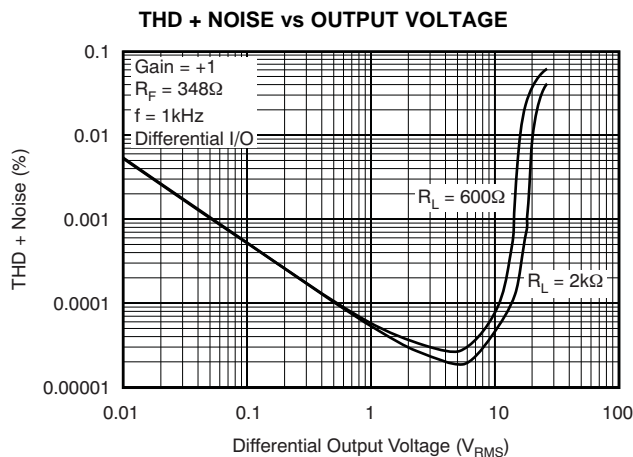


Figure 3.

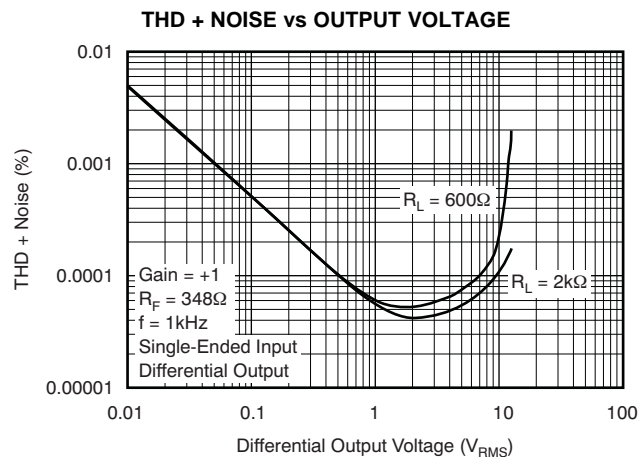


Figure 4.

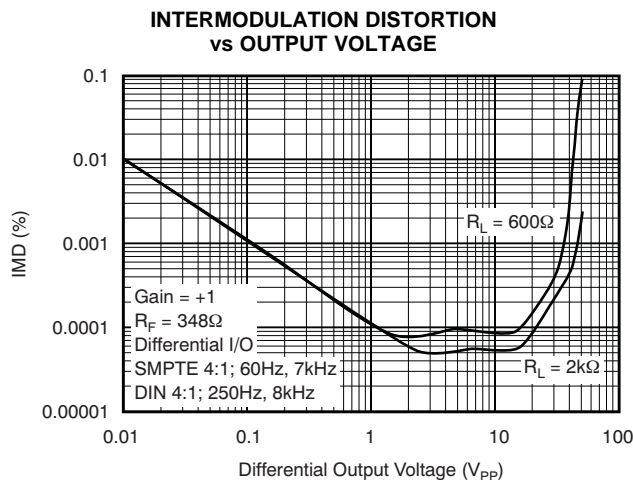


Figure 5.

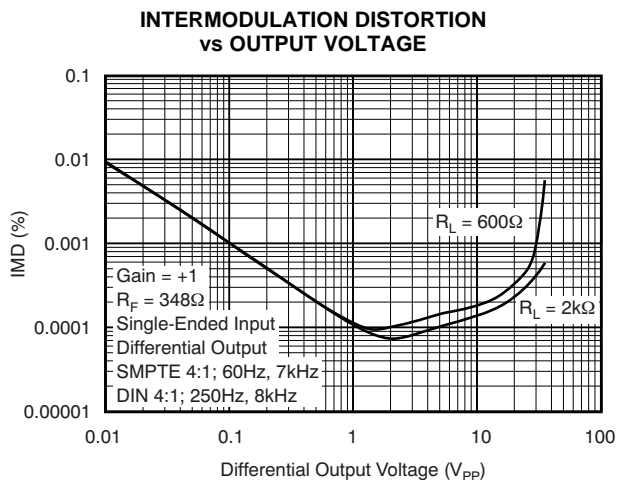


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, and $R_L = 2\text{k}\Omega$, unless otherwise noted.

VOLTAGE NOISE vs FREQUENCY

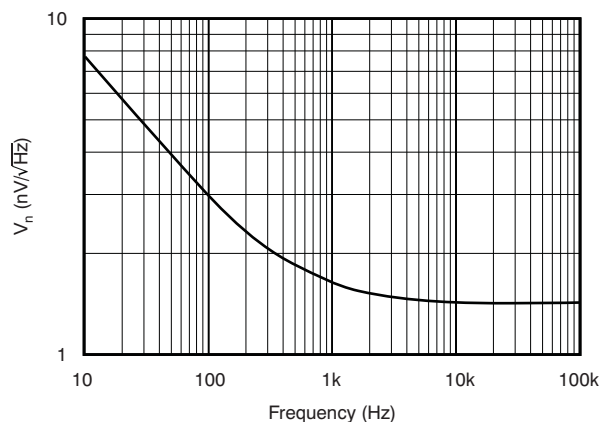


Figure 7.

CURRENT NOISE vs FREQUENCY

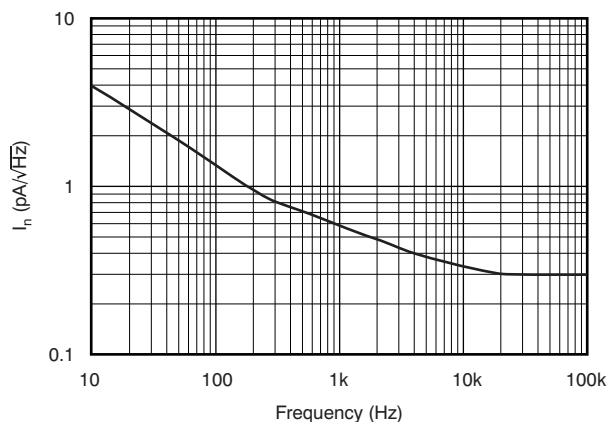


Figure 8.

**OUTPUT VOLTAGE
vs DIFFERENTIAL LOAD RESISTANCE**

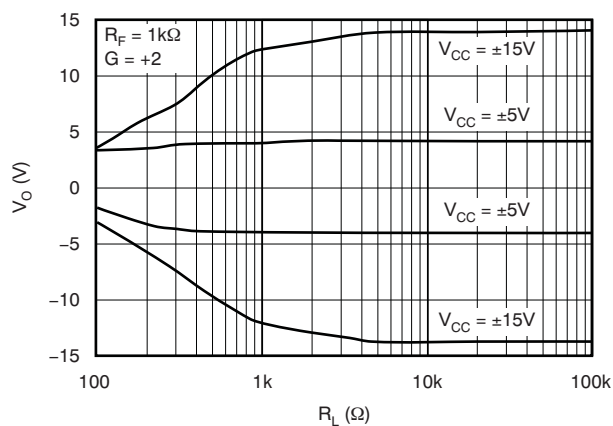


Figure 9.

**OUTPUT IMPEDANCE
vs FREQUENCY**

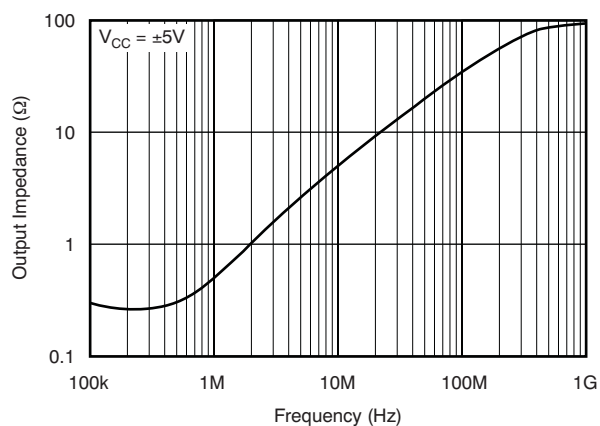


Figure 10.

APPLICATION INFORMATION

Figure 11 shows the OPA1632 used as a differential-output driver for the PCM1804 high-performance audio ADC.

Supply voltages of $\pm 15\text{V}$ are commonly used for the OPA1632. The relatively low input voltage swing required by the ADC allows use of lower power-supply voltage, if desired. Power supplies as low as $\pm 8\text{V}$ can be used in this application with excellent performance. This reduces power dissipation and heat rise. Power supplies should be bypassed with $10\mu\text{F}$ tantalum capacitors in parallel with $0.1\mu\text{F}$ ceramic capacitors to avoid possible oscillations and instability.

The V_{COM} reference voltage output on the PCM1804 ADC provides the proper input common-mode reference voltage (2.5V). This V_{COM} voltage is buffered with op amp A_2 and drives the output common-mode voltage pin of the OPA1632. This biases the average output voltage of the OPA1632 to 2.5V .

The signal gain of the circuit is generally set to approximately 0.25 to be compatible with commonly-used audio line levels. Gain can be adjusted, if necessary, by changing the values of R_1 and R_2 . The feedback resistor values (R_3 and R_4) should be kept relatively low, as indicated, for best noise performance.

R_5 , R_6 , and C_3 provide an input filter and charge glitch reservoir for the ADC. The values shown are generally satisfactory. Some adjustment of the values may help optimize performance with different ADCs.

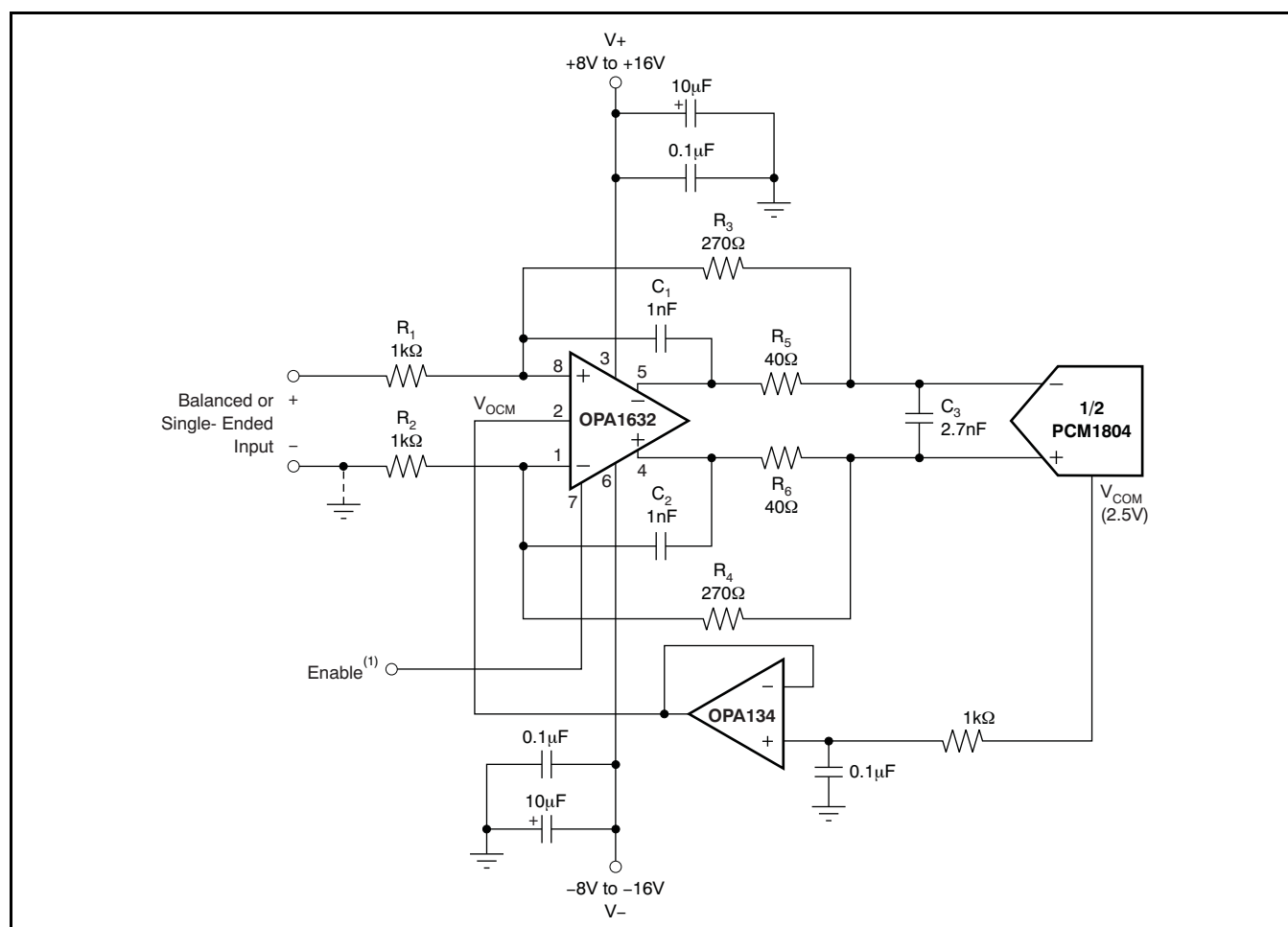


Figure 11. ADC Driver for Professional Audio

It is important to maintain accurate resistor matching on R_1/R_2 and R_3/R_4 to achieve good differential signal balance. Use 1% resistors for highest performance. When connected for single-ended inputs (inverting input grounded, as shown in Figure 11), the source impedance must be low. Differential input sources must have well-balanced or low source impedance.

Capacitors C_1 , C_2 , and C_3 should be chosen carefully for good distortion performance. Polystyrene, polypropylene, NPO ceramic, and mica types are generally excellent. Polyester and high-K ceramic types such as Z5U can create distortion.

FULLY-DIFFERENTIAL AMPLIFIERS

Differential signal processing offers a number of performance advantages in high-speed analog signal processing systems, including immunity to external common-mode noise, suppression of even-order nonlinearities, and increased dynamic range. Fully-differential amplifiers not only serve as the primary means of providing gain to a differential signal chain, but also provide a monolithic solution for converting single-ended signals into differential signals allowing for easy, high-performance processing.

A standard configuration for the device is shown in Figure 12. The functionality of a fully differential amplifier can be imagined as two inverting amplifiers that share a common noninverting terminal (though the voltage is not necessarily fixed). For more information on the basic theory of operation for fully differential amplifiers, refer to the Texas Instruments application note [SLOA054](#), *Fully Differential Amplifiers*, available for download from the TI web site (www.ti.com).

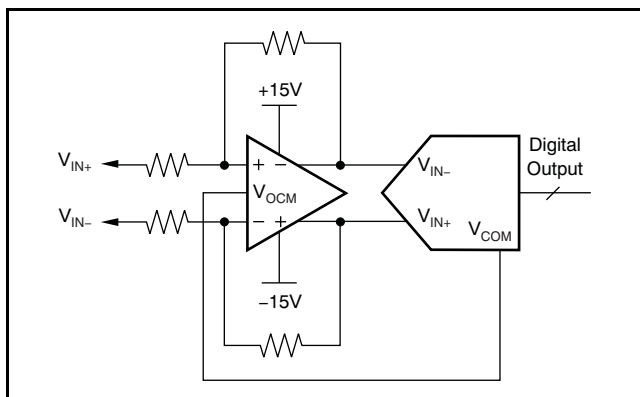


Figure 12. Typical ADC Circuit

SHUTDOWN FUNCTION

The shutdown (enable) function of the OPA1632 is referenced to the negative supply of the operational amplifier. A valid logic low ($< 0.8V$ above negative supply) applied to the enable pin (pin 7) disables the amplifier output. Voltages applied to pin 7 that are greater than $2V$ above the negative supply place the amplifier output in an active state, and the device is enabled. If pin 7 is left disconnected, an internal pull-up resistor enables the device. Turn-on and turn-off times are approximately $2\mu s$ each.

Quiescent current is reduced to approximately $0.85mA$ when the amplifier is disabled. When disabled, the output stage is *not* in a high-impedance state. Thus, the shutdown function cannot be used to create a multiplexed switching function in series with multiple amplifiers.

OUTPUT COMMON-MODE VOLTAGE

The output common-mode voltage pin sets the dc output voltage of the OPA1632. A voltage applied to the V_{OCM} pin from a low-impedance source can be used to directly set the output common-mode voltage. For a V_{OCM} voltage at mid-supply, make no connection to the V_{OCM} pin.

Depending on the intended application, a decoupling capacitor is recommended on the V_{OCM} node to filter any high-frequency noise that could couple into the signal path through the V_{OCM} circuitry. A $0.1\mu F$ or $1\mu F$ capacitor is generally adequate.

Output common-mode voltage causes additional current to flow in the feedback resistor network. Since this current is supplied by the output stage of the amplifier, this creates additional power dissipation. For commonly-used feedback resistance values, this current is easily supplied by the amplifier. The additional internal power dissipation created by this current may be significant in some applications and may dictate use of the MSOP PowerPAD package to effectively control self-heating.

PowerPAD DESIGN CONSIDERATIONS

The OPA1632 is available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted (see [Figure 13\[a\]](#) and [Figure 13\[b\]](#)). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package (see [Figure 13\[c\]](#)). Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

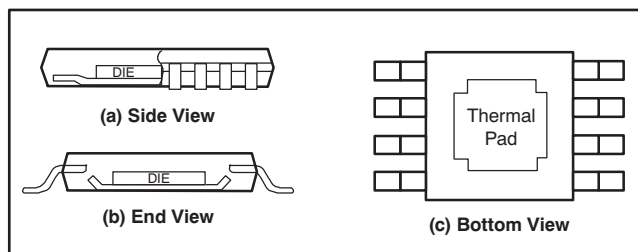


Figure 13. Views of the Thermally-Enhanced Package

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device. Soldering the PowerPAD to the printed circuit board (PCB) is always required, even with applications that have low power dissipation. It provides the necessary thermal and mechanical connection between the lead frame die pad and the PCB.

PowerPAD PCB LAYOUT CONSIDERATIONS

1. The PowerPAD is electrically isolated from the silicon and all leads. Connecting the PowerPAD to any potential voltage between the power-supply voltages is acceptable, but it is recommended to tie to ground because it is generally the largest conductive plane.
2. Prepare the PCB with a top-side etch pattern, as shown in [Figure 14](#). There should be etch for the leads as well as etch for the thermal pad.

3. Place five holes in the area of the thermal pad. These holes should be 13mils (0,03302cm) in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
4. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. These vias help dissipate the heat generated by the OPA1632 IC, and may be larger than the 13mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
5. Connect all holes to the internal ground plane.
6. When connecting these holes to the plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the OPA1632 PowerPAD package should make their connection to the internal plane with a complete connection around the entire circumference of the plated-through hole.
7. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
8. Apply solder paste to the exposed thermal pad area and all of the IC terminals.

With these preparatory steps in place, the IC is simply placed in position and runs through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

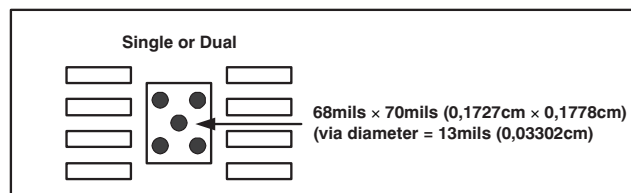


Figure 14. PowerPAD PCB Etch and Via Pattern

POWER DISSIPATION AND THERMAL CONSIDERATIONS

The OPA1632 does not have thermal shutdown protection. Take care to assure that the maximum junction temperature is not exceeded. Excessive junction temperature can degrade performance or cause permanent damage. For best performance and reliability, assure that the junction temperature does not exceed +125°C.

The thermal characteristics of the device are dictated by the package and the circuit board. Maximum power dissipation for a given package can be calculated using the following formula:

$$P_{DMax} = \frac{T_{Max} - T_A}{\theta_{JA}}$$

where:

- P_{DMax} is the maximum power dissipation in the amplifier (W)
- T_{Max} is the absolute maximum junction temperature (°C)
- T_A is the ambient temperature (°C)
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- θ_{JC} is the thermal coefficient from the silicon junctions to the case (°C/W)
- θ_{CA} is the thermal coefficient from the case to ambient air (°C/W)

For systems where heat dissipation is more critical, the OPA1632 is offered in an MSOP-8 with PowerPAD. The thermal coefficient for the MSOP PowerPAD (DGN) package is substantially improved over the traditional SO package. Maximum power dissipation levels are depicted in Figure 15 for the two packages. The data for the DGN package assume a board layout that follows the PowerPAD layout guidelines.

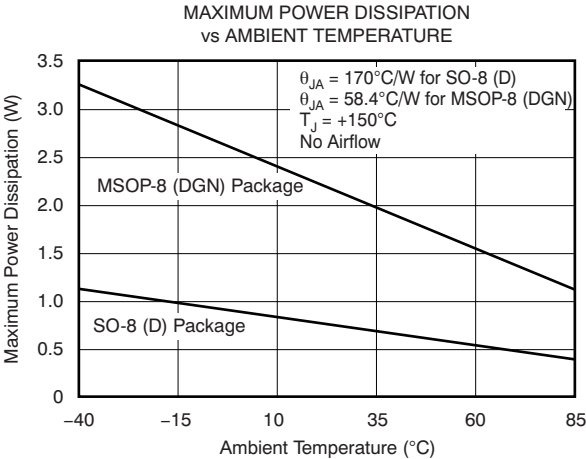


Figure 15. Maximum Power Dissipation vs Ambient Temperature

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September, 2006) to Revision B	Page
• Updated document format to align with current standards	1
• Changed points 1 and 5 of <i>PowerPAD PCB Layout Considerations</i> section	9

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA1632D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	OPA 1632	Samples
OPA1632DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	OPA 1632	Samples
OPA1632DGN	ACTIVE	MSOP- PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	1632	Samples
OPA1632DGNG4	ACTIVE	MSOP- PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	1632	Samples
OPA1632DGNR	ACTIVE	MSOP- PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	1632	Samples
OPA1632DGNG4	ACTIVE	MSOP- PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	1632	Samples
OPA1632DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	OPA 1632	Samples
OPA1632DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	OPA 1632	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA1632DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA1632DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA1632DGNR	MSOP-PowerPAD	DGN	8	2500	364.0	364.0	27.0
OPA1632DR	SOIC	D	8	2500	367.0	367.0	35.0

DGN (S-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-187 variation AA-T

PowerPAD is a trademark of Texas Instruments.

DGN (S-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

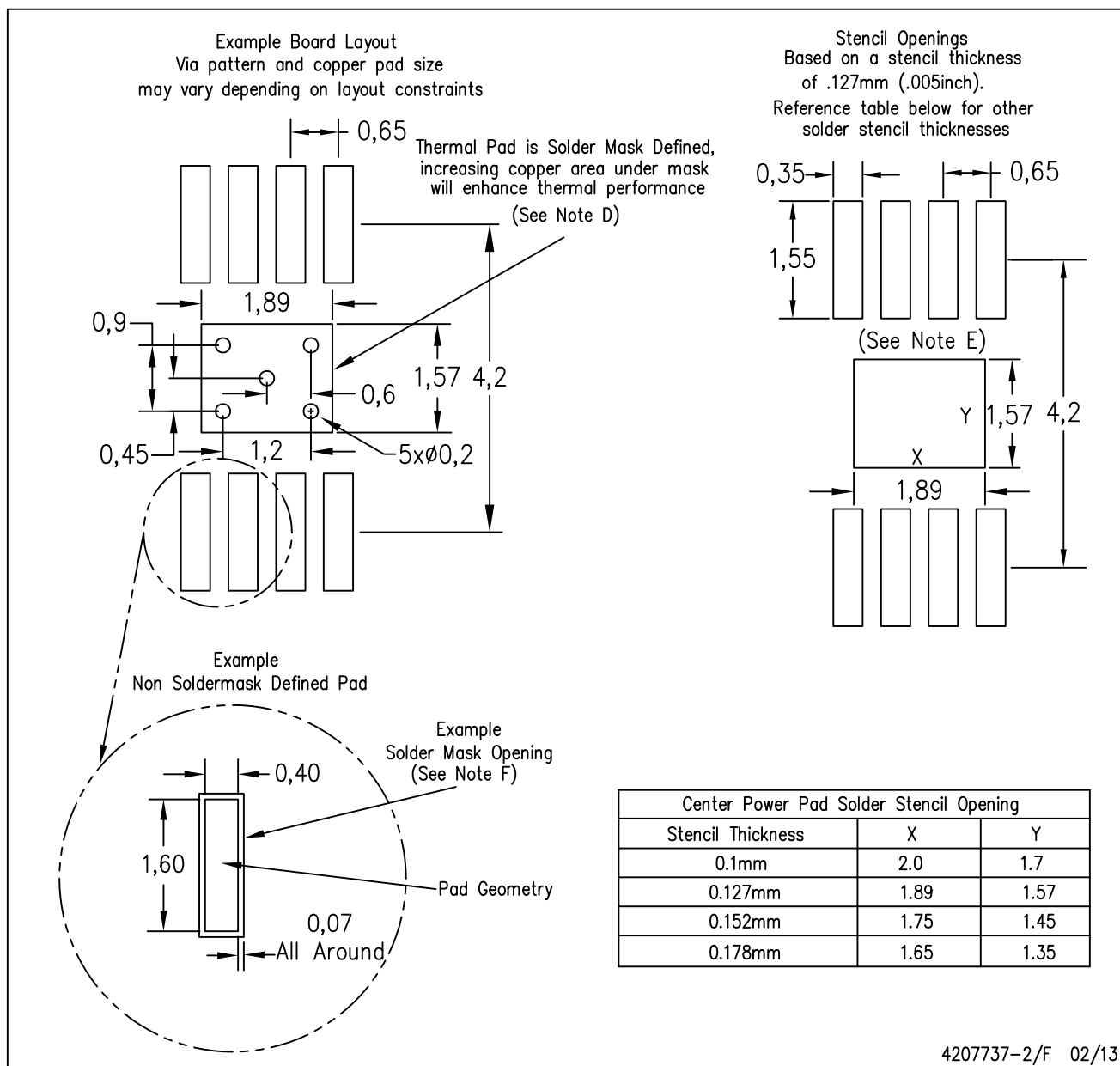
4206323-2/1 12/11

NOTE: All linear dimensions are in millimeters

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DGN (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE



4207737-2/F 02/13

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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