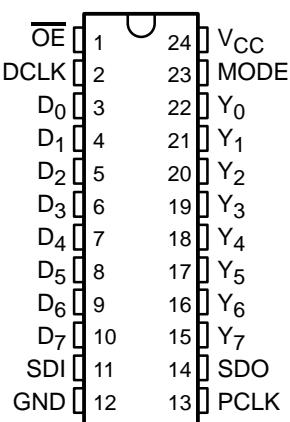


- Function, Pinout, and Drive Compatible With FCT, F Logic, and AM29818
- Reduced V_{OH} (Typically = 3.3 V) Version of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- 8-Bit Pipeline and Shadow Register
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- CY29FCT818CT
 - 64-mA Output Sink Current
 - 32-mA Output Source Current
- CY29FCT818ATDMB
 - 20-mA Output Sink Current
 - 3-mA Output Source Current
- 3-State Outputs

D, P, Q, OR SO PACKAGE
(TOP VIEW)



description

The CY29FCT818T contains a high-speed 8-bit general-purpose data pipeline register and a high-speed 8-bit shadow register. The general-purpose register can be used in an 8-bit-wide data path for a normal system application. The shadow register is designed for applications such as diagnostics in sequential circuits, where it is desirable to load known data at a specific location in the circuit and to read the data at that location.

The shadow register can load data from the output of the device, and can be used as a right-shift register with bit-serial input (SDI) and output (SDO), using DCLK. The data register input is multiplexed to enable loading from the shadow register or from the data input pins, using PCLK. Data can be loaded simultaneously from the shadow register to the pipeline register, and from the pipeline register to the shadow register, provided setup-time and hold-time requirements are satisfied, with respect to the two independent clock inputs.

In a typical application, the general-purpose register in this device replaces an 8-bit data register in the normal data path of a system. The shadow register is placed in an auxiliary bit-serial loop that is used for diagnostics. During diagnostic operation, data is shifted serially into the shadow register, then transferred to the general-purpose register to load a known value into the data path. To read the contents at that point in the data path, the data is transferred from the data register into the shadow register, then shifted serially in the auxiliary diagnostic loop to make it accessible to the diagnostics controller. This data then is compared with the expected value to diagnose faulty operation of the sequential circuit.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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CY29FCT818T
DIAGNOSTIC SCAN REGISTER
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ORDERING INFORMATION

TA	PACKAGE [†]		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	DIP – P	Tube	6	CY29FCT818CTPC	CY29FCT818CTPC
	QSOP – Q	Tape and reel	6	CY29FCT818CTQCT	29FCT818C
	SOIC – SO	Tube	6	CY29FCT818CTSOC	29FCT818C
		Tape and reel	6	CY29FCT818CTSOCT	
–55°C to 125°C	CDIP – D	Tube	12	CY29FCT818ATDMB	

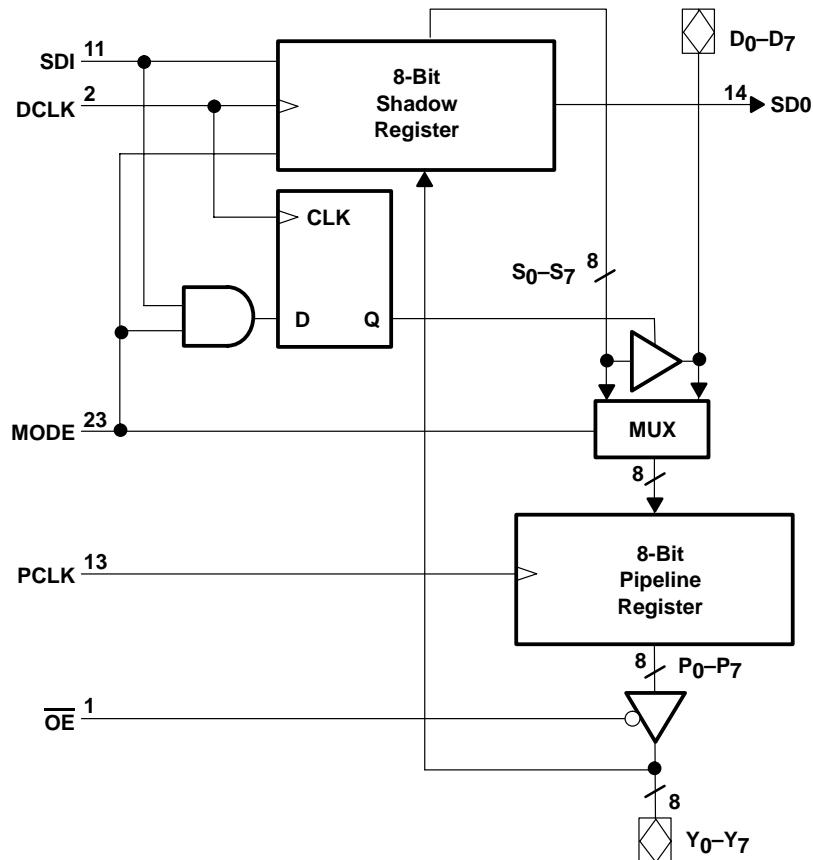
[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS				OUTPUT SDO	SHADOW REGISTER	PIPELINE REGISTER	OPERATION
MODE	SDI	DCLK	PCLK				
L	X	↑	X	S ₇	S ₀ ←SDI S _i ←S _{i-1}	NA	Serial shift; D ₇ –D ₀ output disabled
L	X	X	↑	S ₇	NA	P _i ←D _i	Load pipeline register from data input
H	L	↑	X	L	S _i ←Y _i	NA	Load shadow register from Y output
H	H	↑	X	H	Hold	NA	Hold shadow register; D ₇ –D ₀ output enabled
H	X	X	↑	SDI	NA	P _i ←S _i	Load pipeline register from shadow register

H = High logic level, L = Low logic level, X = Don't care, ↑ Low-to-high transition, ← = Transfer direction, NA = Not applicable

logic diagram



absolute maximum rating over operating free-air temperature range (unless otherwise noted)†

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The package thermal impedance is calculated in accordance with JESD 51-3.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 3)

		CY29FCT818ATDMB			CY29FCT818T			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			-3			-32	mA
I _{OL}	Low-level output current			20			64	mA
T _A	Operating free-air temperature	-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	CY29FCT818ATDMB			CY29FCT818T			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = 4.5 V, I _{IN} = -18 mA		-0.7	-1.2				V
	V _{CC} = 4.75 V, I _{IN} = -18 mA					-0.7	-1.2	
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -3 mA	2.4	3.3					V
	V _{CC} = 4.75 V V _{CC} = 4.75 V	I _{OH} = -32 mA			2			
		I _{OH} = -15 mA			2.4	3.3		
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 20 mA	0.3	0.55					V
	V _{CC} = 4.75 V, I _{OL} = 64 mA				0.3	0.55		
V _{hys}	All inputs	0.2			0.2			V
I _I	V _{CC} = 5.5 V, V _{IN} = V _{CC}			5				µA
	V _{CC} = 5.25 V, V _{IN} = V _{CC}					5		
I _{IH}	V _{CC} = 5.5 V, V _{IN} = 2.7 V		±1					µA
	V _{CC} = 5.25 V, V _{IN} = 2.7 V					±1		
I _{IL}	V _{CC} = 5.5 V, V _{IN} = 0.5 V		±1					µA
	V _{CC} = 5.25 V, V _{IN} = 0.5 V					±1		
I _{OZH}	V _{CC} = 5.5 V, V _{OUT} = 2.7 V		10					µA
	V _{CC} = 5.25 V, V _{OUT} = 2.7 V				10			
I _{OZL}	V _{CC} = 5.5 V, V _{OUT} = 0.5 V		-10					µA
	V _{CC} = 5.25 V, V _{OUT} = 0.5 V				-10			
I _{OS} ‡	V _{CC} = 5.5 V, V _{OUT} = 0 V	-60	-120	-225				mA
	V _{CC} = 5.25 V, V _{OUT} = 0 V				-60	-120	-225	
I _{off}	V _{CC} = 0 V, V _{OUT} = 4.5 V		±1			±1		µA
I _{CC}	V _{CC} = 5.5 V, V _{IN} ≤ 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V	0.2	1.5					mA
	V _{CC} = 5.25 V, V _{IN} ≤ 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V				0.2	1.5		
ΔI _{CC}	V _{CC} = 5.5 V, V _{IN} = 3.4 V§, f ₁ = 0, Outputs open	0.5	2					mA
	V _{CC} = 5.25 V, V _{IN} = 3.4 V§, f ₁ = 0, Outputs open				0.5	2		

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	CY29FCT818ATDMB			CY29FCT818T			UNIT	
		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX		
I _{CCD} [¶]	V _{CC} = 5.5 V, Outputs open, One input switching at 50% duty cycle, OE = GND, V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V		0.25					mA/ MHz	
	V _{CC} = 5.25 V, Outputs open, One input switching at 50% duty cycle, OE = GND, V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V						0.25		
I _C [#]	V _{CC} = 5.5 V, Outputs open, f ₀ = 10 MHz, OE = GND	One bit switching at f ₁ = 5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V		5.3			mA	
			V _{IN} = 3.4 V or GND		7.3				
		Eight bits and four controls switching at f ₁ = 5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V		17.8				
			V _{IN} = 3.4 V or GND		30.8				
	V _{CC} = 5.25 V, Outputs open, f ₀ = 10 MHz, OE = GND	One bit switching at f ₁ = 5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V				5.3	mA	
			V _{IN} = 3.4 V or GND				7.3		
		Eight bits and four controls switching at f ₁ = 5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V				17.8		
			V _{IN} = 3.4 V or GND				30.8		
C _i				5	10		5	10	pF
C _o				9	12		9	12	pF

[†] Typical values are at V_{CC} = 5 V, T_A = 25°C.

[¶] This parameter is derived for use in total power-supply calculations.

[#] I_C = I_{CC} + ΔI_{CC} × D_H × N_T + I_{CCD} (f₀/2 + f₁ × N₁)

Where:

I_C = Total supply current

I_{CC} = Power-supply current with CMOS input levels

ΔI_{CC} = Power-supply current for a TTL high input (V_{IN} = 3.4 V)

D_H = Duty cycle for TTL inputs high

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic current caused by an input transition pair (HLL or LHL)

f₀ = Clock frequency for registered devices, otherwise zero

f₁ = Input signal frequency

N₁ = Number of inputs changing at f₁

All currents are in milliamperes and all frequencies are in megahertz.

^{||} Values for these conditions are examples of the I_{CC} formula.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER		CY29FCT818AT		CY29FCT818CT		UNIT
		MIN	MAX	MIN	MAX	
t_w	Pulse width	PCLK high and low	15	5	5	ns
		DCLK high and low	25	5	5	
t_{su}	Setup time	D before PCLK \uparrow	6	2	2	ns
		MODE before PCLK \uparrow	15	3.5	3.5	
		Y before DCLK \uparrow	5	2	2	
		MODE before DCLK \uparrow	12	3.5	3.5	
		SDI before DCLK \uparrow	10	3.5	3.5	
		DCLK before PCLK \uparrow	15	3.5	3.5	
		PCLK before DCLK \uparrow	45	8.5	8.5	
t_h	Hold time	D after PCLK \uparrow	2	1.5	1.5	ns
		MODE after PCLK \uparrow	0	0	0	
		Y after DCLK \uparrow	5	1.5	1.5	
		MODE after DCLK \uparrow	5	1.5	1.5	
		SDI after DCLK \uparrow	0	0	0	

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY29FCT818AT		CY29FCT818CT		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	PCLK	Y		12		6	ns
	MODE	SDO		18		7.2	
	SDI	SDO		18		7.1	
	DCLK	SDO		30		7.2	
t_{PZL}	\overline{OE}	Y		20		8	ns
	DCLK	D		35		9	
t_{PZH}	\overline{OE}	Y		20		8.5	ns
	DCLK	D		30		9	
t_{PLZ}	\overline{OE}	Y		20		5.5	ns
	DCLK	D		45		5.5	
t_{PHZ}	\overline{OE}	Y		30		8	ns
	DCLK	D		90		8	

PARAMETER MEASUREMENT INFORMATION

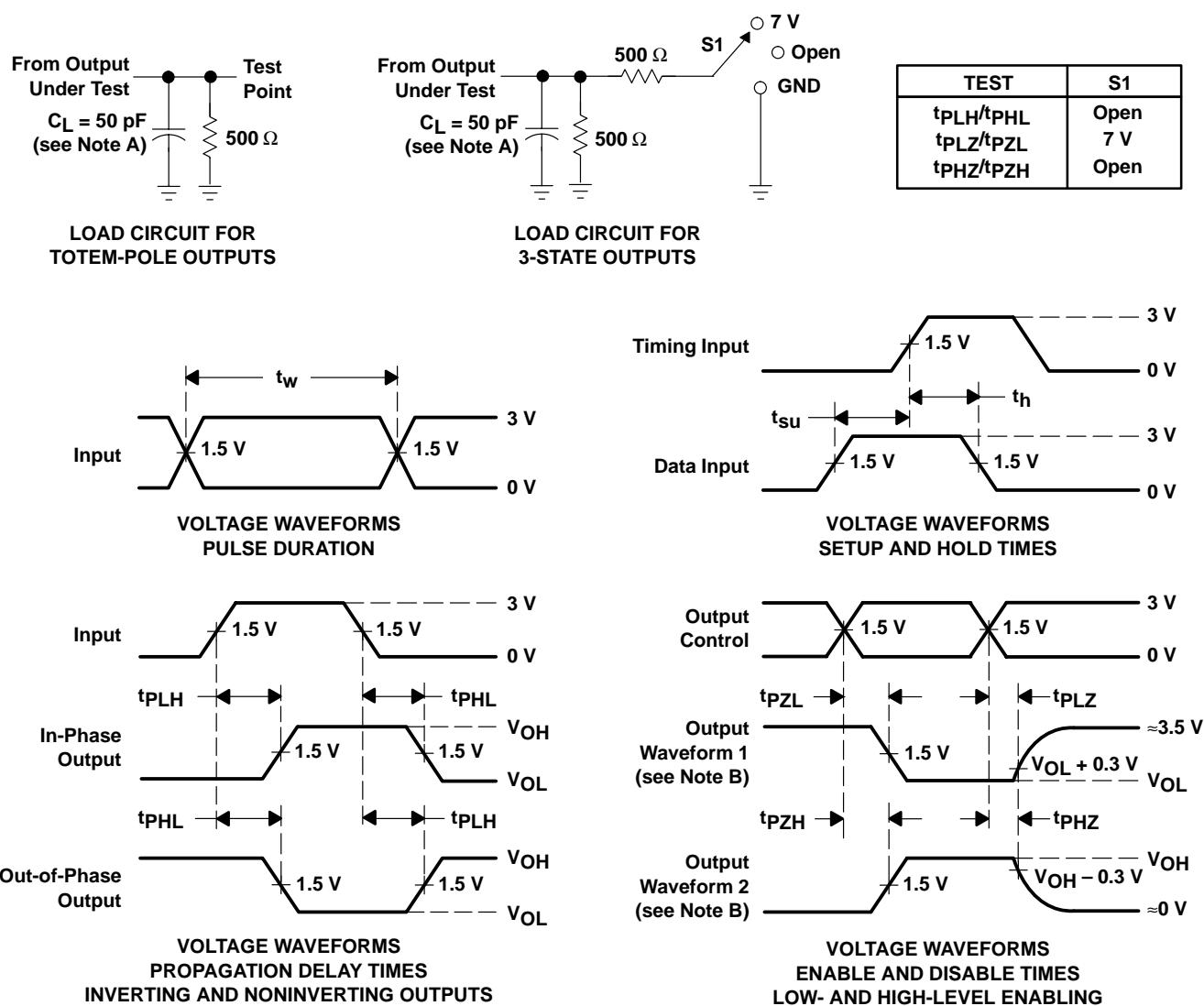


Figure 1. Load Circuit and Voltage Waveforms

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. The outputs are measured one at a time with one input transition per measurement.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9682701Q3A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9682701Q3A	Samples
5962-9682701QLA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9682701QL A CY29FCT818ATDM B	Samples
CY29FCT818ATDMB	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9682701QL A CY29FCT818ATDM B	Samples
CY29FCT818CTSOCT	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	29FCT818C	Samples
CY29FCT818CTSOCTE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	29FCT818C	Samples
CY29FCT818CTSOCTG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	29FCT818C	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

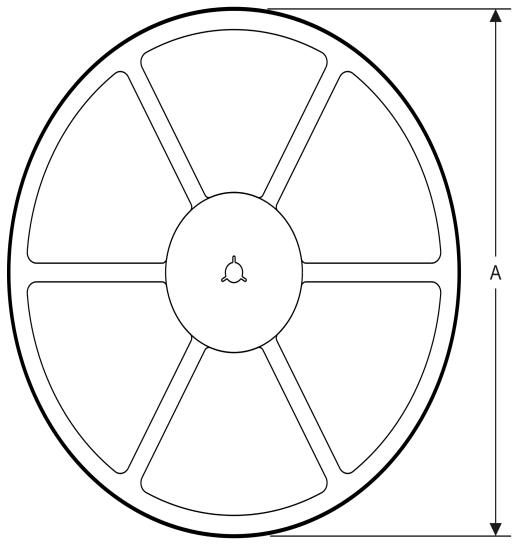
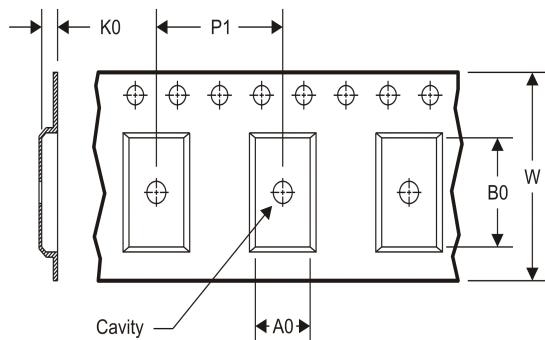
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

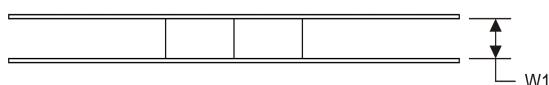
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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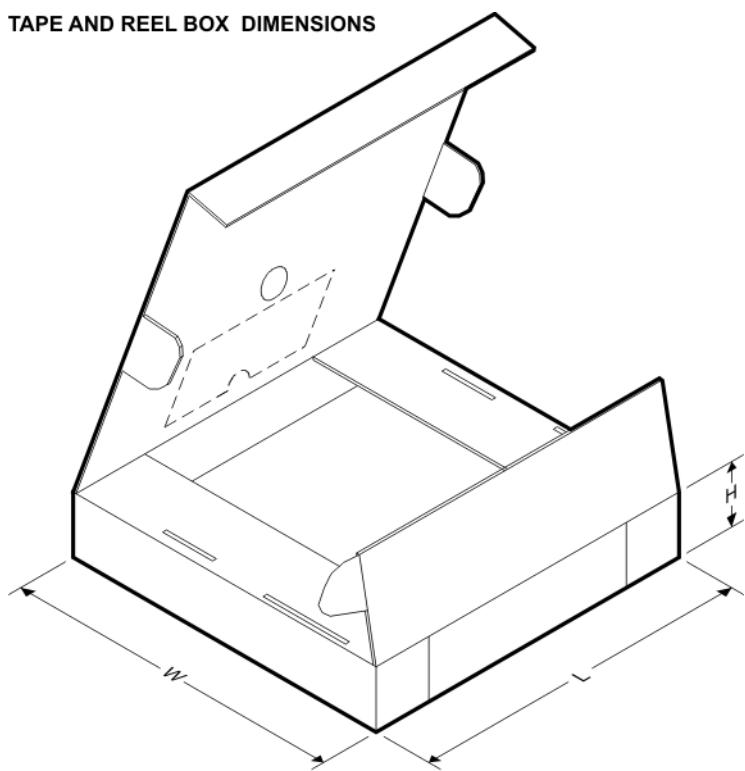
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers


TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY29FCT818CTSOCT	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

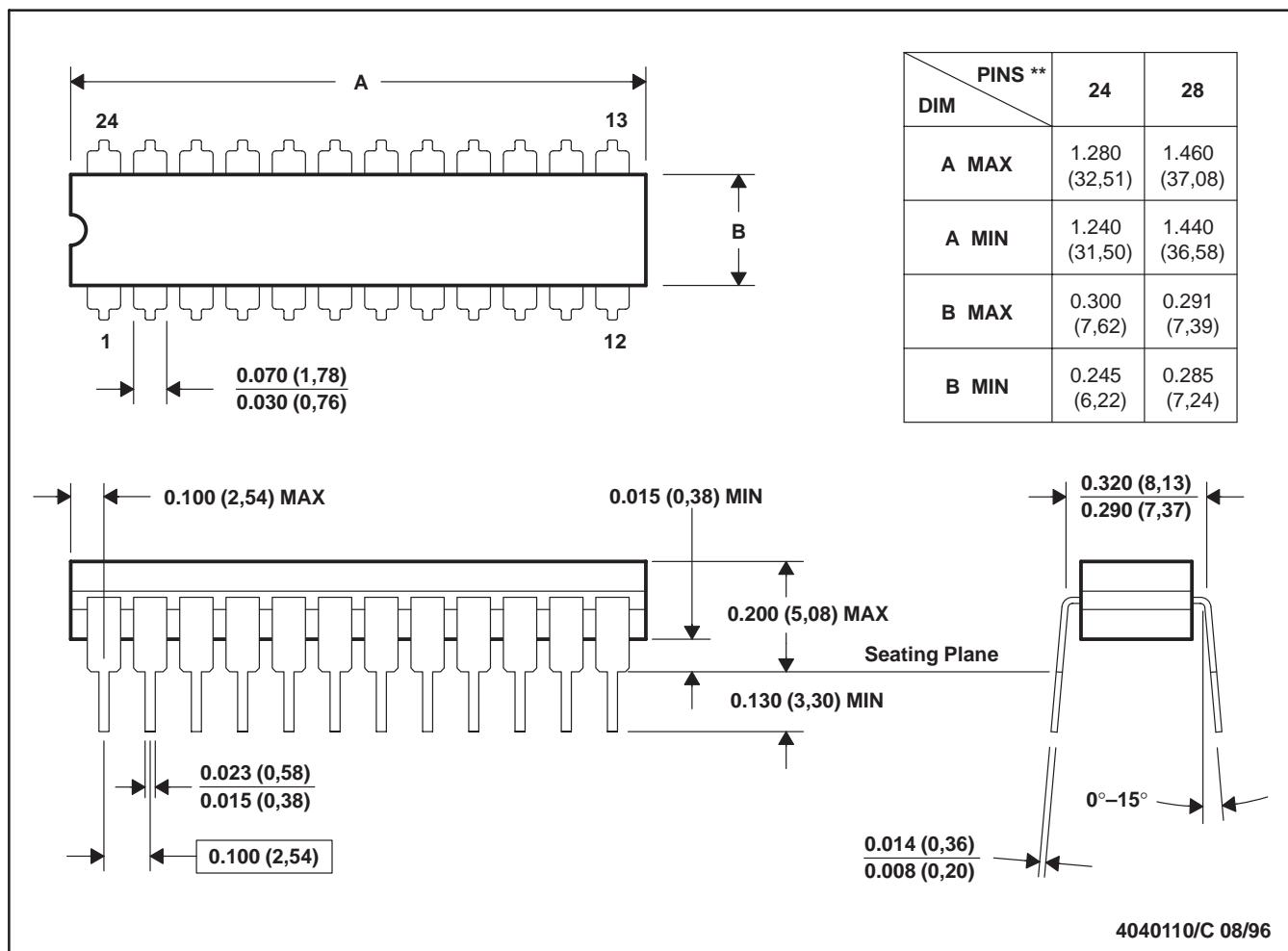
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY29FCT818CTSOCT	SOIC	DW	24	2000	367.0	367.0	45.0

JT (R-GDIP-T**)

24 LEADS SHOWN

CERAMIC DUAL-IN-LINE

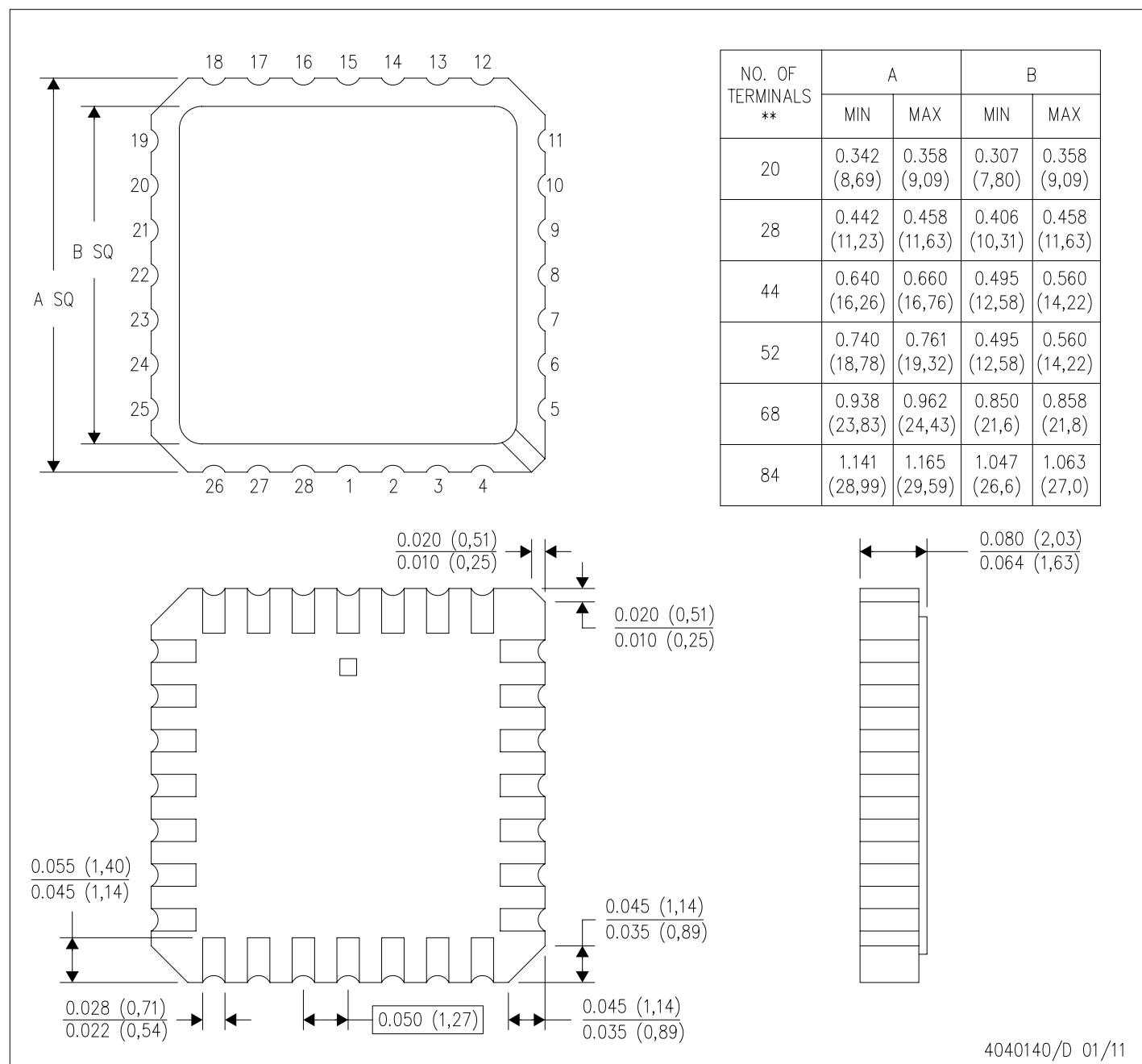


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER

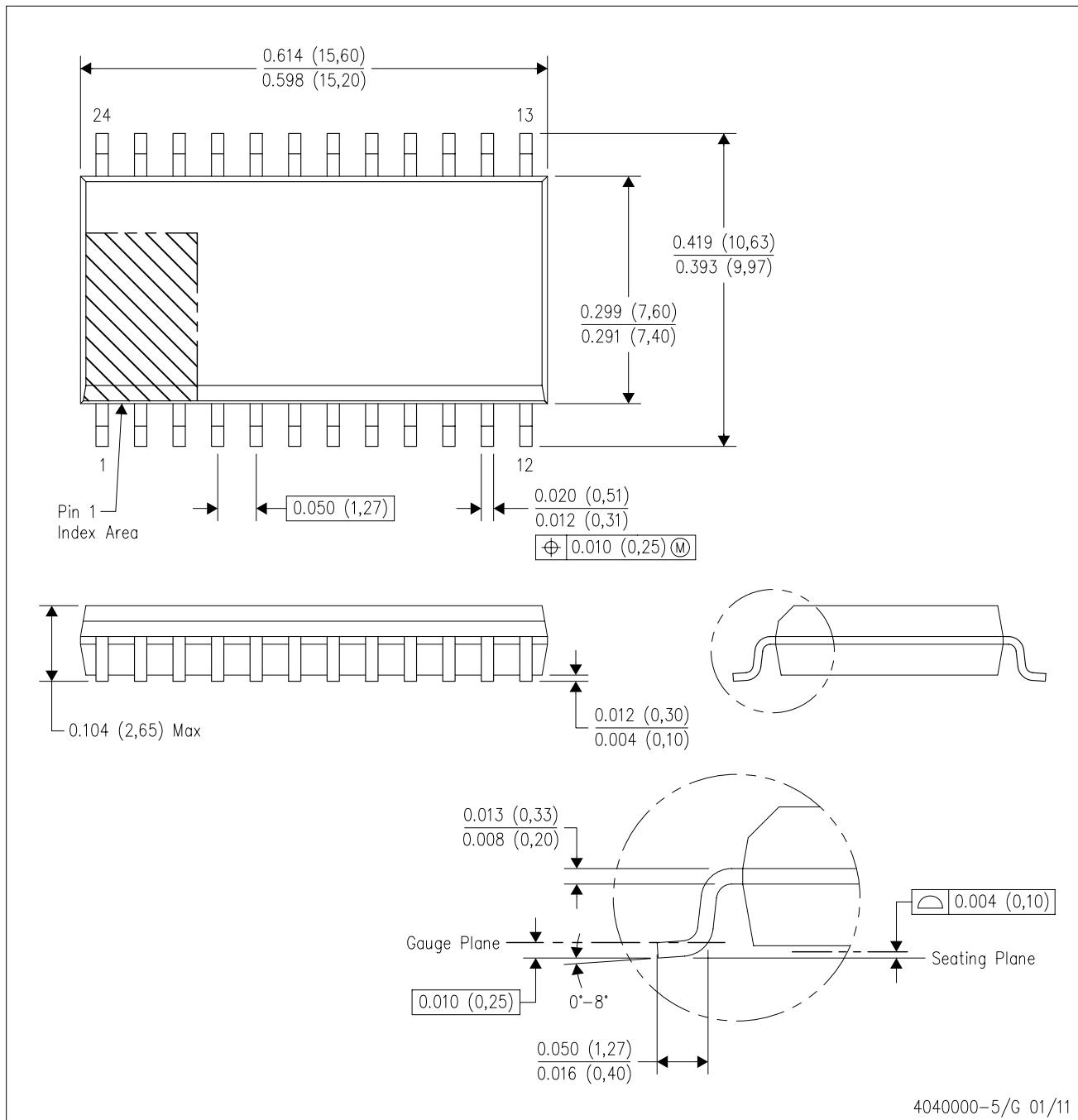


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. Falls within JEDEC MS-004

4040140/D 01/11

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
 - Falls within JEDEC MS-013 variation AD.

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