400MHz Slew Enhanced VFAs

EL5202, EL5203

The EL5202 and EL5203 are dual, high-speed VFAs based on a CFA architecture. This gives the typical high slew rate benefits of a CFA family along with the stability and ease of use associated with the VFA type architecture. With slew rates of 3500V/µs, these devices enable the use of voltage feedback amplifiers in a space where the only alternative has been current feedback amplifiers. This family also includes single, dual, and triple versions with 750MHz bandwidths; please see the EL5104 through EL5304 data sheet for details.

Both devices operate on single 5V or ±5V supplies from minimum supply current. The EL5202 also features an output enable function, which can be used to put the output in to a high-impedance mode. This allows the outputs of multiple amplifiers to be tied together for use in multiplexing applications.

Typical applications for these families include cable driving, filtering, A/D and D/A buffering, multiplexing and summing within video, communications, and instrumentation designs.

Features

- Operates off 3V, 5V, or ±5V supplies
- Power-down to 13µA (EL5202)
- -3dB bandwidth = 400MHz
- ±0.1dB bandwidth = 35MHz
- Low supply current = 5mA per amplifier
- Slew rate = 3500V/µs
- Low offset voltage = 5mV max
- Output current = 150mA
- A_{VOL} = 2000
- Differential gain/phase = 0.01%/0.01°
- Pb-free (RoHS compliant)

Applications

- Video amplifiers
- PCMCIA applications
- A/D drivers
- Line drivers
- Portable computers
- High speed communications
- RGB applications
- Broadcast equipment
- Active filtering

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
1-888-INTERSIL or 1-888-468-3774 | Copyright Intersil Americas LLC 2002-2008, 2014. All Rights Reserved
Intersil (and design) is a trademark owned by Intersil Corporation or one of its subsidiaries.
All other trademarks mentioned are the property of their respective owners.

Ordering Information

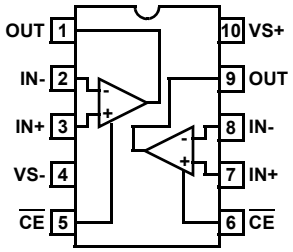
PART NUMBER (Note 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG DWG. #
EL5202IYZ (Note 2)	BAAAD	-40 to +85	10 Ld MSOP (3.0mm)	M10.118A
EL5202IYZ-T7 (Notes 1, 2)	BAAAD	-40 to +85	10 Ld MSOP (3.0mm)	M10.118A
EL5202IYZ-T13 (Notes 1, 2)	BAAAD	-40 to +85	10 Ld MSOP (3.0mm)	M10.118A
EL5203ISZ (Note 2)	5203ISZ	-40 to +85	8 Ld SOIC (150 mil)	M8.15E
EL5203ISZ-T7 (Notes 1, 2)	5203ISZ	-40 to +85	8 Ld SOIC (150 mil)	M8.15E
EL5203ISZ-T13 (Notes 1, 2)	5203ISZ	-40 to +85	8 Ld SOIC (150 mil)	M8.15E
EL5203IYZ (Note 2)	BAAAE	-40 to +85	8 Ld MSOP (3.0mm)	M8.118A
EL5203IYZ-T7 (Notes 1, 2)	BAAAE	-40 to +85	8 Ld MSOP (3.0mm)	M8.118A
EL5203IYZ-T13 (Notes 1, 2)	BAAAE	-40 to +85	8 Ld MSOP (3.0mm)	M8.118A

NOTES:

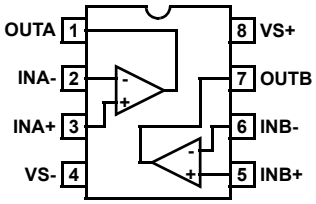
1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see product information page for EL5202, EL5203 . For more information on MSL, please see tech brief TB363.

Pin Configurations

EL5202
(10 LD MSOP)
TOP VIEW



EL5203
(8 LD SOIC, MSOP)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage between V_S+ and V_S- 13.2V
Maximum Supply Slew Rate between V_S+ and V_S- 1V/µs
Input Voltage ..... $\pm V_S$
Differential Input Voltage ..... ±4V
Maximum Continuous Output Current 80mA
Maximum Current into I_N+, I_N-, $\overline{CE}$ ..... ±5mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld MSOP Package (Notes 4, 5)	160	75
8 Ld SOIC Package (Notes 4, 5)	125	75
8 Ld MSOP Package (Notes 4, 5)	170	80

Storage Temperature Range ..... -65°C to +150°C
Ambient Operating Temperature Range ..... -40°C to +85°C
Operating Junction Temperature ..... +150°C
Pb-Free Reflow Profile ..... see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is taken at the package top center.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Specifications MV_S+ = +5V, V_S- = -5V, T_A = +25°C, R_L = 500Ω, $V_{\overline{CE}}$ = 0V, Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
V_{OS}	Offset Voltage			1	5	mV
TCV_{OS}	Offset Voltage Temperature Coefficient	Measured from T_{MIN} to T_{MAX}		10		µV/°C
IB	Input Bias Current	V_{IN} = 0V	-12	2	12	µA
I_{OS}	Input Offset Current	V_{IN} = 0V	-8	1	8	µA
TCI_{OS}	Input Bias Current Temperature Coefficient	Measured from T_{MIN} to T_{MAX}		50		nA/°C
PSRR	Power Supply Rejection Ratio	V_S = ±4.75V to ±5.25V	-70	-80		dB
CMRR	Common Mode Rejection Ratio	V_{CM} = -3V to 3.0V	-60	-80		dB
CMIR	Common Mode Input Range	Guaranteed by CMRR test	-3	±3.3	3	V
R_{IN}	Input Resistance	Common mode	200	400		kΩ
C_{IN}	Input Capacitance	SO package		1		pF
$I_{S,ON}$	Supply Current - Enabled, Per Amplifier		4.6	5.2	5.8	mA
$I_{S,OFF}$	Supply Current - Shut-down, Per Amplifier	V_S+	+1	+9	+25	µA
		V_S-	-25	-13	-1	µA
AVOL	Open Loop Gain	V_{OUT} = ±2.5V, R_L = 1kΩ to GND	58	66		dB
		V_{OUT} = ±2.5V, R_L = 150Ω to GND		60		dB
V_{OUT}	Output Voltage Swing	R_L = 1kΩ to GND	±3.5	±3.9		V
		R_L = 150Ω to GND	±3.4	±3.7		V
I_{OUT}	Output Current	A_V = 1, R_L = 10Ω to 0V	±80	±150		mA
$V_{\overline{CE}}$-ON	$\overline{CE}$ Pin Voltage for Power-up		(V_S+) -5		(V_S+) -3	V
$V_{\overline{CE}}$-OFF	$\overline{CE}$ Pin Voltage for Shut-down		(V_S+) -1		V_S+	V
$I_{\overline{CE}}$-ON	$\overline{CE}$ Pin Current - Enabled	$\overline{CE}$ = 0V	-1	0	+1	µA
$I_{\overline{CE}}$-OFF	$\overline{CE}$ Pin Current - Disabled	$\overline{CE}$ = +5V	1	14	25	µA

Closed Loop AC Electrical Specifications

$V_S+ = +5V$, $V_S- = -5V$, $T_A = +25°C$, $V_{\overline{CE}} = 0V$, $A_V = +1$, $R_F = 0\Omega$, $R_L = 150\Omega$ to GND, Unless Otherwise Specified. (Note 6)

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
BW	-3dB Bandwidth ($V_{OUT} = 400mV_{P-P}$)	$A_V = 1$, $R_F = 0\Omega$		400		MHz
SR	Slew Rate	$A_V = +2$, $R_L = 100\Omega$, $V_{OUT} = -3V$ to $+3V$	1100	2200	5000	V/µs
		$R_L = 500\Omega$, $V_{OUT} = -3V$ to $+3V$		4000		V/µs
t_R,t_F	Rise Time, Fall Time	±0.1V step		2.8		ns
OS	Overshoot	±0.1V step		10		%
t_S	0.1% Settling Time	$V_S = ±5V$, $R_L = 500\Omega$, $A_V = 1$, $V_{OUT} = ±3V$		20		ns
dG	Differential Gain (Note 7)	$A_V = 2$, $R_F = 1k\Omega$		0.01		%
dP	Differential Phase (Note 7)	$A_V = 2$, $R_F = 1k\Omega$		0.01		°
e_N	Input Noise Voltage	f = 10kHz		12		$nV/\sqrt{Hz}$
i_N	Input Noise Current	f = 10kHz		11		$pA/\sqrt{Hz}$
t_{DIS}	Disable Time (Note 8)			50		ns
t_{EN}	Enable Time (Note 8)			25		ns

NOTES:

6. All AC tests are performed on a “warmed up” part, except slew rate, which is pulse tested.
7. Standard NTSC signal = $286mV_{P-P}$, f = 3.58MHz, as V_{IN} is swept from 0.6V to 1.314V.R_L is DC coupled.
8. Disable/Enable time is defined as the time from when the logic signal is applied to the $\overline{CE}$ pin to when the supply current has reached half its final value.
9. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves

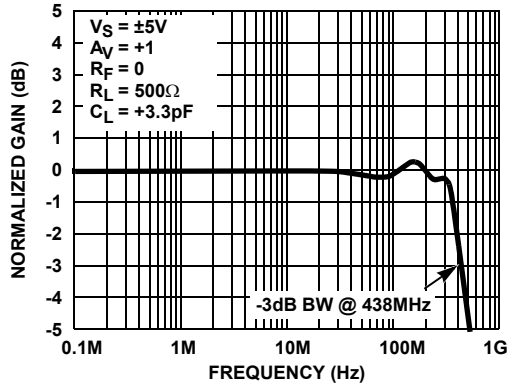


FIGURE 1. GAIN vs FREQUENCY (-3dB BANDWIDTH)

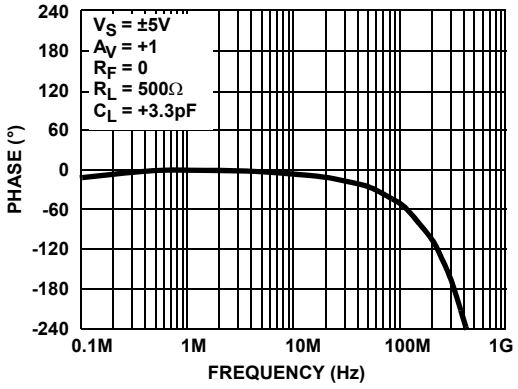


FIGURE 2. PHASE vs FREQUENCY

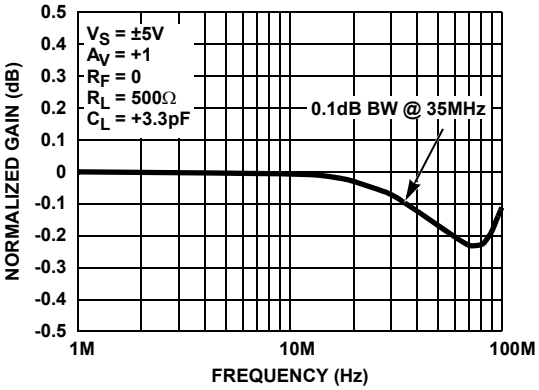


FIGURE 3. 0.1dB BANDWIDTH

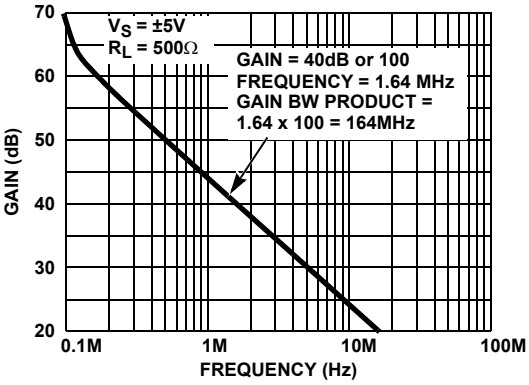


FIGURE 4. GAIN BANDWIDTH PRODUCT

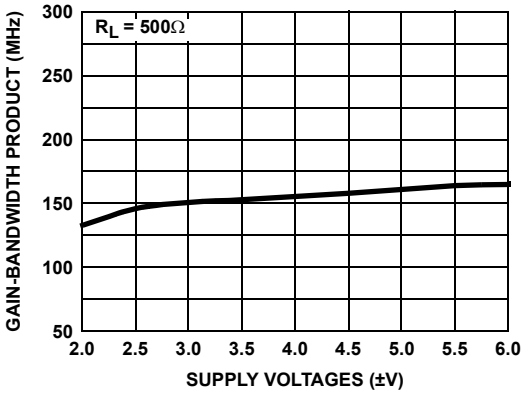


FIGURE 5. GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGES

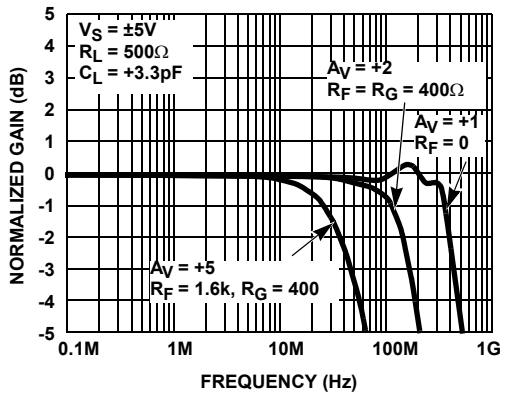


FIGURE 6. GAIN vs FREQUENCY FOR VARIOUS +A_V

Typical Performance Curves (Continued)

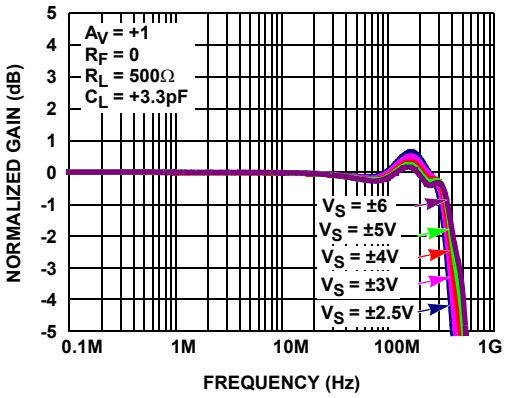


FIGURE 7. GAIN vs FREQUENCY FOR VARIOUS $\pm V_S$

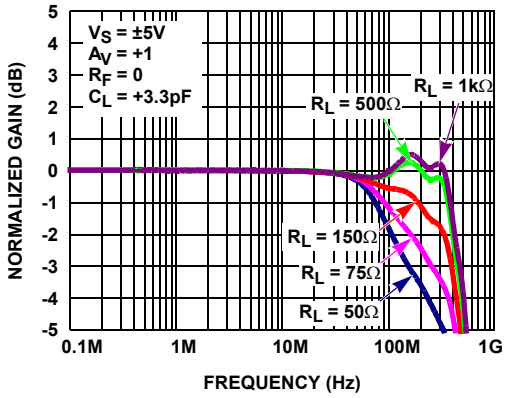


FIGURE 8. GAIN vs FREQUENCY FOR VARIOUS R_{LOAD} (A_V = +1)

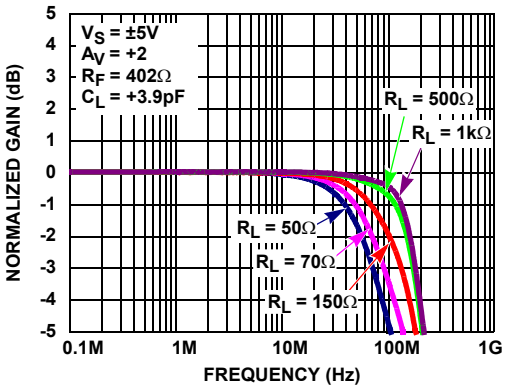


FIGURE 9. GAIN vs FREQUENCY FOR VARIOUS R_{LOAD} (A_V = +2)

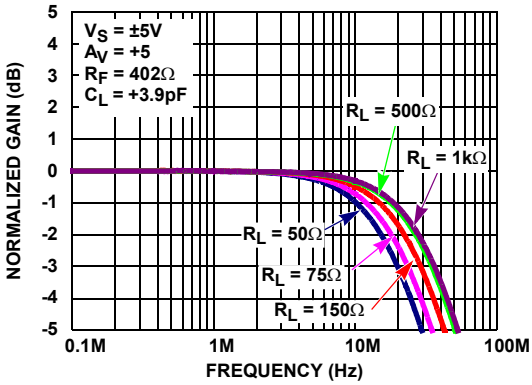


FIGURE 10. GAIN vs FREQUENCY FOR VARIOUS R_{LOAD} (A_V = +5)

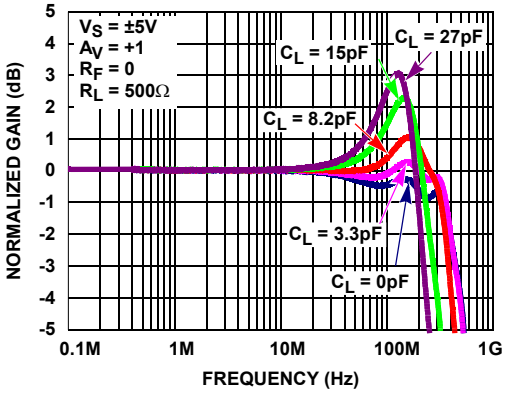


FIGURE 11. GAIN vs FREQUENCY FOR VARIOUS C_{LOAD} (A_V = +1)

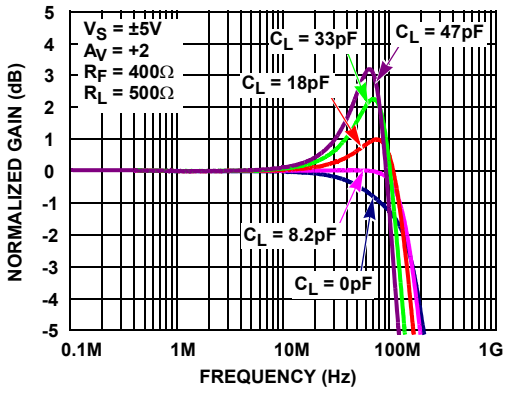


FIGURE 12. GAIN vs FREQUENCY FOR VARIOUS C_{LOAD} (A_V = +2)

Typical Performance Curves (Continued)

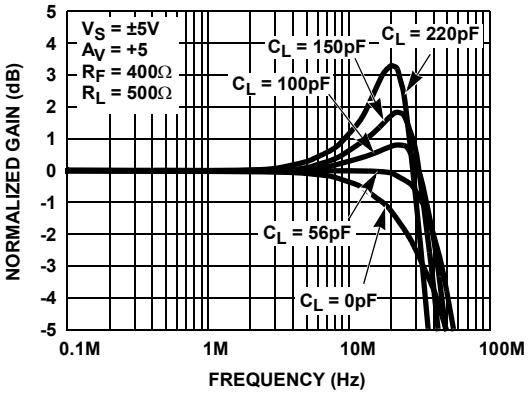


FIGURE 13. GAIN vs FREQUENCY FOR VARIOUS C_{LOAD} (A_V = +5)

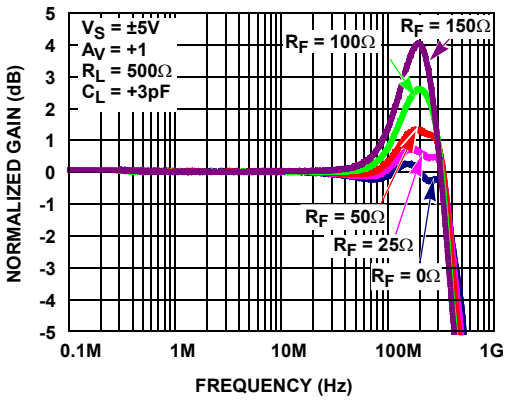


FIGURE 14. GAIN vs FREQUENCY FOR VARIOUS R_F (A_V = +1)

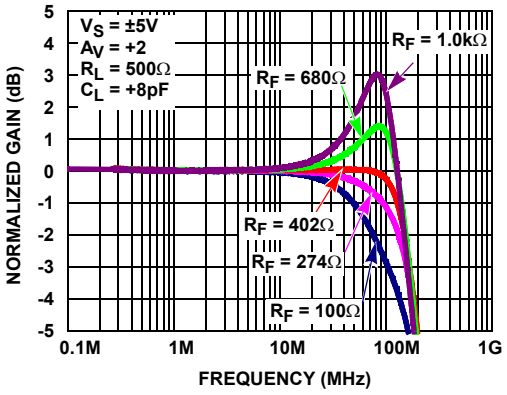


FIGURE 15. GAIN vs FREQUENCY FOR VARIOUS R_F (A_V = +2)

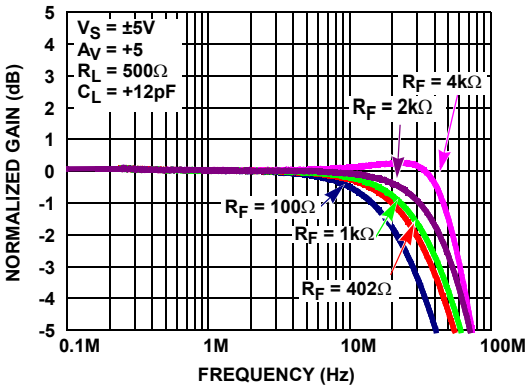


FIGURE 16. GAIN vs FREQUENCY FOR VARIOUS R_F (A_V = +5)

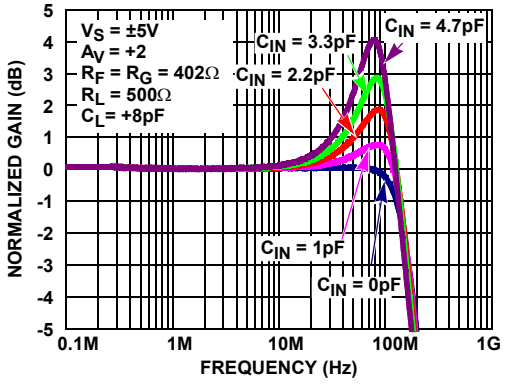


FIGURE 17. GAIN vs FREQUENCY FOR VARIOUS C_{IN}(-) (A_V = +2)

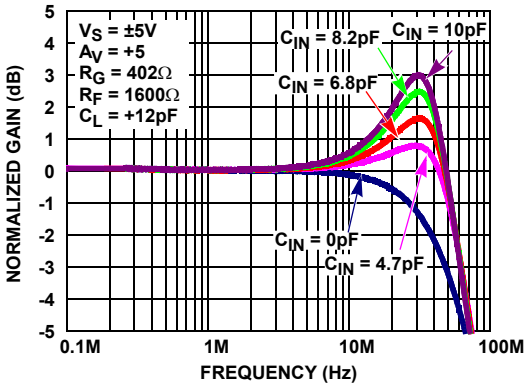


FIGURE 18. GAIN vs FREQUENCY FOR VARIOUS C_{IN}(-) (A_V = +5)

Typical Performance Curves (Continued)

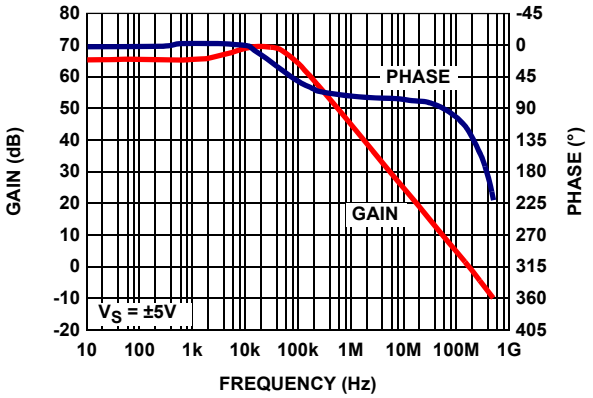


FIGURE 19. OPEN LOOP GAIN AND PHASE vs FREQUENCY

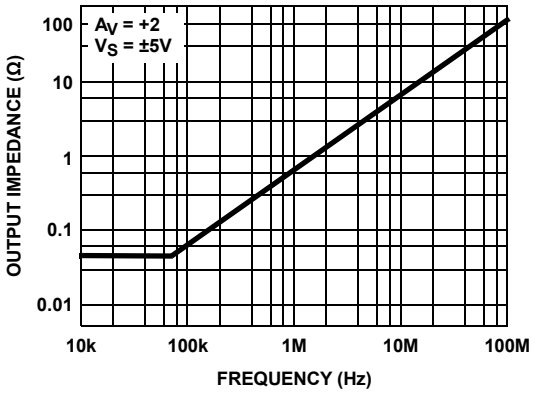


FIGURE 20. OUTPUT IMPEDANCE vs FREQUENCY

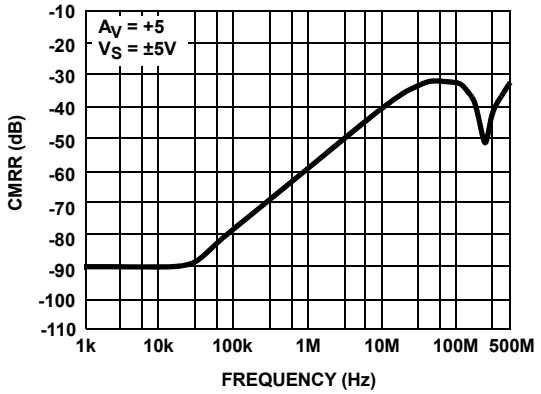


FIGURE 21. CMRR vs FREQUENCY

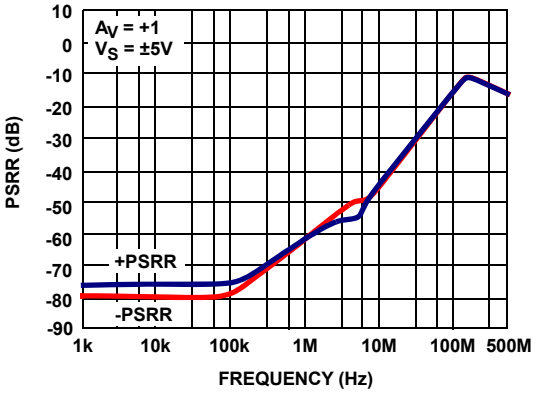


FIGURE 22. PSRR vs FREQUENCY

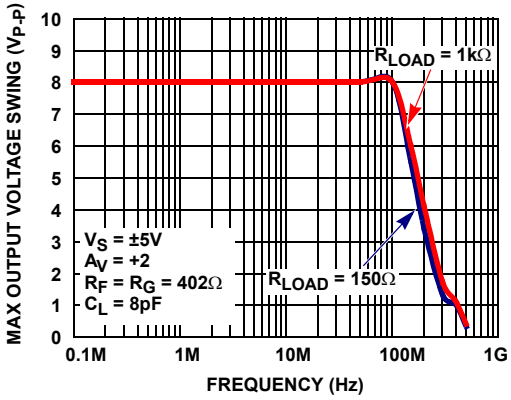


FIGURE 23. MAX OUTPUT VOLTAGE SWING vs FREQUENCY

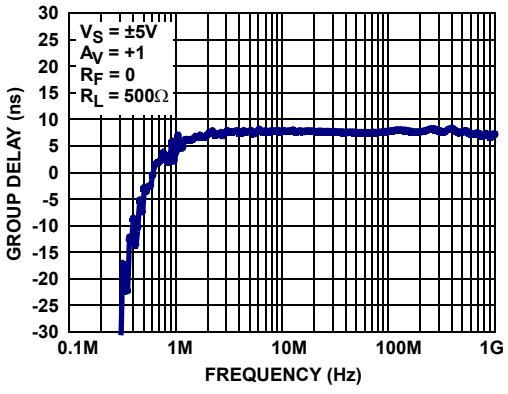


FIGURE 24. GROUP DELAY vs FREQUENCY

Typical Performance Curves (Continued)

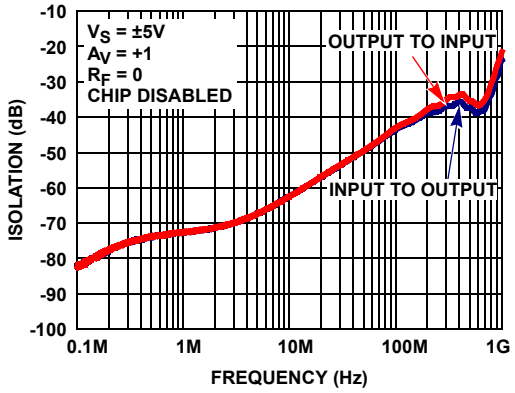


FIGURE 25. INPUT AND OUTPUT ISOLATION

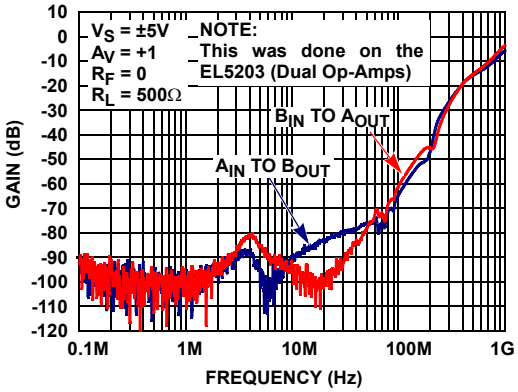


FIGURE 26. CHANNEL-TO-CHANNEL ISOLATION

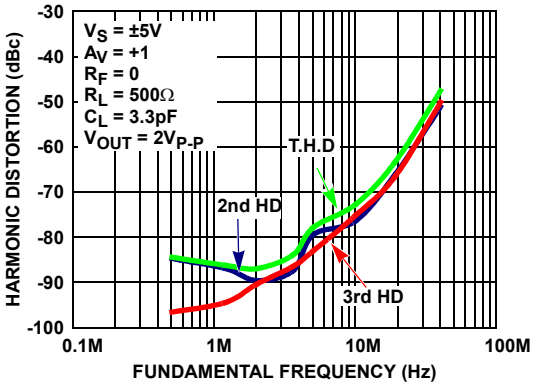


FIGURE 27. HARMONIC DISTORTION vs FREQUENCY

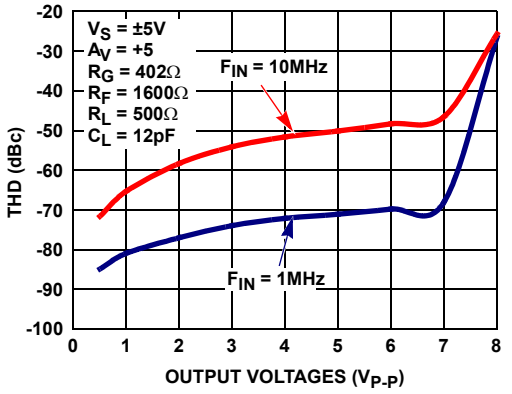


FIGURE 28. TOTAL HARMONIC DISTORTION vs OUTPUT VOLTAGES

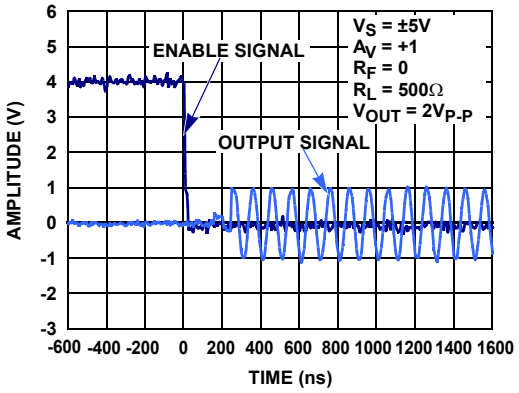


FIGURE 29. TURN-ON TIME

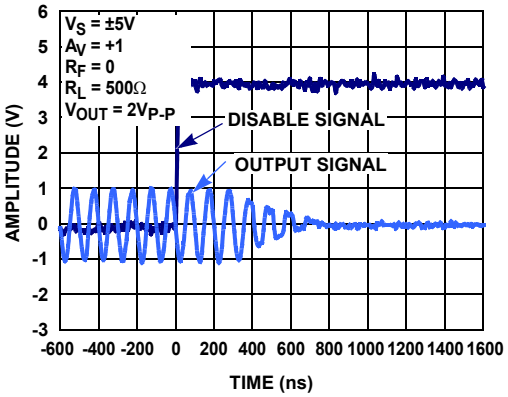


FIGURE 30. TURN-OFF TIME

Typical Performance Curves (Continued)

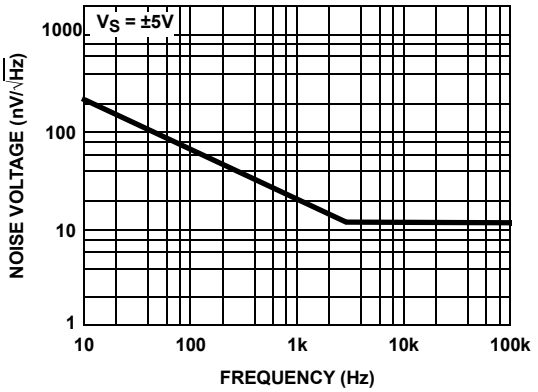


FIGURE 31. EQUIVALENT NOISE VOLTAGE vs FREQUENCY

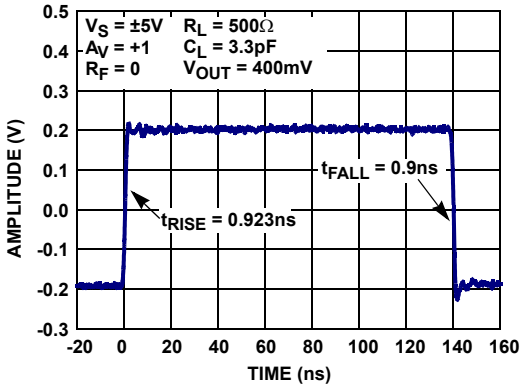


FIGURE 32. SMALL SIGNAL STEP RESPONSE RISE AND FALL TIME

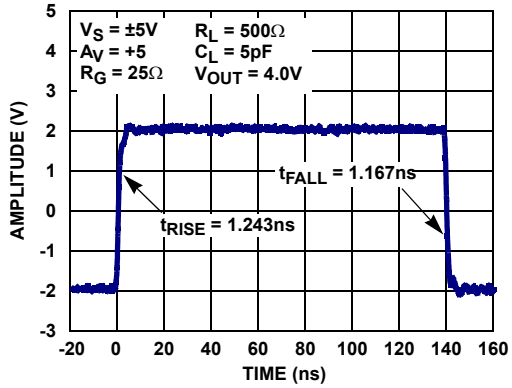


FIGURE 33. LARGE SIGNAL STEP RESPONSE RISE AND FALL TIME

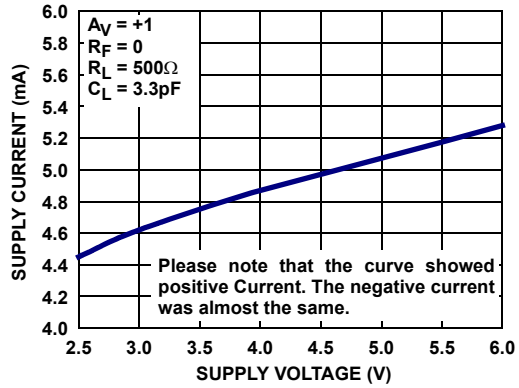


FIGURE 34. SUPPLY CURRENT vs SUPPLY VOLTAGE

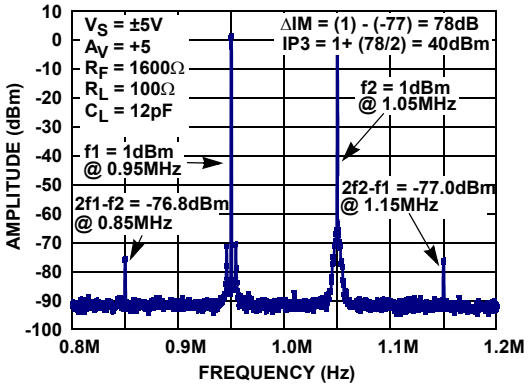


FIGURE 35. THIRD ORDER IMD INTERCEPT (IP3)

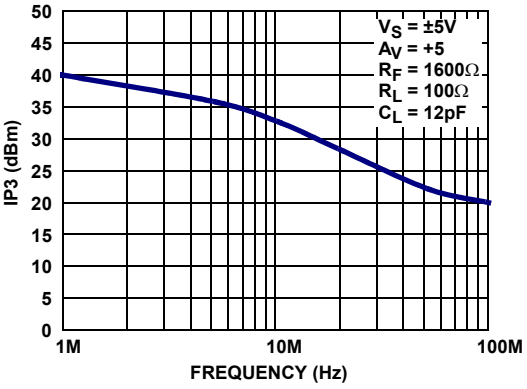


FIGURE 36. THIRD ORDER IMD INTERCEPT vs FREQUENCY

For additional products, see www.intersil.com/en/products.html

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

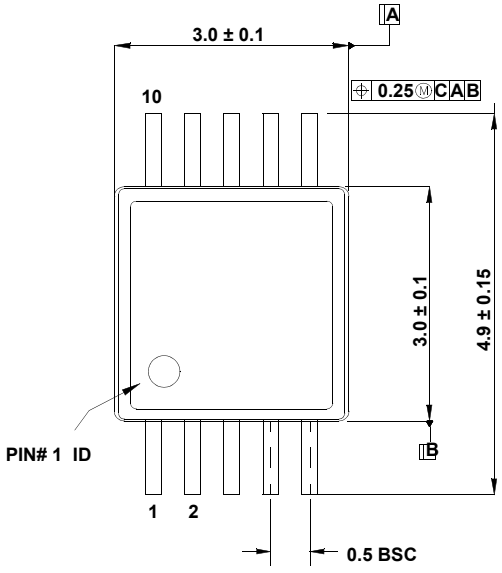
For information regarding Intersil Corporation and its products, see www.intersil.com

Package Outline Drawing

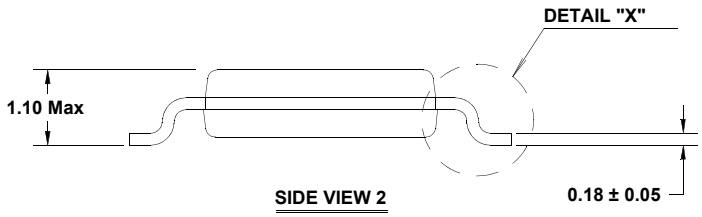
M10.118A (JEDEC MO-187-BA)

10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE (MSOP)

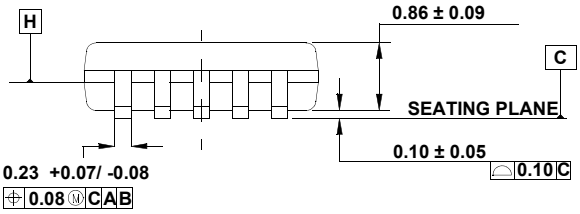
Rev 0, 9/09



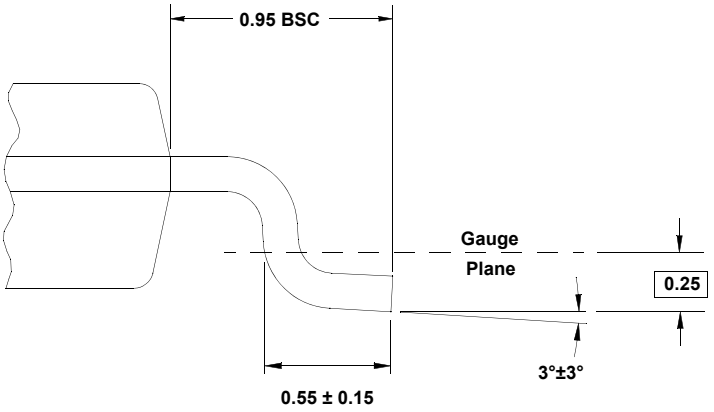
TOP VIEW



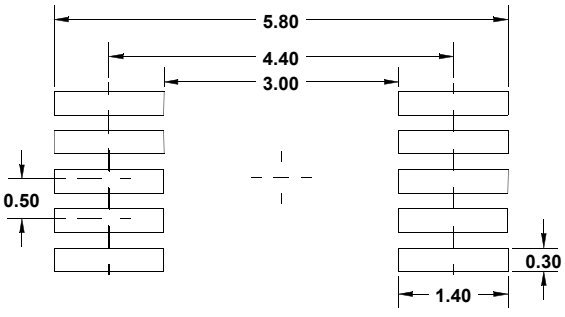
SIDE VIEW 2



SIDE VIEW 1



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

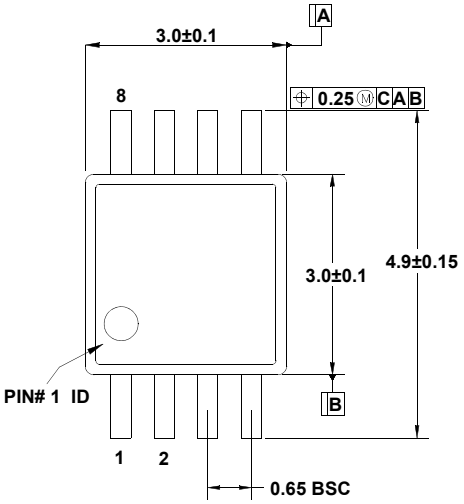
NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.25mm max per side are not included.
5. Dimensions “D” and “E1” are measured at Datum Plane “H”.
6. This replaces existing drawing # MDP0043 MSOP10L.

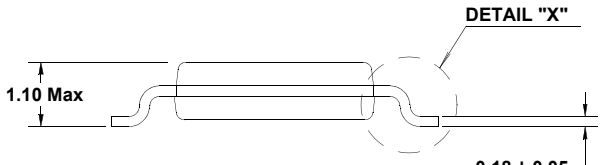
Package Outline Drawing

M8.118A

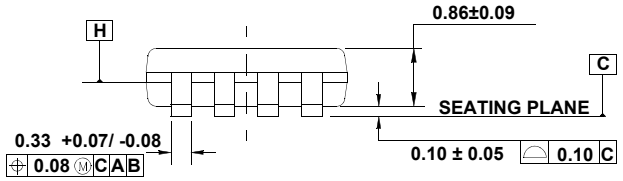
8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE (MSOP)
Rev 0, 9/09



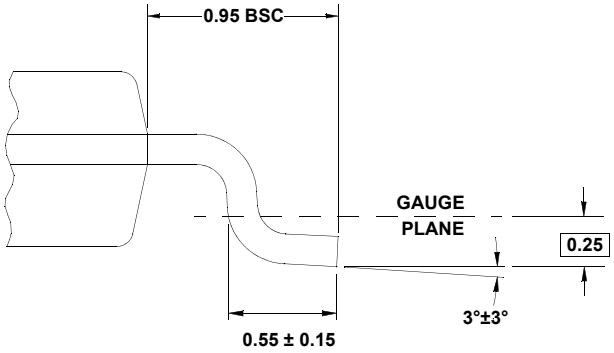
TOP VIEW



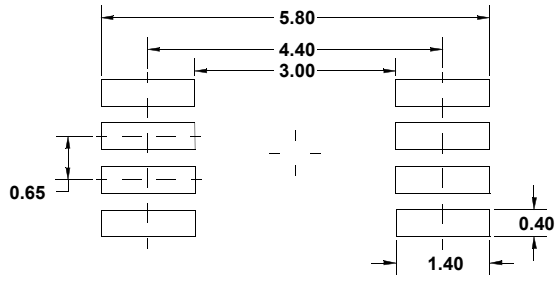
SIDE VIEW 2



SIDE VIEW 1



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

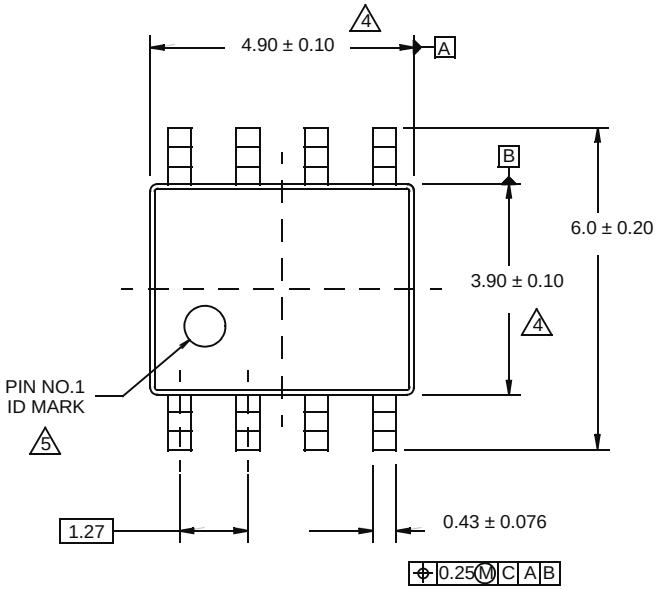
NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSE Y14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.25mm max per side are not included.
5. Dimensions “D” and “E1” are measured at Datum Plane “H”.
6. This replaces existing drawing # MDP0043 MSOP 8L.

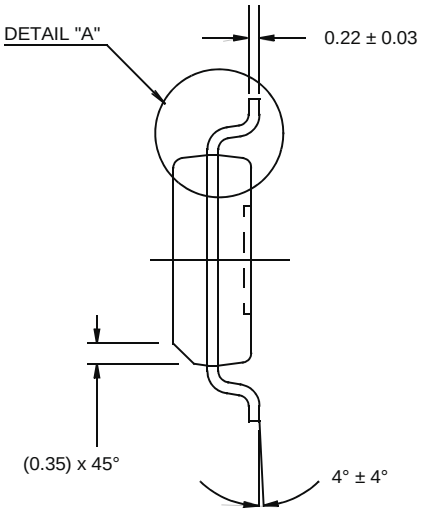
Package Outline Drawing

M8.15E

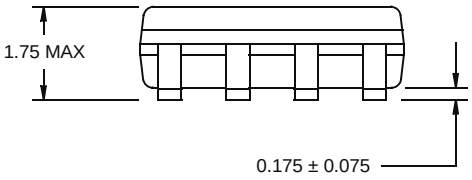
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 0, 08/09



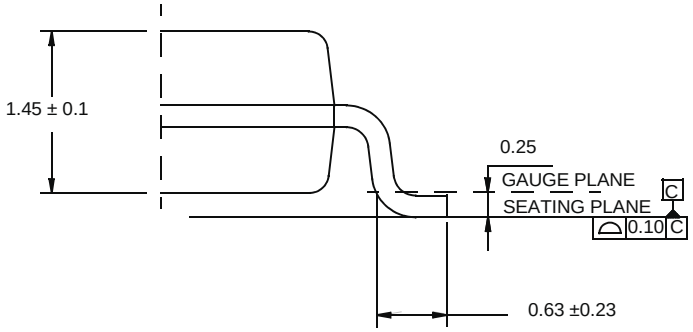
TOP VIEW



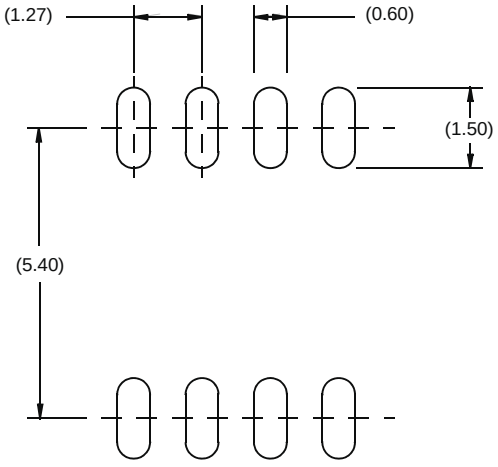
SIDE VIEW “B”



SIDE VIEW “A”



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.