

4-BIT PARALLEL-ACCESS SHIFT REGISTER WITH RESET

DESCRIPTION

The M74LS195AP is a semiconductor integrated circuit containing a 4-bit serial/parallel input-serial/parallel output shift register function with a direct reset input.

FEATURES

- Synchronous serial/parallel input-serial/parallel output
- Right shift function
- Left shift function available with external connection
- Mode control input provided
- Serial inputs J and \bar{K} provided
- Direct reset input provided
- Q_3 and \bar{Q}_3 outputs provided
- Wide operating temperature range ($T_a = -20 \sim +75^\circ\text{C}$)

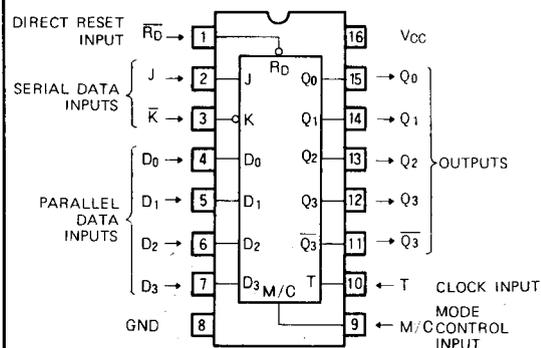
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device can be used as a serial input-serial/parallel output and parallel input-serial/parallel output shift register with the mode control input M/C signal. When M/C is kept in high, the serial data are applied to serial data inputs J and \bar{K} and the clock pulse is applied to clock input T, the serial data are shifted sequentially into outputs $Q_0 \sim \bar{Q}_3$ in synchronization with the clock pulse. The first stage flip-flop with J and \bar{K} functions as a J-K flip-flop. When serial data are applied from line 1, J and \bar{K} are mutually connected and used as serial input pins. When M/C is kept in low, the parallel data are applied to parallel data inputs $D_0 \sim D_3$ and a 1-bit clock pulse is applied to T, the $D_0 \sim D_3$ signals appears in $Q_0 \sim \bar{Q}_3$. When T changes from low to high, the shift or parallel reading operation is performed.

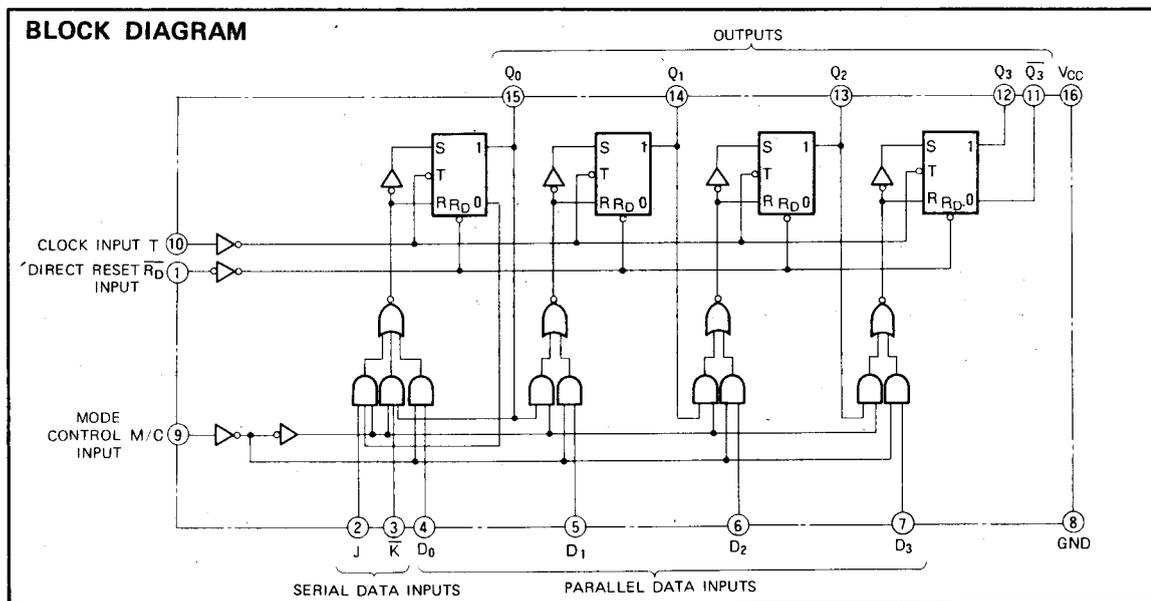
PIN CONFIGURATION (TOP VIEW)



Outline 16P4

The last stage flip-flop output has mutually complementary outputs Q_3 and \bar{Q}_3 . $Q_0 \sim Q_3$ are reset low and \bar{Q}_3 high by setting direct reset input \bar{R}_D low irrespective of all the other input signals.

BLOCK DIAGRAM



4-BIT PARALLEL-ACCESS SHIFT REGISTER WITH RESET

FUNCTION TABLE (Note 1)

| Operational mode | T | $\overline{R_D}$ | M/C | J | K | $D_0 \sim D_3$ | Q_0 | Q_1 | Q_2 | Q_3 | $\overline{Q_3}$ |
|------------------|---|------------------|-----|---|---|----------------|--------------------|---------|---------|---------|--------------------|
| Direct reset | X | L | X | X | X | X | L | L | L | L | H |
| Right shift | ↑ | H | H | H | H | X | H | Q_0^0 | Q_1^0 | Q_2^0 | $\overline{Q_2^0}$ |
| | ↑ | H | H | L | L | X | L | Q_0^0 | Q_1^0 | Q_2^0 | $\overline{Q_2^0}$ |
| | ↑ | H | H | H | L | X | $\overline{Q_0^0}$ | Q_0^0 | Q_1^0 | Q_2^0 | $\overline{Q_2^0}$ |
| | ↑ | H | H | L | H | X | Q_0^0 | Q_0^0 | Q_1^0 | Q_2^0 | $\overline{Q_2^0}$ |
| Parallel read | ↑ | H | L | X | X | $D_0 \sim D_3$ | D_0 | D_1 | D_2 | D_3 | $\overline{D_3}$ |

Note 1. ↑ : Transition from low to high (positive edge triggering)
 Q_0^0 : Level of Q before the indicated steady-state input conditions were established
 X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | Unit |
|-----------|--|-------------------|--------------------|------------------|
| V_{CC} | Supply voltage | | $-0.5 \sim +7$ | V |
| V_I | Input voltage | | $-0.5 \sim +15$ | V |
| V_O | Output voltage | High-level output | $-0.5 \sim V_{CC}$ | V |
| T_{opr} | Operating free-air ambient temperature range | | $-20 \sim +75$ | $^\circ\text{C}$ |
| T_{stg} | Storage temperature range | | $-65 \sim +150$ | $^\circ\text{C}$ |

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

| Symbol | Parameter | | Limits | | | Unit |
|----------|---------------------------|---------------------------|--------|-----|------|---------------|
| | | | Min | Typ | Max | |
| V_{CC} | Supply voltage | | 4.75 | 5 | 5.25 | V |
| I_{OH} | High-level output current | $V_{OH} \geq 2.7\text{V}$ | 0 | | -400 | μA |
| I_{OL} | Low-level output current | $V_{OL} \leq 0.4\text{V}$ | 0 | | 4 | mA |
| | | $V_{OL} \leq 0.5\text{V}$ | 0 | | 8 | mA |

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit | |
|----------|---------------------------------------|---|-----------------------|------|------|---------------|---|
| | | | Min | Typ* | Max | | |
| V_{IH} | High-level input voltage | | 2 | | | V | |
| V_{IL} | Low-level input voltage | | | | 0.8 | V | |
| V_{IC} | Input clamp voltage | $V_{CC} = 4.75\text{V}, I_{IC} = -18\text{mA}$ | | | -1.5 | V | |
| V_{OH} | High-level output voltage | $V_{CC} = 4.75\text{V}, V_I = 0.8\text{V}$ $V_I = 2\text{V}, I_{OH} = -400\mu\text{A}$ | 2.7 | 3.4 | | V | |
| V_{OL} | Low-level output voltage | $V_{CC} = 4.75\text{V}$ $V_I = 0.8\text{V}, V_I = 2\text{V}$ | $I_{OL} = 4\text{mA}$ | | 0.25 | 0.4 | V |
| | | | $I_{OL} = 8\text{mA}$ | | 0.35 | 0.5 | V |
| I_{IH} | High-level input current | $V_{CC} = 5.25\text{V}, V_I = 2.7\text{V}$ | | | 20 | μA | |
| | | $V_{CC} = 5.25\text{V}, V_I = 10\text{V}$ | | | 0.1 | mA | |
| I_{IL} | Low-level input current | $V_{CC} = 5.25\text{V}, V_I = 0.4\text{V}$ | | | -0.4 | mA | |
| I_{OS} | Short-circuit output current (Note 2) | $V_{CC} = 5.25\text{V}, V_O = 0\text{V}$ | -20 | | -100 | mA | |
| I_{CC} | Supply current | $V_{CC} = 5.25\text{V}$ (Note 3) | | 14 | 21 | mA | |

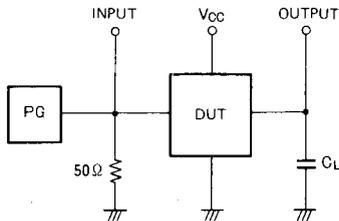
* : All typical values are at $V_{CC} = 5\text{V}, T_a = 25^\circ\text{C}$.
 Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.
 Note 3: I_{CC} is measured with M/C at 0V, J, K and $D_0 \sim D_3$ at 4.5V, with $\overline{R_D}$ kept at 4.5V after changing from 0V and after changing T from 0V to 4.5V.

4-BIT PARALLEL-ACCESS SHIFT REGISTER WITH RESET

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|------------------|---|---------------------------------|--------|-----|-----|------|
| | | | Min | Typ | Max | |
| t _{max} | Maximum clock frequency | C _L = 15 pF (Note 4) | 30 | 60 | | MHz |
| t _{PLH} | Low-to-high-level, high-to-low-level output propagation time, from input T to outputs Q ₀ ~ Q ₃ , \bar{Q}_3 | | | 12 | 22 | ns |
| t _{PHL} | High-to-low-level output propagation time, from input T to outputs Q ₀ ~ Q ₃ | | | 12 | 26 | ns |
| t _{PHL} | High-to-low-level output propagation time, from input \bar{R}_D to output Q ₀ ~ Q ₃ | | | 14 | 30 | ns |
| t _{PLH} | Low-to-high-level output propagation time, from input \bar{R}_D to output Q ₃ | | | 12 | 30 | ns |

Note 4: Measurement circuit

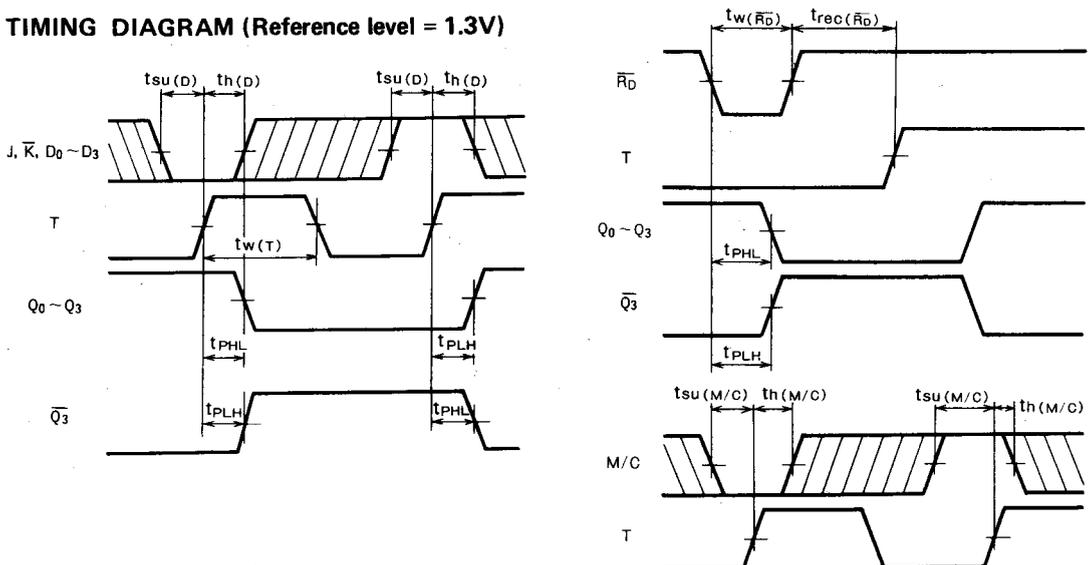


- (1) The pulse generator has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
V_p = 3V_{pp}, Z_o = 50Ω.
- (2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|----------------------------------|--------------------------------------|-----------------|--------|-----|-----|------|
| | | | Min | Typ | Max | |
| t _w (T) | Clock input T high pulse width | | 16 | 10 | | ns |
| t _w (\bar{R}_D) | Direct reset \bar{R}_D pulse width | | 12 | 6 | | ns |
| t _{SU} (D) | Setup time input data to T | | 15 | 3 | | ns |
| t _{SU} (M/C) | Setup time M/C to T | | 25 | 10 | | ns |
| t _H (D) | Hold time input data to T | | 3 | -1 | | ns |
| t _H (M/C) | M/C hold time to T | | 0 | -7 | | ns |
| t _{rec} (\bar{R}_D) | Direct reset recovery time to T | | 25 | 5 | | ns |

TIMING DIAGRAM (Reference level = 1.3V)

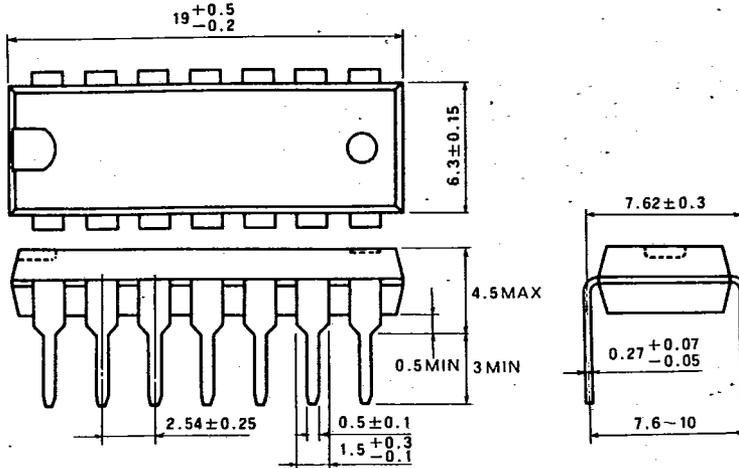


Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

T-90-20

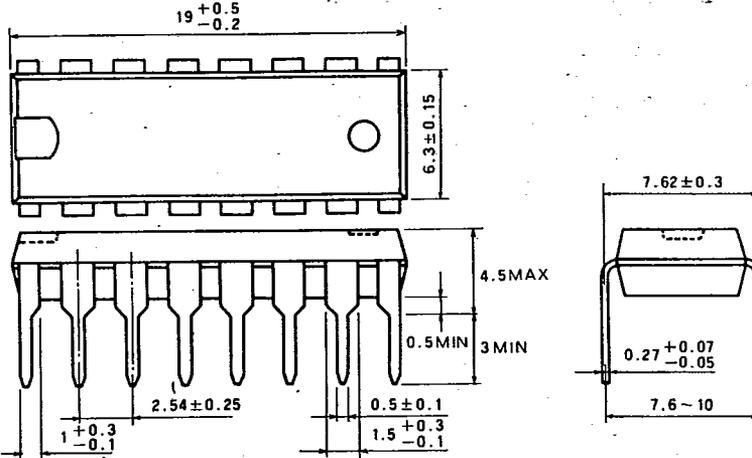
TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimension in mm

