

## 12V, P-Channel NexFET™ Power MOSFETs

Check for Samples: [CSD23381F4](#)

### FEATURES

- Ultra Low On Resistance
- Ultra Low  $Q_g$  and  $Q_{gd}$
- High Operating Drain Current
- Ultra Small Footprint (0402 Case Size)
  - 1.0 mm x 0.6 mm
- Ultra Low Profile
  - 0.35 mm Max Height
- Integrated ESD Protection Diode
  - Rated > 4kV HBM
  - Rated > 2kV CDM
- Pb Free Terminal Plating and Hallogen Free
- RoHS Compliant

### APPLICATIONS

- Optimized for Load Switch Applications
- Optimized for General Purpose Switching Applications
- Battery Applications
- Handheld and Mobile Applications

### DESCRIPTION

This 150mΩ, 12V P-Channel FemtoFET™ MOSFET has been designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing at least a 60% reduction in footprint size.

### PRODUCT SUMMARY

$V_{DS}$	Drain to Source Voltage	-12	V
$Q_g$	Gate Charge Total (-4.5V)	1140	pC
$Q_{gd}$	Gate Charge Gate to Drain	190	pC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = -1.8V$	480 mΩ
		$V_{GS} = -2.5V$	250 mΩ
		$V_{GS} = -4.5V$	150 mΩ
$V_{GS(th)}$	Threshold Voltage	-0.95	V

### ORDERING INFORMATION

Device	Qty	Media	Package	Ship
CSD23381F4	3,000	7-Inch Reel	Femto(0402) 1.0mm x 0.6mm Land Grid Array (LGA)	Tape and Reel

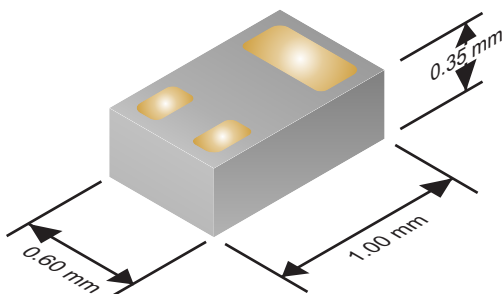
### ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain to Source Voltage	-12	V
$V_{GS}$	Gate to Source Voltage	-8	V
$I_D$	Continuous Drain Current <sup>(1)</sup>	-2.3	A
$I_{DM}$	Pulsed Drain Current <sup>(2)</sup>	-9	A
$P_D$	Power Dissipation <sup>(1)</sup>	500	mW
ESD Rating	Human Body Model (HBM)	4	kV
	Charged Device Model (CDM)	2	kV
$T_J$ , $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to 150	°C

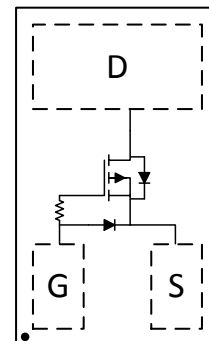
(1) Typical  $R_{\theta JA} = 85^\circ\text{C/W}$  on 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

(2) Pulse duration  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$

Typical Part Dimensions



Top View



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FemtoFET is a trademark of Texas Instruments.

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## ELECTRICAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV <sub>DSS</sub>	Drain to Source Voltage	V <sub>GS</sub> = 0V, I <sub>DS</sub> = -250μA	-12			V
I <sub>DSS</sub>	Drain to Source Leakage Current	V <sub>GS</sub> = 0V, V <sub>DS</sub> = -9.6V	-1			μA
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>DS</sub> = 0V, V <sub>GS</sub> = -8V	-100			nA
V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>DS</sub> = -250μA	-0.70	-0.95	-1.20	V
R <sub>DS(on)</sub>	Drain to Source On Resistance	V <sub>GS</sub> = -1.8V, I <sub>DS</sub> = -0.1A		480	970	mΩ
		V <sub>GS</sub> = -2.5V, I <sub>DS</sub> = -0.5A		250	300	mΩ
		V <sub>GS</sub> = -4.5V, I <sub>DS</sub> = -0.5A		150	175	mΩ
g <sub>fs</sub>	Transconductance	V <sub>DS</sub> = -6V, I <sub>DS</sub> = -0.5A		2.0		S
Dynamic Characteristics						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> = 0V, V <sub>DS</sub> = -6V, f = 1MHz		236		pF
C <sub>oss</sub>	Output Capacitance			98		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			6.9		pF
R <sub>G</sub>	Series Gate Resistance			20		Ω
Q <sub>g</sub>	Gate Charge Total (4.5V)	V <sub>DS</sub> = -6V, I <sub>DS</sub> = -0.5A		1140		pC
Q <sub>gd</sub>	Gate Charge Gate to Drain			190		pC
Q <sub>gs</sub>	Gate Charge Gate to Source			300		pC
Q <sub>g(th)</sub>	Gate Charge at V <sub>th</sub>			145		pC
Q <sub>oss</sub>	Output Charge	V <sub>DS</sub> = -6V, V <sub>GS</sub> = 0V		1290		pC
t <sub>d(on)</sub>	Turn On Delay Time	V <sub>DS</sub> = 0V, V <sub>GS</sub> = -4.5V, I <sub>DS</sub> = -0.5A, R <sub>G</sub> = 2Ω		4.5		ns
t <sub>r</sub>	Rise Time			3.9		ns
t <sub>d(off)</sub>	Turn Off Delay Time			18.0		ns
t <sub>f</sub>	Fall Time			7.0		ns
Diode Characteristics						
V <sub>SD</sub>	Diode Forward Voltage	I <sub>SD</sub> = -0.5A, V <sub>GS</sub> = 0V		-0.75		V
Q <sub>rr</sub>	Reverse Recovery Charge	V <sub>DS</sub> = -10V, I <sub>F</sub> = -0.5A, di/dt = 100A/μs		1260		pC
t <sub>rr</sub>	Reverse Recovery Time			7.9		ns

## THERMAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER		Typical Values	UNIT
$R_{\theta JA}$	Thermal Resistance Junction to Ambient <sup>(1)</sup>	85	$^\circ\text{C/W}$
	Thermal Resistance Junction to Ambient <sup>(2)</sup>	245	$^\circ\text{C/W}$

(1) Device mounted on FR4 material with 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu.

(2) Device mounted on FR4 material with minimum Cu mounting area.

## TYPICAL MOSFET CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

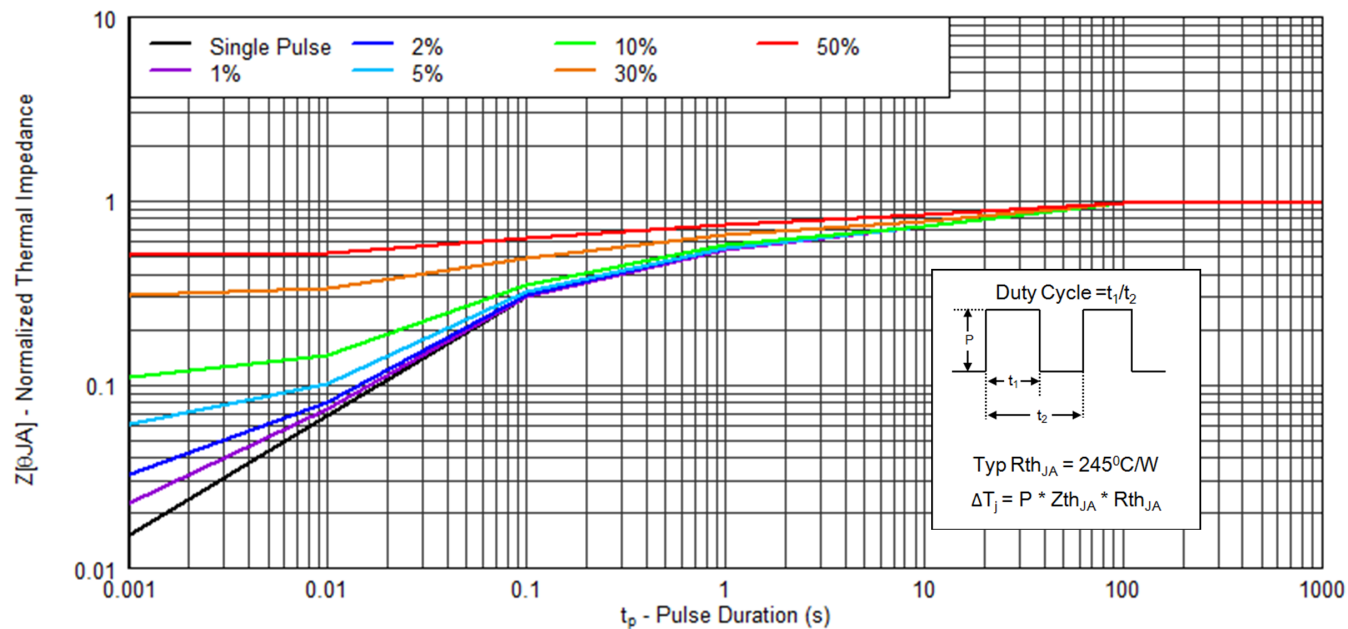


Figure 1. Transient Thermal Impedance

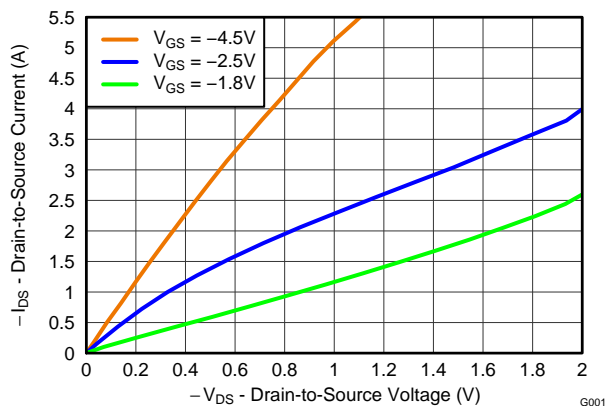


Figure 2. Saturation Characteristics

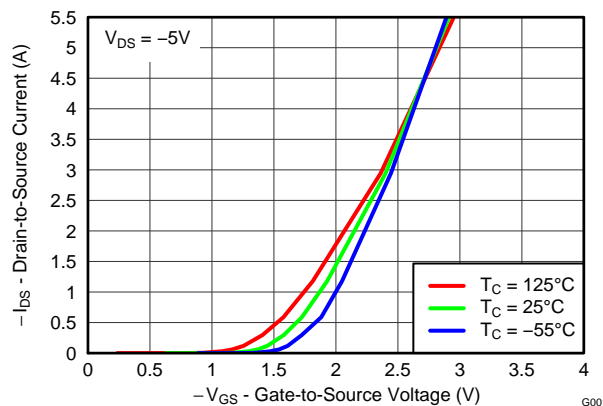


Figure 3. Transfer Characteristics

## TYPICAL MOSFET CHARACTERISTICS (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

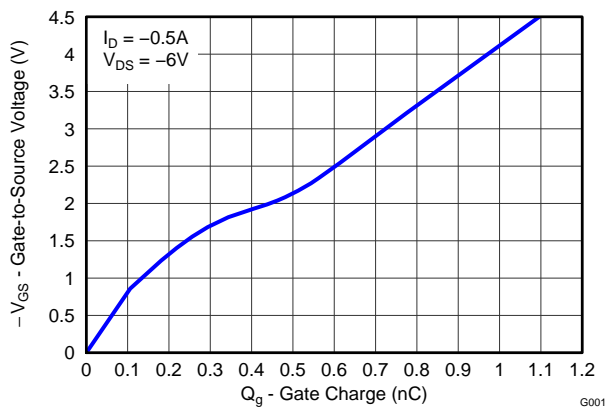


Figure 4. Gate Charge

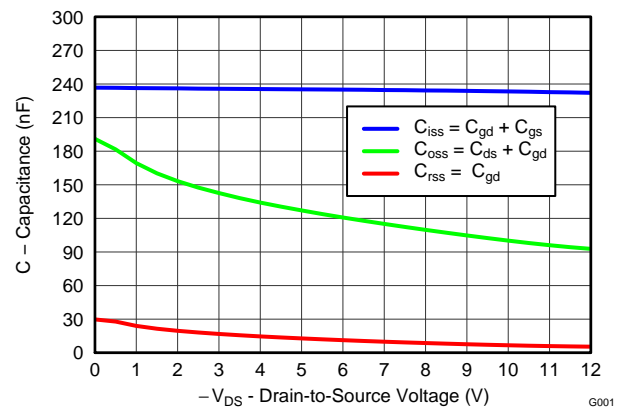


Figure 5. Capacitance

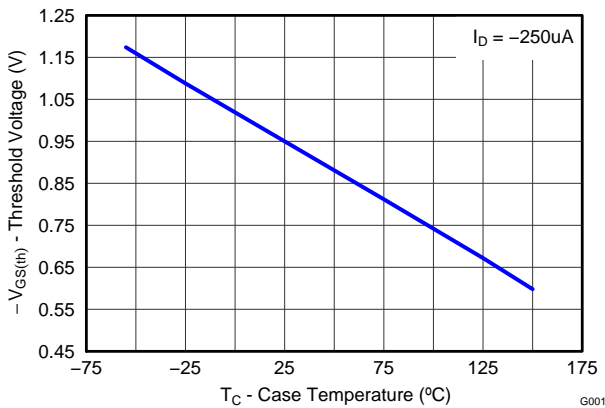


Figure 6. Threshold Voltage vs. Temperature

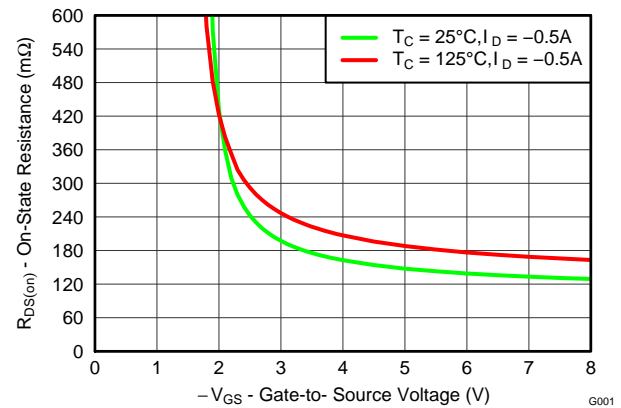


Figure 7. On-State Resistance vs. Gate-to-Source Voltage

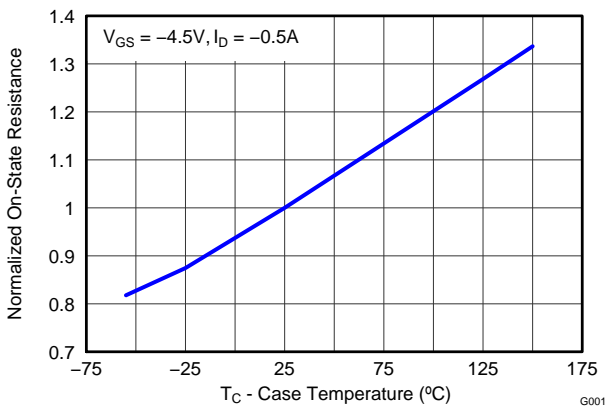


Figure 8. Normalized On-State Resistance vs. Temperature

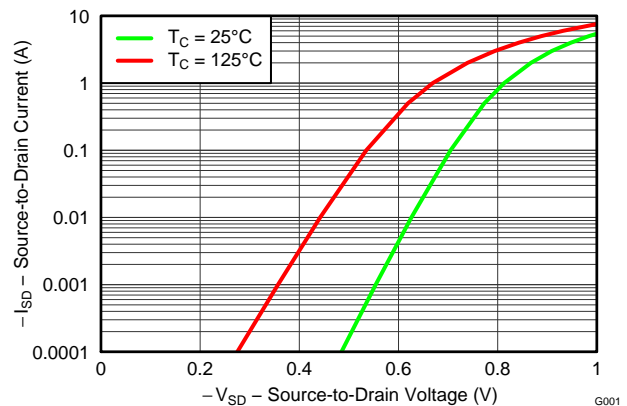
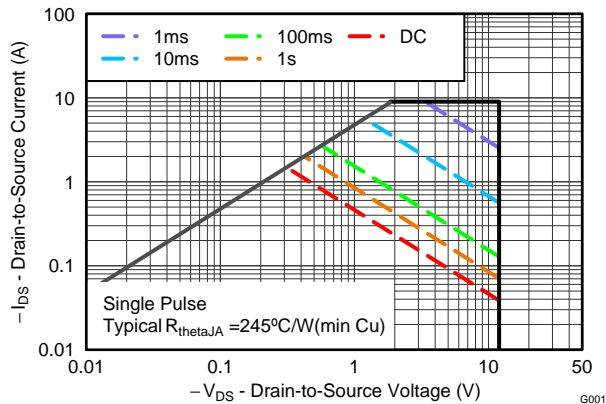


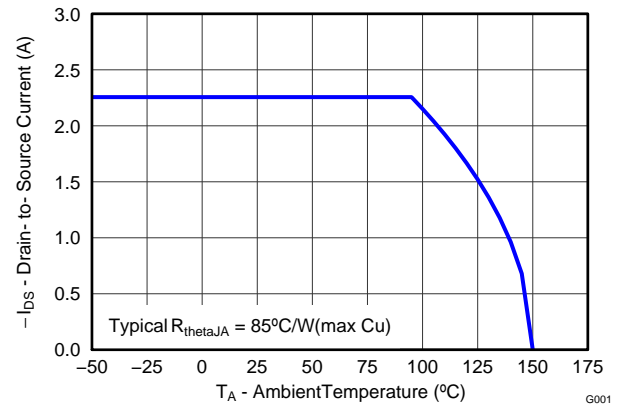
Figure 9. Typical Diode Forward Voltage

## TYPICAL MOSFET CHARACTERISTICS (continued)

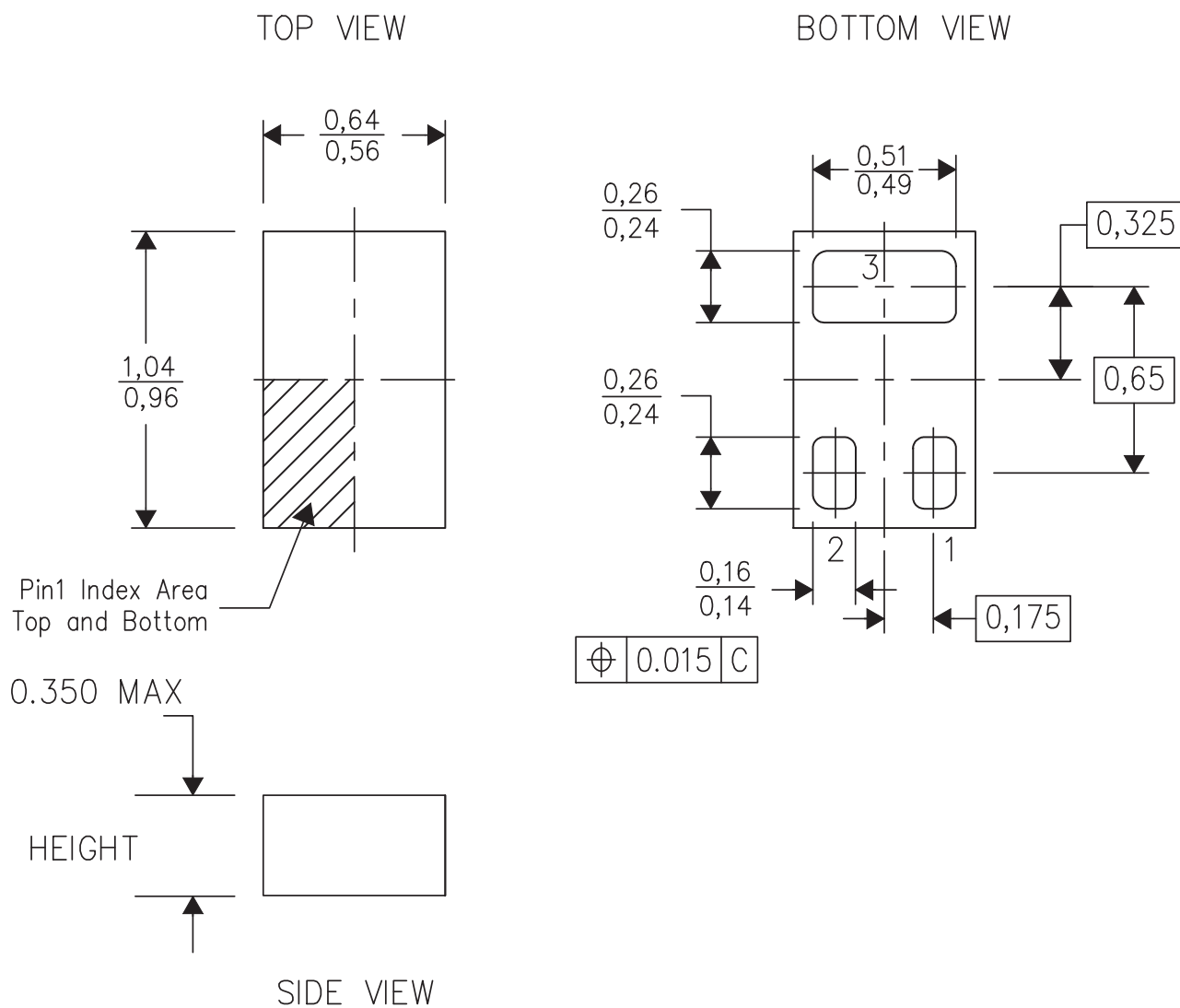
( $T_A = 25^\circ\text{C}$  unless otherwise stated)



**Figure 10. Maximum Safe Operating Area**



**Figure 11. Maximum Drain Current vs. Temperature**

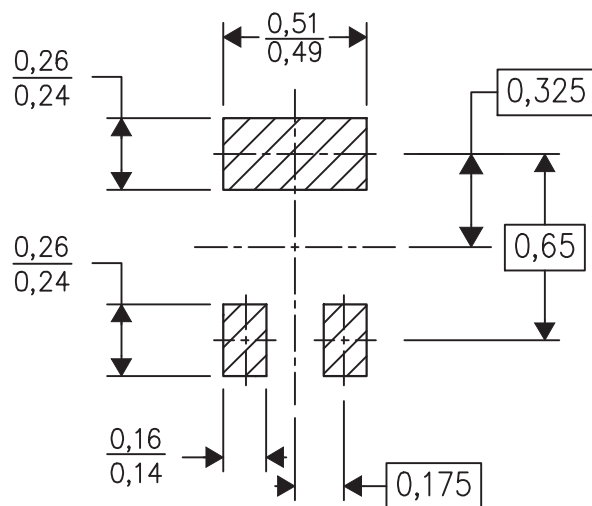
**MECHANICAL DATA****0402 Mechanical Dimensions**

- (1) All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994)
- (2) This drawing is subject to change without notice
- (3) This package is a PB-Free solder land design

**Table 1. Pin Configuration**

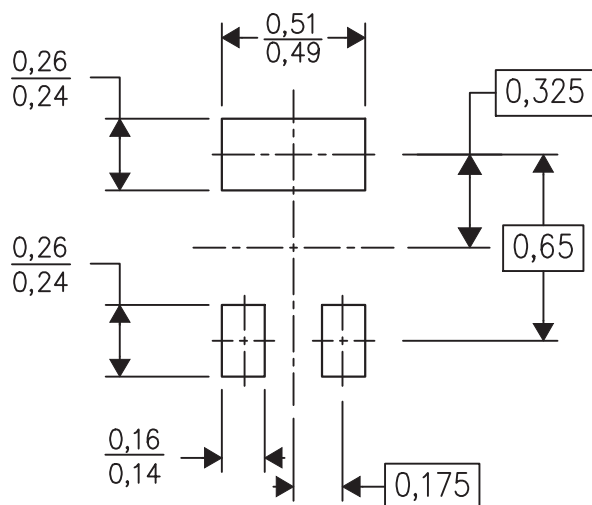
Position	Designation
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

## Recommended Minimum PCB Layout



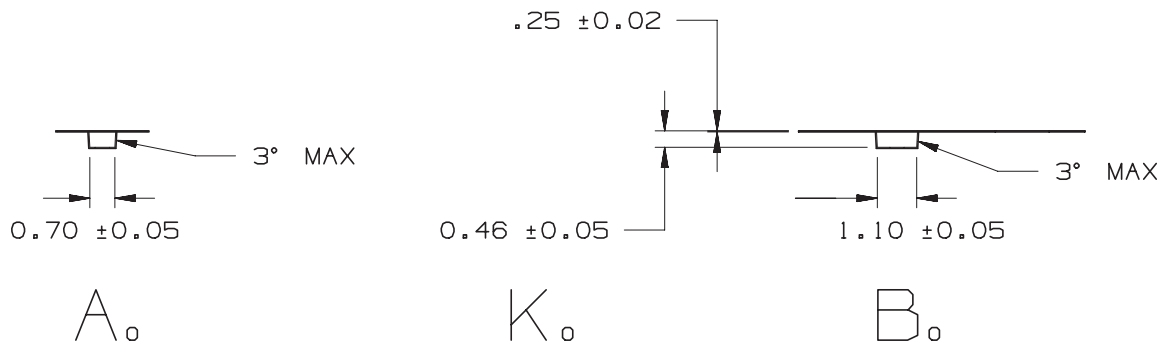
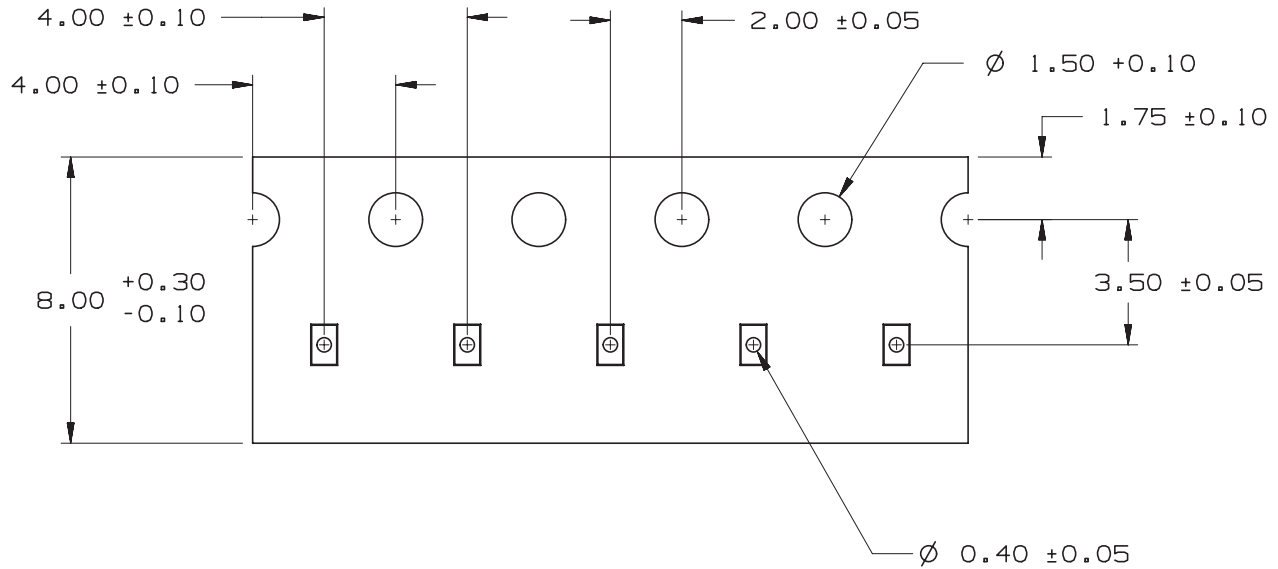
(1) All dimensions are in millimeters.

## Recommended Stencil Pattern



(1) All dimensions are in millimeters.

## CSD23381F4 Embossed Carrier Tape Dimensions



- (1) Pin 1 will be oriented in the top right quadrant of the tape enclosure (Quadrant 2), closest to the carrier tape sprocket holes.



## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD23381F4	ACTIVE	PICOSTAR	YJC	3	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-250C-UNLIM	-40 to 85	DS	<a href="#">Samples</a>
CSD23381F4R	PREVIEW	PICOSTAR	YJC	3	18000	TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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