

74LV245

Octal bus transceiver; 3-state

Rev. 03 — 15 April 2009

Product data sheet

1. General description

The 74LV245 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC245 and 74HCT245.

The 74LV245 is an octal transceiver with non-inverting 3-state bus compatible outputs in both send and receive directions. A send/receive (DIR) input controls direction, and an output enable ($\overline{OE}$) input makes easy cascading possible. Pin $\overline{OE}$ controls the outputs so that the buses are effectively isolated.

2. Features

- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between $V_{CC} = 2.7$ V and $V_{CC} = 3.6$ V
- Typical output ground bounce < 0.8 V at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C
- Typical HIGH-level output voltage (V_{OH}) undershoot: > 2 V at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to $+85$ °C and from -40 °C to $+125$ °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV245N	-40 °C to $+125$ °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74LV245D	-40 °C to $+125$ °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LV245DB	-40 °C to $+125$ °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74LV245PW	-40 °C to $+125$ °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4. Functional diagram

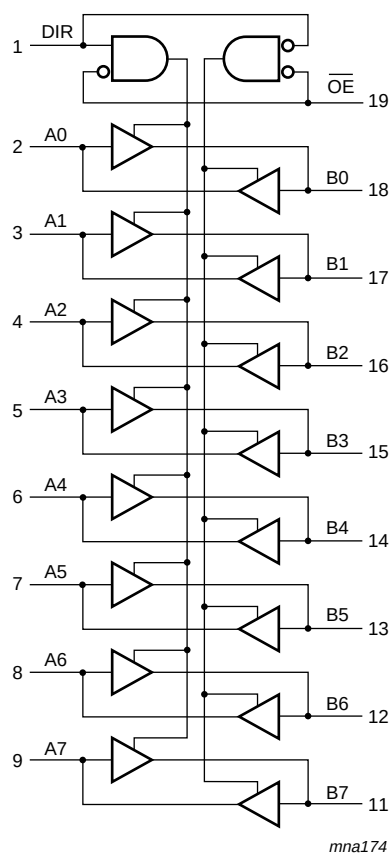


Fig 1. Logic symbol

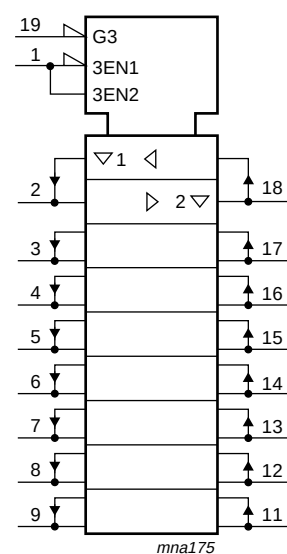
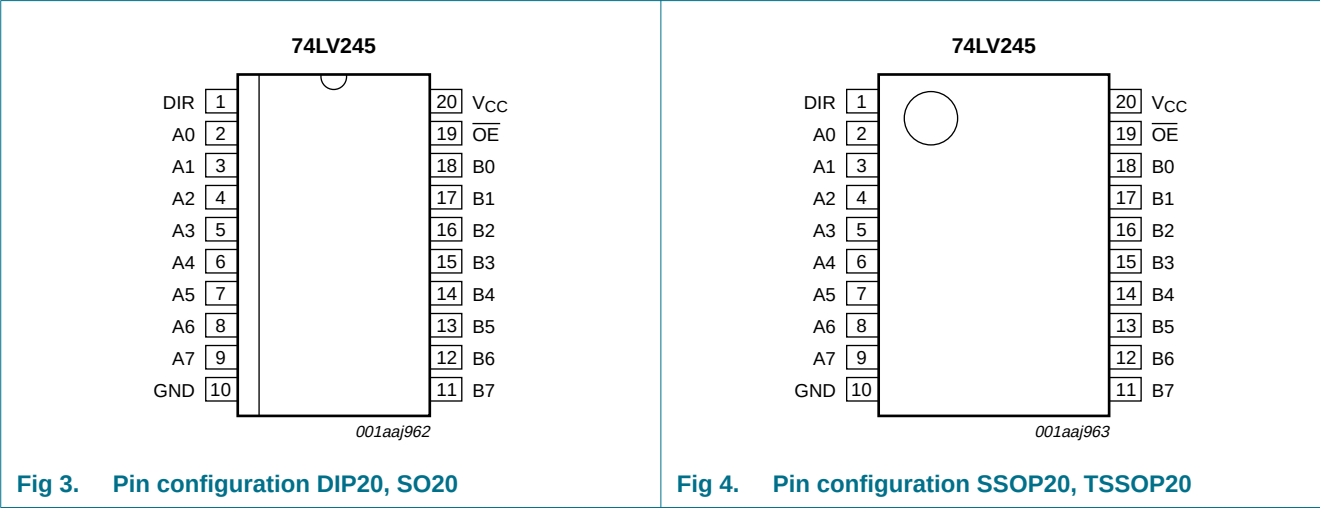


Fig 2. IEC logic symbol

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
DIR	1	direction control
A0 to A7	2, 3, 4, 5, 6, 7, 8, 9	data input/output
GND	10	ground (0 V)
B0 to B7	18, 17, 16, 15, 14, 13, 12, 11	data input/output
$\overline{\text{OE}}$	19	output enable input (active LOW)
V _{CC}	20	supply voltage

6. Functional description

Table 3. Function selection^[1]

Input		Output/input	
OE	DIR	A _n	B _n
L	L	A = B	input
L	H	input	B = A
H	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	[1] -	±20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	[1] -	±50	mA
I_O	output current	$V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$	-	±35	mA
I_{CC}	supply current		-	70	mA
I_{GND}	ground current		-70	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$	[2]		
		DIP20	-	750	mW
		SO20, SSOP20, TSSOP20	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For DIP20 packages: above 70 °C the value of P_{tot} derates linearly with 12 mW/K.

For SO20 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.

For (T)SSOP20 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage[1]		1.0	3.3	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.0\text{ V}$ to 2.0 V	-	-	500	ns/V
		$V_{CC} = 2.0\text{ V}$ to 2.7 V	-	-	200	ns/V
		$V_{CC} = 2.7\text{ V}$ to 3.6 V	-	-	100	ns/V
		$V_{CC} = 3.6\text{ V}$ to 5.5 V	-	-	50	ns/V

[1] The static characteristics are guaranteed from $V_{CC} = 1.2\text{ V}$ to $V_{CC} = 5.5\text{ V}$, but LV devices are guaranteed to function down to $V_{CC} = 1.0\text{ V}$ (with input levels GND or V_{CC}).

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	−40 °C to +85 °C			−40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	0.9	-	-	0.9	-	V
		V _{CC} = 2.0 V	1.4	-	-	1.4	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7V _{CC}	-	-	0.7V _{CC}	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.3	-	0.3	V
		V _{CC} = 2.0 V	-	-	0.6	-	0.6	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3V _{CC}	-	0.3V _{CC}	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = −100 μA; V _{CC} = 1.2 V	-	1.2	-	-	-	V
		I _O = −100 μA; V _{CC} = 2.0 V	1.8	2.0	-	1.8	-	V
		I _O = −100 μA; V _{CC} = 2.7 V	2.5	2.7	-	2.5	-	V
		I _O = −100 μA; V _{CC} = 3.0 V	2.8	3.0	-	2.8	-	V
		I _O = −100 μA; V _{CC} = 4.5 V	4.3	4.5	-	4.3	-	V
		I _O = −8 mA; V _{CC} = 3.0 V	2.4	2.82	-	2.2	-	V
		I _O = −16 mA; V _{CC} = 4.5 V	3.6	4.2	-	3.5	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 100 μA; V _{CC} = 1.2 V	-	0	-	-	-	V
		I _O = 100 μA; V _{CC} = 2.0 V	-	0	0.2	-	0.2	V
		I _O = 100 μA; V _{CC} = 2.7 V	-	0	0.2	-	0.2	V
		I _O = 100 μA; V _{CC} = 3.0 V	-	0	0.2	-	0.2	V
		I _O = 100 μA; V _{CC} = 4.5 V	-	0	0.2	-	0.2	V
		I _O = 8 mA; V _{CC} = 3.0 V	-	0.25	0.40	-	0.50	V
		I _O = 16 mA; V _{CC} = 4.5 V	-	0.35	0.55	-	0.65	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	1.0	-	1.0	μA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 5.5 V	-	-	5	-	10	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	20	-	160	μA
ΔI _{CC}	additional supply current	per input; V _I = V _{CC} − 0.6 V; V _{CC} = 2.7 V to 3.6 V	-	-	500	-	850	μA
C _I	input capacitance		-	3.5	-	-	-	pF
C _{I/O}	input/output capacitance		-	10	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	An, Bn to Bn, An; see Figure 5 ^[2]						
		V _{CC} = 1.2 V	-	45	28	-	-	ns
		V _{CC} = 2.0 V	-	15	28	-	34	ns
		V _{CC} = 2.7 V	-	11	19	-	24	ns
		V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF ^[3]	-	7	-	-	-	ns
		V _{CC} = 3.0 V to 3.6 V ^[3]	-	9	16	-	20	ns
		V _{CC} = 4.5 V to 5.5 V ^[3]	-	8	11	-	14	ns
t _{en}	enable time	$\overline{OE}$ to An, Bn; see Figure 6 ^[2]						
		V _{CC} = 1.2 V	-	55	-	-	-	ns
		V _{CC} = 2.0 V	-	19	31	-	39	ns
		V _{CC} = 2.7 V	-	14	23	-	29	ns
		V _{CC} = 3.0 V to 3.6 V ^[3]	-	10	18	-	23	ns
		V _{CC} = 4.5 V to 5.5 V ^[3]	-	8.5	14	-	18	ns
t _{dis}	disable time	$\overline{OE}$ to An, Bn; see Figure 6 ^[2]						
		V _{CC} = 1.2 V	-	65	-	-	-	ns
		V _{CC} = 2.0 V	-	24	32	-	39	ns
		V _{CC} = 2.7 V	-	18	24	-	29	ns
		V _{CC} = 3.0 V to 3.6 V ^[3]	-	14	20	-	24	ns
		V _{CC} = 4.5 V to 5.5 V ^[3]	-	11.5	16	-	19	ns
C _{PD}	power dissipation capacitance	C _L = 50 pF; f _i = 1 MHz; V _I = GND to V _{CC} ; V _{CC} = 3.3 V ^[4]	-	40	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

t_{en} is the same as t_{PZL} and t_{PZH}.

t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz, f_o = output frequency in MHz

C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11. Waveforms

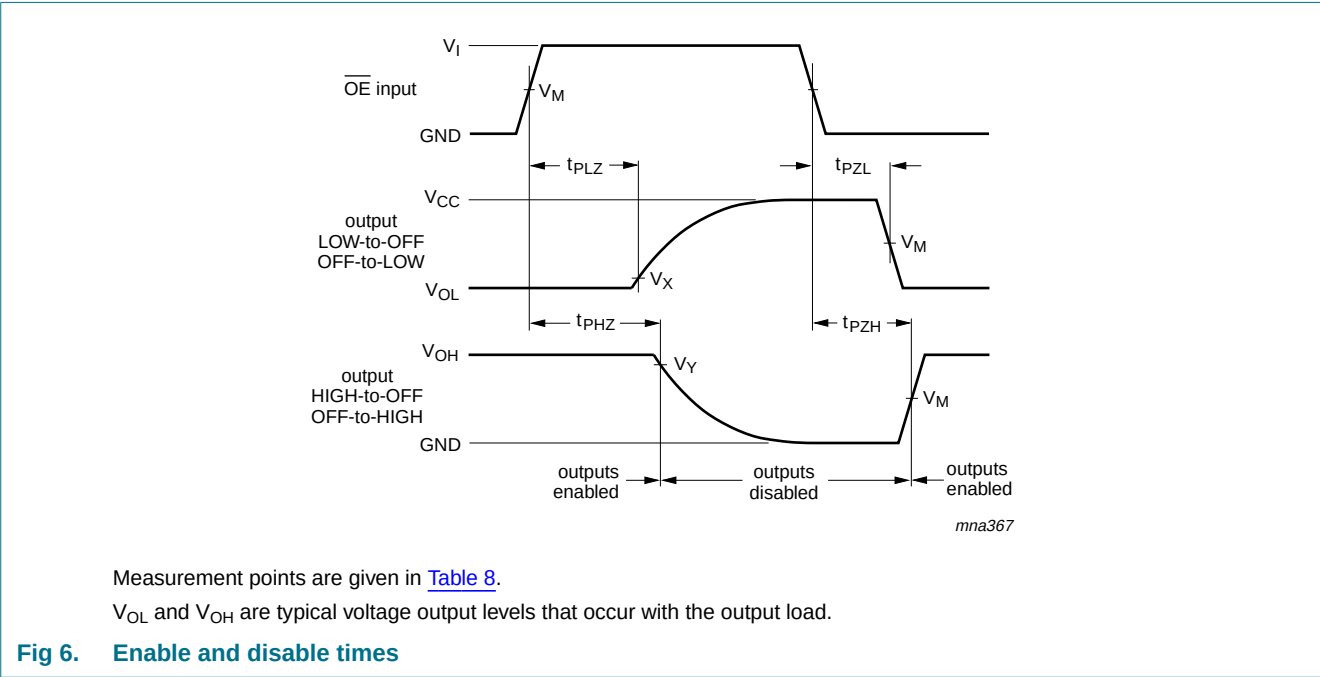
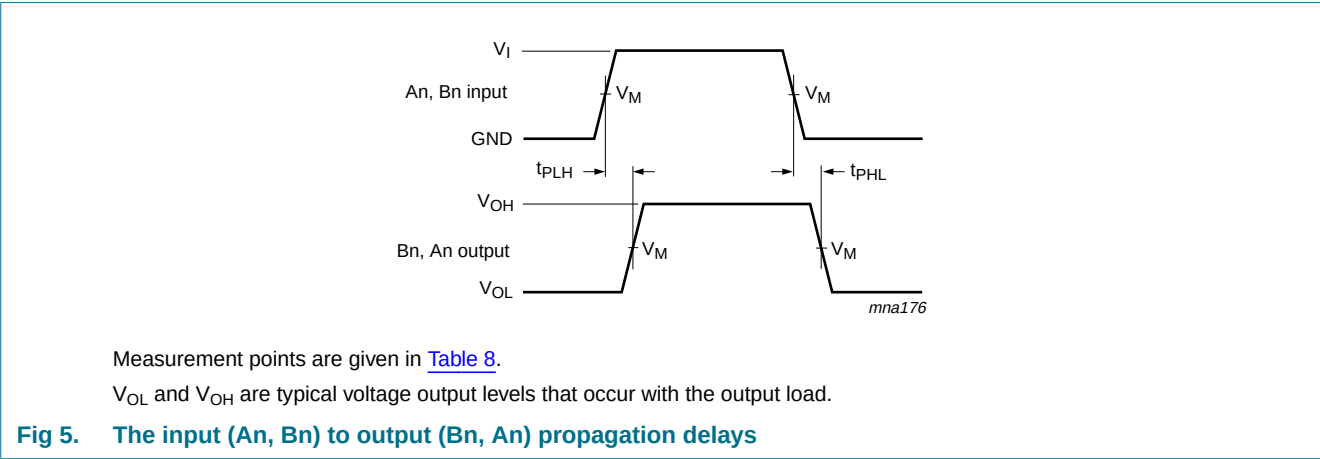
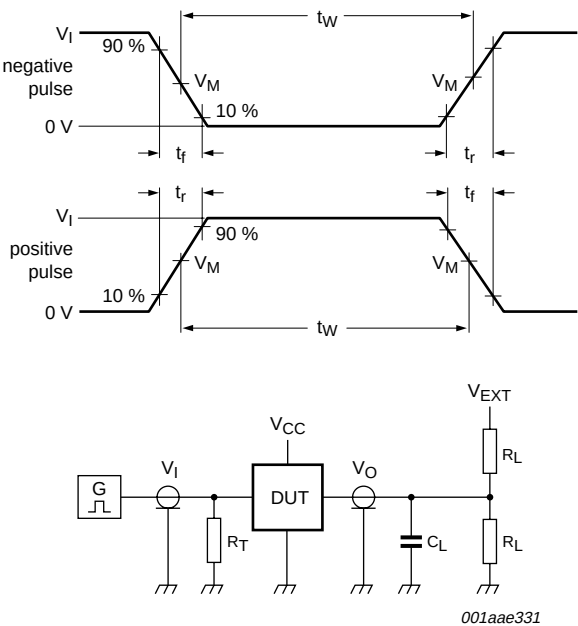


Table 8. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
< 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$
2.7 V to 3.6 V	1.5 V	1.5 V	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$
$\geq 4.5\text{ V}$	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$



Test data is given in [Table 9](#).
Definitions for test circuit:
 R_L = Load resistance.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.
 V_{EXT} = External voltage for measuring switching times.

Fig 7. Load circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
< 2.7 V	V_{CC}	≤ 2.5 ns	50 pF	1 k Ω	open	GND	$2V_{CC}$
2.7 V to 3.6 V	2.7 V	≤ 2.5 ns	15 pF, 50 pF	1 k Ω	open	GND	$2V_{CC}$
≥ 4.5 V	V_{CC}	≤ 2.5 ns	50 pF	1 k Ω	open	GND	$2V_{CC}$

12. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1

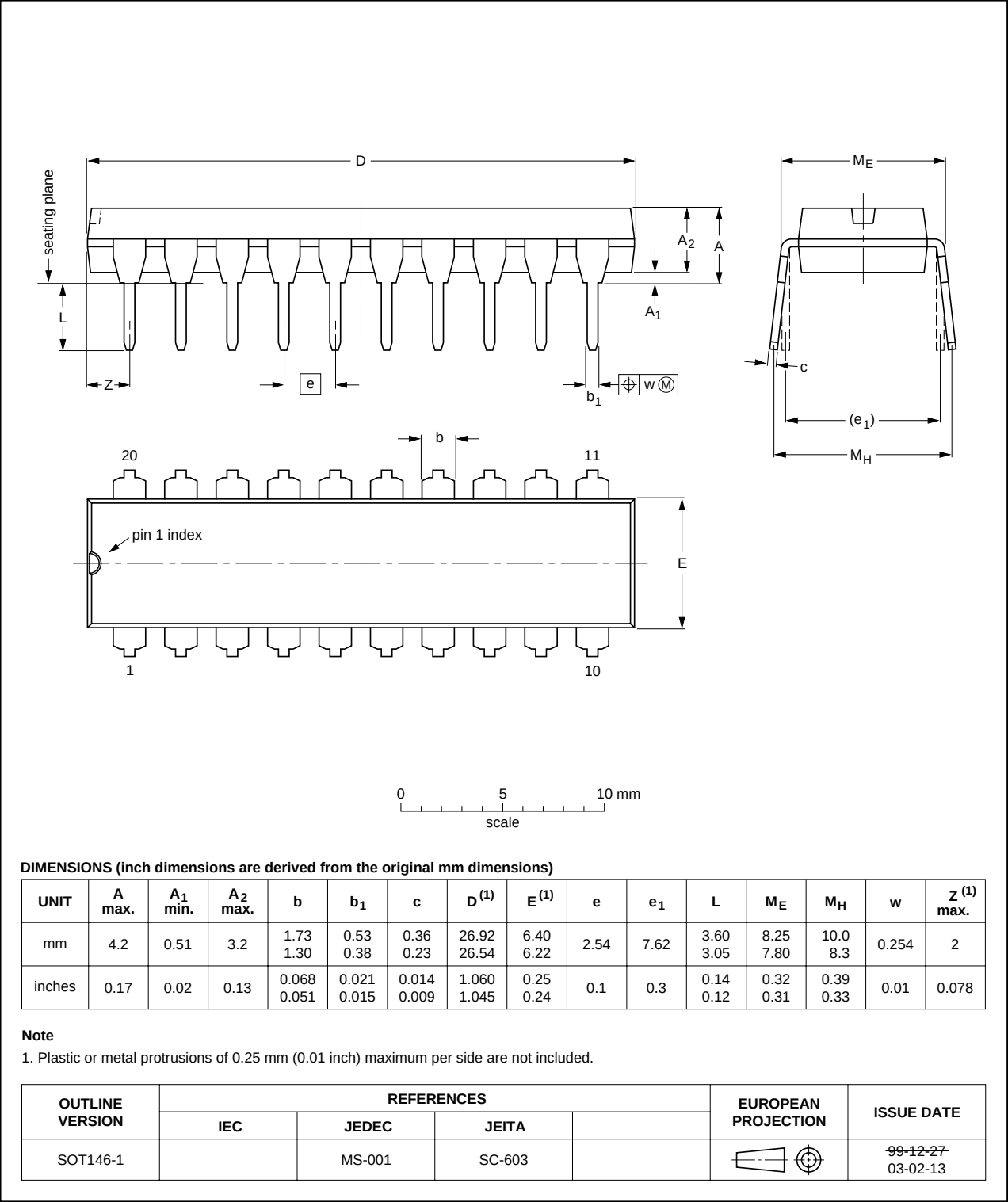


Fig 8. Package outline SOT146-1 (DIP20)

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

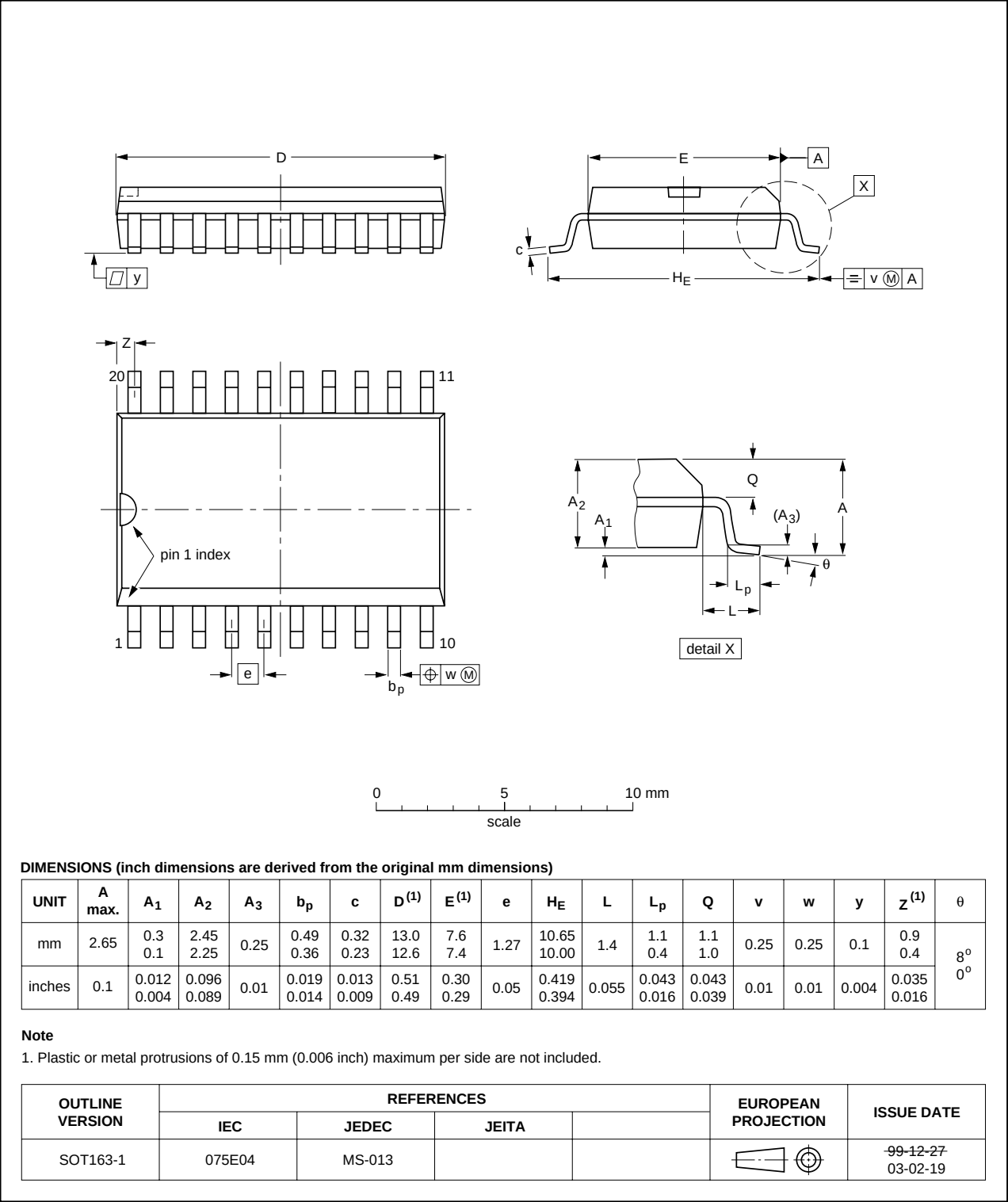


Fig 9. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

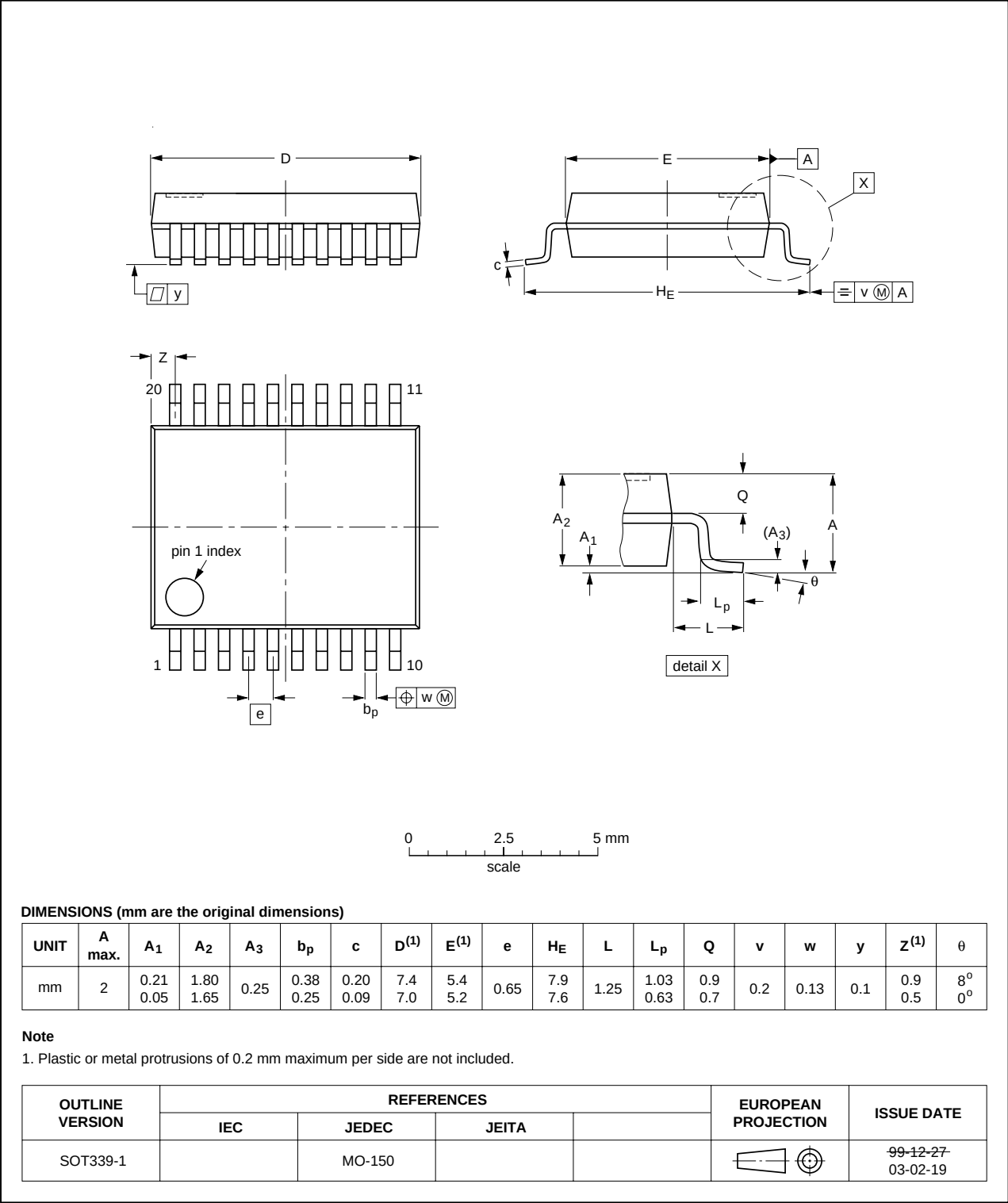


Fig 10. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

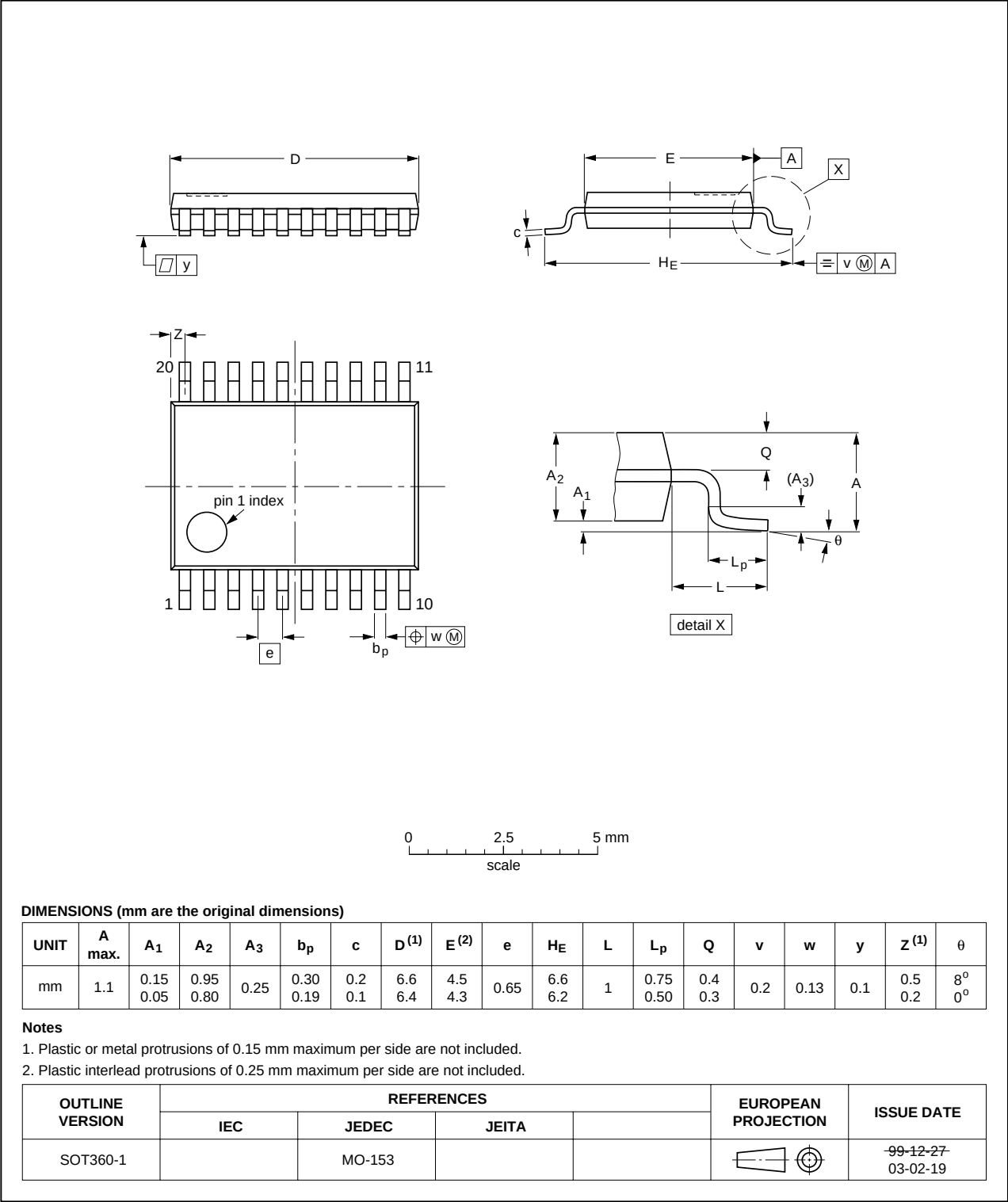


Fig 11. Package outline SOT360-1 (TSSOP20)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV245_3	20090415	Product data sheet	-	74LV245_2
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name when appropriate.			
74LV245_2	19980420	Product specification	-	74LV245_1
74LV245_1	19970303	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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