Hot Swap Controller

Features

- 10 to 90V operation, positive or negative supply
- UV/OV lock out & power-on-reset
- Circuit breaker
- 100ms startup timer
- Automatic retry or latched operation
- Low Power, 400µA sleep mode
- Active low power good
- 8-Lead SOIC package

Applications

- 48V central office switching
- 24V cellular and fixed wireless systems
- 24V PBX systems
- Line cards
- 48V powered ethernet for VoIP
- Distributed power systems
- Power supply control
- 48V storage networks
- Electronic circuit breaker

General Description

The Supertex HV311 Hot Swap Controller provides inrush current limiting and other power supply support functions for hot swap equipment. Current limiting is provided by control of an external MOSFET which is placed in the return line of the power supply connection. Placement in the return allows use of an N-channel MOSFET without the need for high side driving.

An internal clamp at the GATE pin activates when full bias for the HV311 is not available, thus keeping the MOSFET in the off-state during the initial insertion phase. As soon as adequate bias is available for the main control circuits, the UV (undervoltage) and OV (overvoltage) pins check for normal operating voltage on the power supply input.

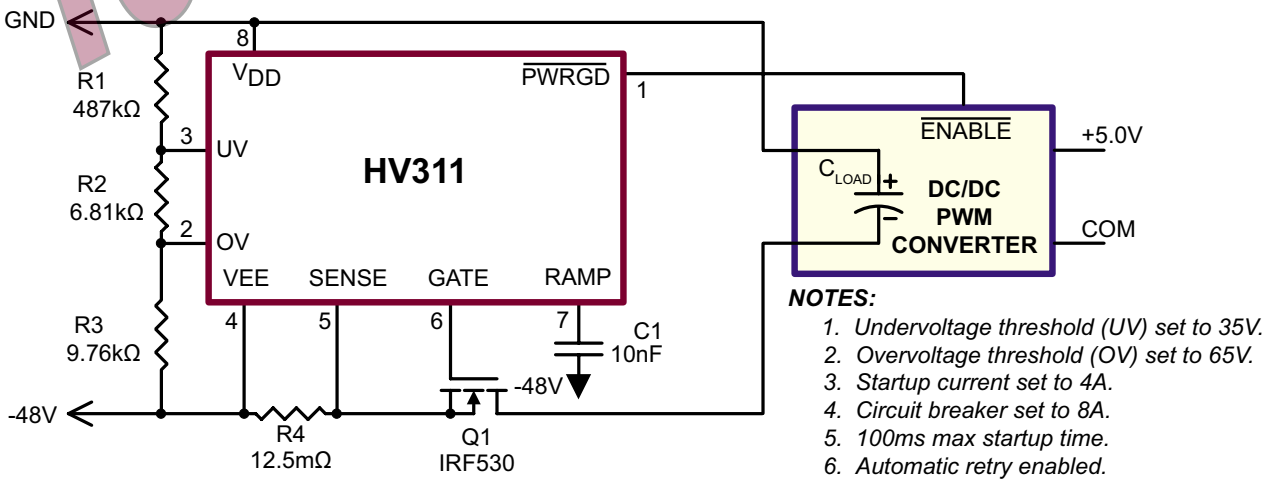
Once normal operating voltage is present, the GATE voltage for the external MOSFET ramps up at a constant rate. The rate is controlled by the value of an external capacitor placed at the RAMP pin. At some point the external MOSFET channel is enhanced, allowing power supply current to flow, thereby energizing downstream power supply capacitors.

During the GATE ramp up the power supply current is monitored with the aid of an external sense resistor which forces reduction in the ramp rate when the power supply current reaches a set limit. The limit is set by the value of the external sense resistor and the threshold of the current sense amplifier (50mV).

Once inrush current subsides, the GATE voltage resumes its rise to the output voltage of an internal regulator V_{REG}, with an output voltage ranging from 8.5 to 12V. When GATE is within 1.2V of V_{REG}, GATE is pulled high to V_{REG} with an internal switch, the open-drain $\overline{PWRGD}$ pin pulls low, and the HV311 enters a low power mode.

The HV311 includes a start-up timer and a circuit breaker function to protect the MOSFET from excessive power dissipation. The start-up timer trips when the start-up phase exceeds 100ms. The circuit breaker trips at double the current limit threshold (100mV). Upon tripping of either the start-up timer or the circuit breaker the MOSFET is turned off, and the $\overline{PWRGD}$ pin becomes high impedance. Thereafter, a programmable automatic retry timer allows the MOSFET to cool down before resetting and restarting. The automatic retry can be disabled by adding an external resistor at the RAMP pin (about 2.5MΩ, see applications section).

Typical Application Circuit



NOTES:

1. *Undervoltage threshold (UV) set to 35V.*
2. *Overvoltage threshold (OV) set to 65V.*
3. *Startup current set to 4A.*
4. *Circuit breaker set to 8A.*
5. *100ms max startup time.*
6. *Automatic retry enabled.*

Ordering Information

Device	Package Options
	8-Lead SOIC (Narrow Body) *4.90x3.90mm body 1.75mm height (max) 1.27mm pitch*
HV311	HV311LG-G

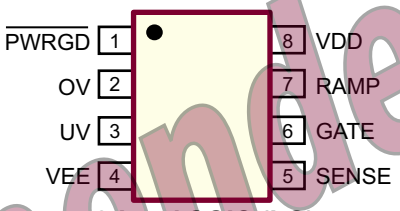
-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

Parameter	Value
V_{DD} (referenced to V_{EE})	-0.3V to +100V
$V_{\overline{PWRGD}}$ (referenced to V_{EE})	-0.3V to +100V
V_{UV} and V_{OV} (referenced to V_{EE})	-0.3V to +12V
Operating ambient temperature, T_J	-40°C to +85°C
Operating junction temperature, T_J	-40°C to +125°C
Storage temperature range, T_S	-65°C to +150°C

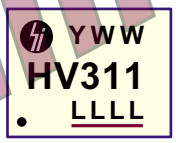
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



8-Lead SOIC (LG)

Product Marking



Y = Last Digit of Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

8-Lead SOIC (LG)

Electrical Characteristics *(-40°C to +85°C unless otherwise specified, all voltages are referenced to V_{EE})*

Sym	Parameter	Min	Typ	Max	Units	Conditions
Supply						
V_{DD}	Supply voltage	10	-	90	V	---
I_{DD}	Supply current	-	600	700	µA	V_{DD} = 48V, mode = limiting
	Standby mode supply current	-	400	450	µA	V_{DD} = 48V, mode = standby
OV and UV Comparators						
V_{RTH}	Rising threshold	-	1.26	-	V	Low to high transition
V_{FTH}	Falling threshold	-	1.16	-	V	High to low transition
V_{HYS}	Hysteresis	-	100	-	mV	---
I	Input current[1]	-	-	1.0	nA	V_{UV} = 1.9V
Current Limit						
V_{CL}	Current limit threshold voltage	40	50	60	mV	V_{UV} = 1.9V, V_{OV} = 0.5V
V_{CB}	Circuit breaker threshold voltage	80	100	120	mV	V_{UV} = 1.9V, V_{OV} = 0.5V

Notes:

1. *Guaranteed by design.*

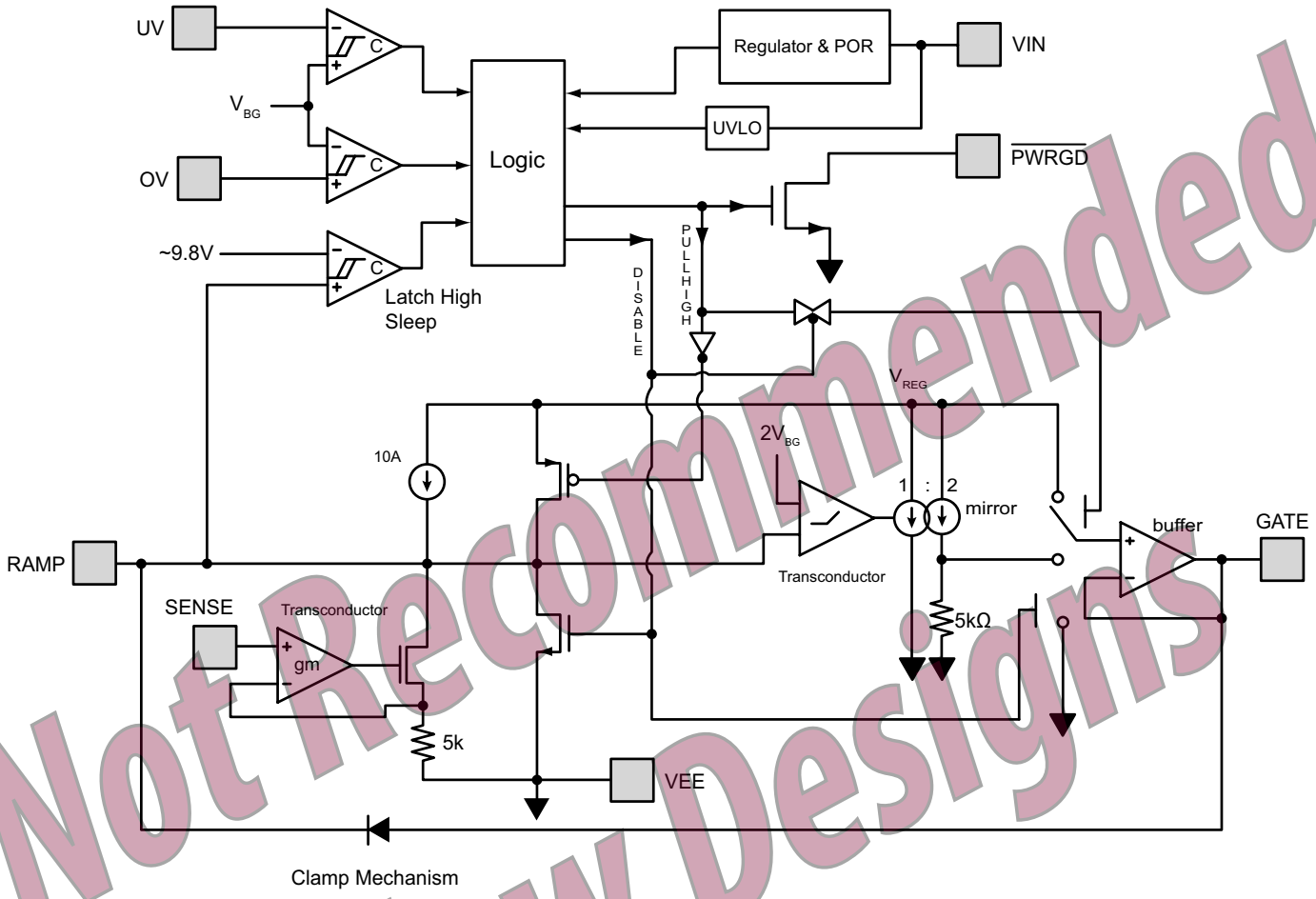
Electrical Characteristics *(-40°C to +85°C unless otherwise specified, all voltages are referenced to V_{EE})*

Sym	Parameter	Min	Typ	Max	Units	Conditions
Gate Drive Output						
V_{GATE}	Maximum GATE drive voltage	8.5	10	12	V	V_{UV} = 1.9V, V_{OV} =0.5V
I_{GATEUP}	GATE drive pull-up current	500	-	-	µA	V_{UV} = 1.9V, V_{OV} = 0.5V
$I_{GATEDOWN}$	GATE drive pull-down current	40	-	-	mA	V_{UV} = 0V, V_{OV} = 0.5V
Ramp Timing Control *(Test conditions: C_{LOAD} = 100µF, C_{RAMP} = 10nF, V_{UV} = 1.9V, V_{OV} = 0.5V, External MOSFET is IRF530[3])*						
I_{RAMP}	Ramp pin output current	-	10	-	µA	V_{SENSE} = 0V
t_{POR}	Time from UV to GATE turn on[1]	2.0	-	-	ms	---
t_{RISE}	Time from GATE turn on to V_{SENSE} limit	400	-	-	µs	---
t_{LIMIT}	Duration of current limit mode	-	5.0	-	ms	---
$t_{\overline{PWRGD}}$	Time from current limit to $\overline{PWRGD}$	-	5.0	-	ms	---
V_{RAMP}	Voltage on ramp pin in current limit mode[2]	-	3.6	-	V	---
$t_{STARTLIMIT}$	Start up time limit	80	100	120	ms	---
t_{CBTRIP}	Circuit breaker delay time	2.0	-	5.0	µs	May be extended by external RC circuit
t_{AUTO}	Automatic restart delay time	12	-	-	s	---
Power Good Output						
$V_{\overline{PWRGD}(HI)}$	Power good pin breakdown voltage	90	-	-	V	$\overline{PWRGD}$ is high
$V_{\overline{PWRGD}(LO)}$	Power good pin output low voltage	-	0.5	0.8	V	$I_{\overline{PWRGD}}$ = 1.0mA, $\overline{PWRGD}$ is low
Dynamic Characteristics						
$t_{GATEHLOV}$	OV delay	-	-	500	ns	---
$t_{GATEHLUV}$	UV delay	-	-	500	ns	---

Notes:

1. *This timing depends on the threshold voltage of the external N-Channel MOSFET. The higher its threshold is, the longer this timing.*
2. *This voltage depends on the characteristics of the external N-Channel MOSFET. V_{th} = 3.0V for an IRF530.*
3. *IRF530 is a registered trademark of International Rectifier.*

Functional Block Diagram



Functional Description

The HV311 provides control over the power supply current on systems where circuit cards are inserted into live backplanes. Such systems can frequently be found in the telecom, data networking and computing industry. The device provides means of limiting the power supply current after contact with the live backplane is made, thereby protecting card and backplane connectors and reducing the voltage disturbance on the backplane's power supply. Additional protection is provided in the form of a circuit breaker function and a start-up time limiter, both for protection of the external MOSFET and the system as a whole.

Start-up Sequence

After first contact is made with the backplane, the HV311 tries to establish an internal bias supply of 10V. During this time, GATE and RAMP are positively held low by circuitry that can operate with partial supply voltage, and $\overline{\text{PWRGD}}$ is in a high impedance state.

When the internal bias supply is in regulation, the undervoltage (UV) and overvoltage (OV) comparators start monitoring the external power supply. External resistor dividers at UV and OV pin set the window for normal operating supply voltage. These may be two individual dividers, or a single divider with two taps, as shown in the application diagrams.

Once the power supply voltage is within normal operating range, a 10µA internal source turns on to charge an external capacitor at the RAMP pin. The voltage at the GATE output follows the RAMP pin voltage with an offset of about 2.5V for control of the external MOSFET.

Power supply current starts to flow once the GATE voltage reaches the MOSFET threshold voltage, which is typically in the 2.0 to 4.0V range. The current sense amplifier at the SENSE pin reduces the RAMP charging current in proportion to the supply current, thereby slowing the voltage rise at RAMP, and thus the rise of the GATE voltage. At a sense voltage of 50mV the RAMP current is reduced to zero, and the RAMP and GATE voltages stop rising, thereby preventing a further rise in the power supply current.

Functional Description *(cont.)*

Once external power supply capacitors are charged, the power supply current subsides, and the RAMP current increases again to its maximum value of 10µA. The RAMP and GATE voltages resume their rise. When the RAMP voltage is within 1.2V of the internal supply, then GATE is connected to the internal supply, and the open-drain $\overline{\text{PWRGD}}$ pin is pulled low, marking the end of the start-up.

If the start-up sequence is not finished within 100ms, then the internal start-up timer causes a reset of the RAMP and GATE voltage to 0V, and the automatic retry timer is started to allow the MOSFET to cool off. After the retry delay a new startup sequence is initiated if the power supply voltage is within the normal operating range, as determined by the UV and OV comparators.

The circuit breaker monitors the sense amplifier for the presence of an overcurrent condition at all times. The overcurrent threshold is set at twice the maximum inrush current threshold. Should overcurrent occur, then RAMP and GATE are brought to zero, $\overline{\text{PWRGD}}$ returns to high impedance, and the automatic retry timer is started.

The automatic retry timer can be disabled by attachment of an additional resistor at the RAMP pin if a latched shutdown is desired.

A further reduction in the ramp rate of the RAMP and GATE voltages can be attained by connection of a feedback capacitor from the drain node to the RAMP pin. During startup the drain voltage drops at a rate proportional to the inrush current. This falling voltage waveform can be used to further reduce the current that flows onto the RAMP capacitor, thereby reducing the maximum inrush current.

Design Information

Setting up the UV and OV comparators

The following example shows how the resistors for the threshold setting divider can be determined. The procedure applies to the (R1, R2, R3) divider having two taps as shown on the typical applications diagram.

The following procedure bases the selection of the divider resistors on specification of the shutdown / disable voltages. A similar procedure can be devised that bases selection on specification of the enable voltages.

Let's assume the following:

- nominal divider current draw I_{NOM} = 100µA,
- nominal power supply voltage V_{NOM} = 50V,
- overvoltage shutdown voltage V_{OVS} = 65V,
- undervoltage shutdown voltage V_{UVS} = 35V,
- negligible (UV, OV) comparator input currents,
- Comparator rising threshold V_{RTH} = 1.26V
- Comparator falling threshold V_{FTH} = 1.16V

The following applies:

- $R_{123} = (R_1 + R_2 + R_3)$
- $R_{123} = V_{NOM} / I_{NOM}$
- R_{123} = 500kΩ

R_3 follows from the OV shutdown voltage:

- $DF_{OV} = R_3 / R_{123}$
- $V_{RTH} = V_{OVS} \cdot DF_{OV}$
- $R_3 = R_{123} \cdot V_{RTH} / V_{OVS}$
- R_3 = 9.692kΩ (97.6k 1%)

R_2 follows from the UV shutdown voltage:

- $DF_{UV} = (R_2 + R_3) / R_{123}$
- $V_{FTH} = V_{UVS} \cdot DF_{UV}$
- $R_2 + R_3 = R_{123} \cdot V_{FTH} / V_{UVS}$
- R2 = 6.879kΩ (6.81k 1%)

And:

- R1 = 483.429kΩ (487k 1%)

Now the upper and lower enable voltages can be determined:

- Lower Enable Voltage V_{LEN}
- Upper Enable Voltage V_{UEN}
- $V_{RTH} = DF_{UV} \cdot V_{LEN}$
- $V_{FTH} = DF_{OV} \cdot V_{UEN}$
- V_{LEN} = 38.0V
- V_{UEN} = 59.8V

Programming Maximum Inrush Current and Circuit Breaker Current

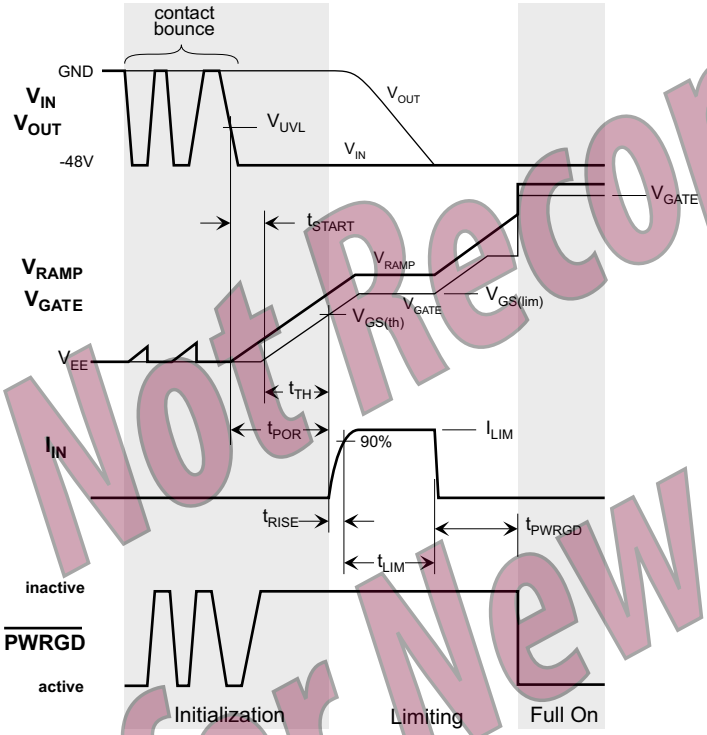
The values of the current limit threshold voltage V_{CL} and the external current sense resistor R_{CS} determine the maximum power supply current during startup I_{MAX} (the maximum inrush current). Similarly the circuit breaker trip current I_{CB} is determined by the values of the circuit breaker threshold voltage V_{CB} and the value of R_{CS}.

Design Information *(cont.)*

A numerical example:

V_{CL} = 50mV
V_{CB} = 100mV
R_{CS} = 10mΩ
$I_{MAX} \cdot R_{CS} = V_{CL}$
$I_{CB} \cdot R_{CS} = V_{CB}$
I_{MAX} = 5.0A
I_{CB} = 10A

Timing



The figure shows the sequence of events during startup and associated timing characteristics. The following is a discussion of timing values assuming the following component values:

- C_{RAMP} = 10nF
- C_{LOAD} = 100µF
- V_{VDD} = 48V
- MOSFET = IRF530
- $V_{GS(TH)}$ = 3.0V
- g_m = 7.4S
- R_{CS} = 50mΩ (I_{MAX} = 1.0A)

A number of false starts may be caused by contact bounce at the card edge. The startup begins when V_{VIN} rises through the lower enable voltage V_{LEN}, whose level is programmed at the UV comparator.

t_{START}

During this time the RAMP voltage rises steadily as the 10µA current source charges capacitor C_{RAMP}. The voltage at the GATE pin starts to follow the RAMP pin voltage when V_{RAMP} reaches a fixed offset voltage V_{OFS} of about 1.2V after a delay indicated as t_{START} in the figure.

- $t_{START} \cdot I_{RAMP} = V_{OFS} \cdot C_{RAMP}$
- $t_{START} = (1.2)(10n)/(10µ)$
- t_{START} = 1.2ms

t_{TH}

This time interval is associated with the rise of the GATE voltage from zero to the gate threshold voltage of the external MOSFET.

- $t_{TH} \cdot I_{RAMP} = V_{GS(TH)} \cdot C_{RAMP}$
- $t_{TH} = (3)(10n)/(10µ)$
- t_{START} = 3.0ms

t_{RISE}

During this time period the drain current rises more or less exponentially to the maximum inrush current I_{MAX}. As current rises from zero, the RAMP current is reduced by the action of the current sense amplifier, hence the more or less exponential current rise. t_{RISE} is here defined as the time to reach 90% of I_{MAX}.

- 90% rise corresponds to 2.3τ
- $I_{RAMP} \cdot \tau = C_{RAMP} \cdot \Delta V_{GS}$
- $I_{MAX} \approx g_m \cdot \Delta V_{GS}$
- $t_{RISE} \approx 2.3(C_{RAMP} \cdot I_{MAX}) / (I_{RAMP} \cdot g_m)$
- $t_{RISE} \approx (2.3)(10n)(1)/(10µ)(7.4) = 0.3ms$

t_{LIM}

During this time period the external load capacitor is charged at I_{MAX}.

- $I_{MAX} \cdot t_{LIM} = C_{LOAD} \cdot V_{VDD}$
- $t_{LIM} = (100µ)(48) / (1)$
- t_{LIM} = 4.8ms

$t_{\overline{PWRGD}}$

Final rise of GATE voltage to V_{REG} minus about 1.2V.

- $I_{RAMP} \cdot t_{\overline{PWRGD}} = C_{RAMP} \cdot (V_{REG} – (1.2V + V_{GS(TH)} + \Delta V_{GS}))$
- $t_{\overline{PWRGD}} = (10n)(10 – (1.2 + 3 + 1/7.4)/(10µ)$
- $t_{\overline{PWRGD}}$ = 4.3ms

Startup Timer

The startup timer limits the startup to 100ms. Should there be an overload or short circuit during startup, then the external pass transistor will carry current for no more than 100ms. Upon tripping of the timer the RAMP and GATE voltages reset to zero, and the autoretry timer starts if enabled.

Circuit Breaker

The circuit breaker trips in less than 5.0µs when the voltage across the sense resistor reaches 100mV. Upon tripping of the circuit breaker the RAMP and GATE voltages reset to zero, and the autoretry timer starts if enabled.

Autoretry Timer

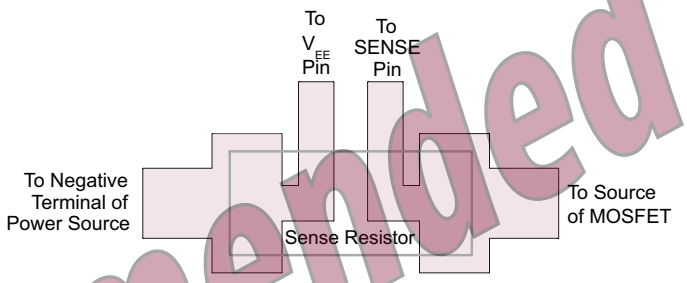
The retry interval is determined by charging and discharging the C_{RAMP} capacitor 256 times. One cycle corresponds to charging of C_{RAMP} to 8.0V with a current of 2.5µA, and subsequent discharging to zero with a current of 2.5µA. Hence:

- $I_{CHARGE} \cdot t_{CYCLE} = C_{RAMP} \cdot 2 \cdot \Delta V$
- $t_{CYCLE} = (10n)(2)(8)/(2.5µ)$
- $t_{CYCLE} = 64ms$
- $t_{AUTORETRY} = (256)(64m)$
- $t_{AUTORETRY} = 16.4s$

The autoretry timer can be disabled by adding a resistor at the RAMP pin. A resistor which keeps the RAMP voltage from rising to 8.0V will keep the timer from counting. This can accomplished by adding a resistor at the RAMP pin with a value of about 2.5MΩ. Note that this resistor forms an additional load during the startup, thereby causing the time intervals to increase somewhat.

Kelvin Connections

In order to make an accurate measurement of power supply current it is advisable to make use of Kelvin connections. The idea is to not incur voltage drops in the sense leads due to the main power supply current. See diagram below.



Paralleling External MOSFETs

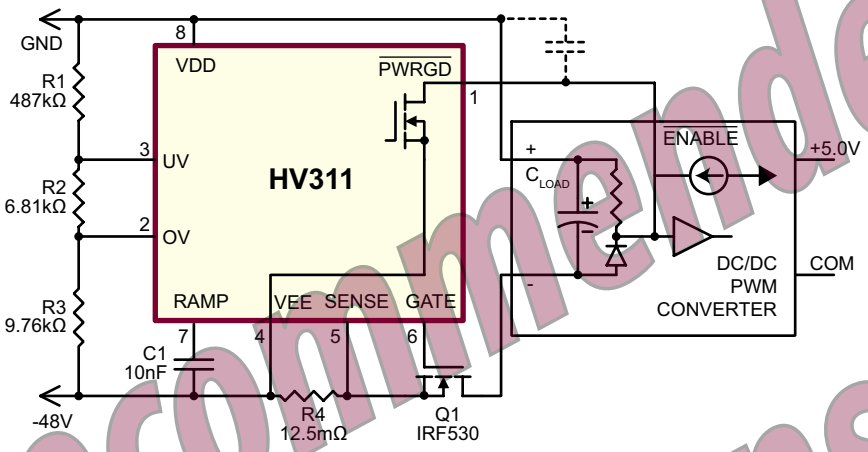
Equal current sharing may not be achievable due to the tolerance issues with the threshold voltage and gain characteristics of the MOSFETs. Paralleling of devices is not recommended. The issues with paralleling can be alleviated by using resistor ballasting.

For this application the HV311 with active low $\overline{\text{PWRGD}}$ is recommended where the $\overline{\text{PWRGD}}$ pins of multiple hot swap circuits can be connected in a wired OR configuration.

Application Circuit 1

$\overline{\text{PWRGD}}$ Output

Many DC/DC PWM converters reference their $\overline{\text{ENABLE}}$ inputs to the negative input terminal. If the $\overline{\text{ENABLE}}$ input is active LOW then the HV311 can be directly connected as shown below **(Application Circuit 1)** since the open drain $\overline{\text{PWRGD}}$ output is in a High-Z state until the external MOSFET is fully turned on and the potential on the negative input of the converter is essentially the same as the VEE pin of the HV311.

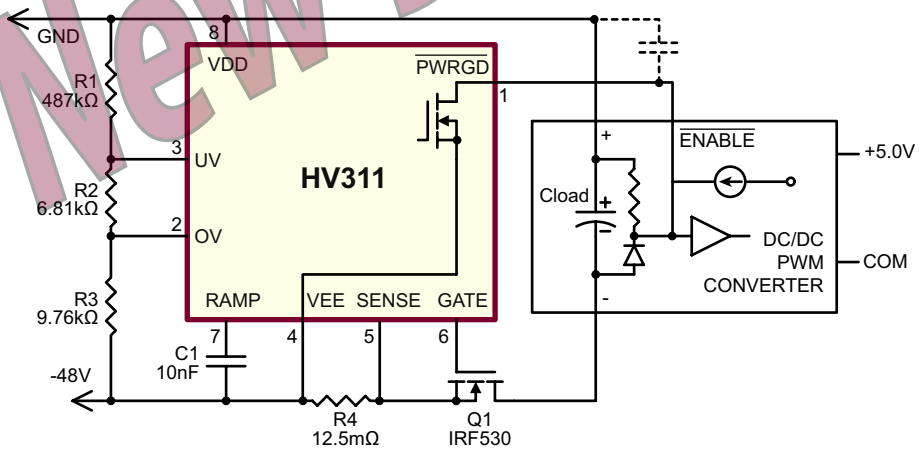


Note:

A capacitor may be needed to slow $\overline{\text{PWRGD}}$ dv/dt if gate oscillations are observed when V_{IN} is close to OV_{LO}.

Application Circuit 2

However, if the DC/DC PWM Converter with the $\overline{\text{ENABLE}}$ input circuit configuration was active HIGH, then the apparent choice of the HV311 would result in the creation of a current path through the protective diode clamp of the $\overline{\text{ENABLE}}$ input and the $\overline{\text{PWRGD}}$ output MOSFET of the HV311. For this situation the HV311 should be used as shown below.

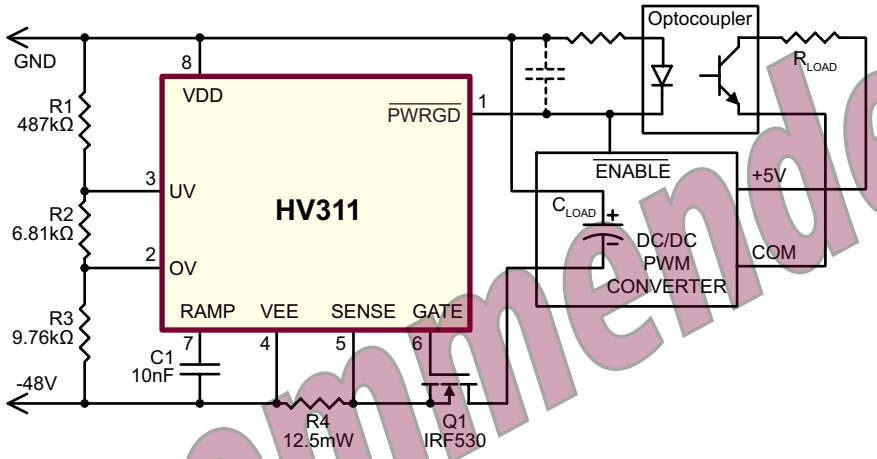


Note:

A capacitor may be needed to slow $\overline{\text{PWRGD}}$ dv/dt if gate oscillations are observed when V_{IN} is close to OV_{LO}.

Application Circuit 3

In some applications the $\overline{\text{PWRGD}}$ signal is used to activate load circuitry on the isolated output side of the DC/DC PWM Converter. In this situation an optocoupler is needed to provide the required isolation as shown below.

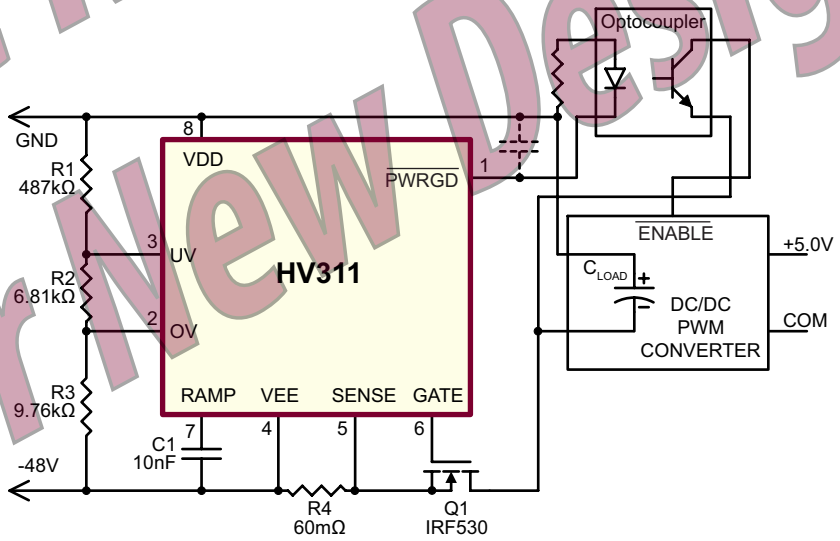


Note:

A capacitor may be needed to slow $\overline{\text{PWRGD}}$ dv/dt if gate oscillations are observed when V_{IN} is close to OV_{LO}.

Application Circuit 4

When the details of the load $\overline{\text{ENABLE}}$ circuitry is not known, using an optocoupler always provides a safe solution.



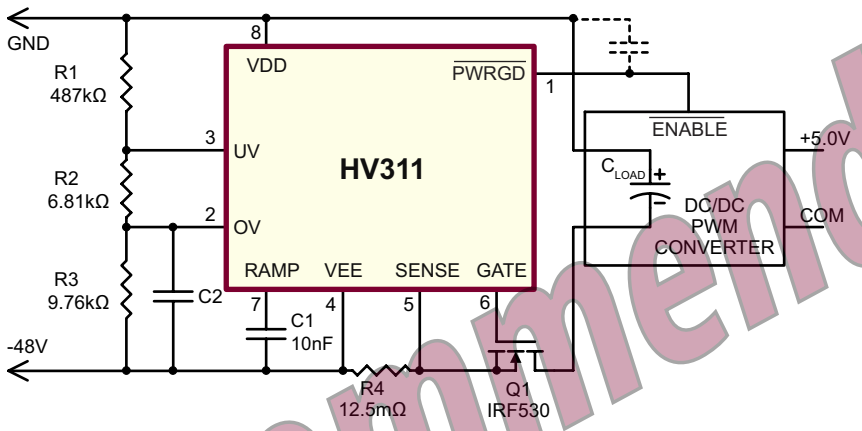
Note:

A capacitor may be needed to slow $\overline{\text{PWRGD}}$ dv/dt if gate oscillations are observed when V_{IN} is close to OV_{LO}.

Application Circuit 5

Filtering Voltage Spikes on Input Supply

In some systems over voltage spikes of very short duration may exist. For these systems a small capacitor may be added from the OV pin to the VEE pin to filter the voltage spikes.

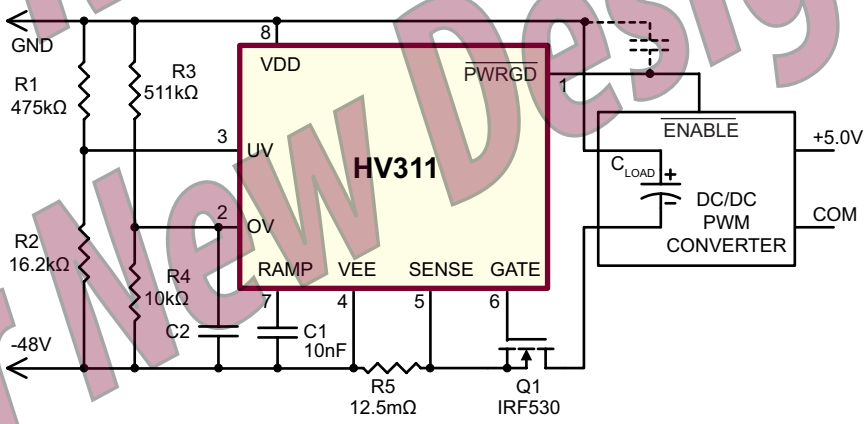


Note:

A capacitor may be needed to slow $\overline{PWRGD}$ dv/dt if gate oscillations are observed when V_{IN} is close to OV_{LO}.

Application Circuit 6

Unfortunately this will also cause some delay in responding to UV conditions. If this UV delay is not acceptable, then separate resistor dividers can be provided for OV and UV with a capacitor connected from OV pin to the VEE pin.



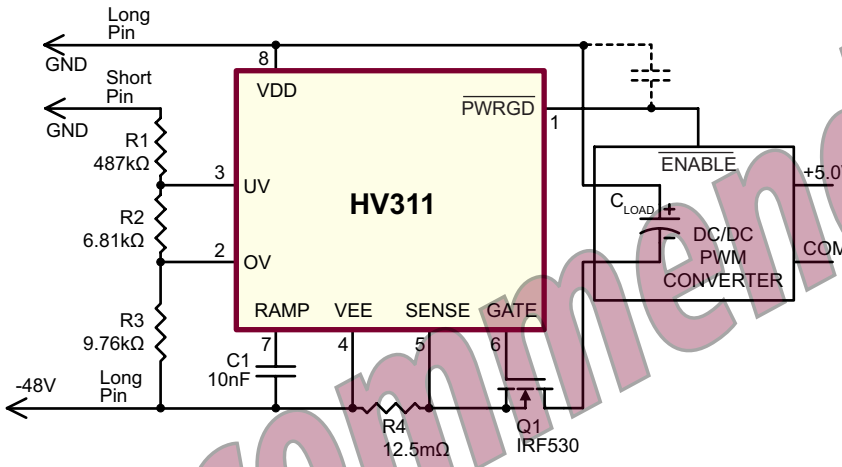
Note:

A capacitor may be needed to slow $\overline{PWRGD}$ dv/dt if gate oscillations are observed when V_{IN} is close to OV_{LO}.

Application Circuit 7

Using Short Connector Pin

In some systems short connector pins are used to guarantee that the power pins are fully mated before the hot swap control circuit is enabled. For these systems the positive (VDD) end of the R1, R2, and R3 resistor divider should be connected to

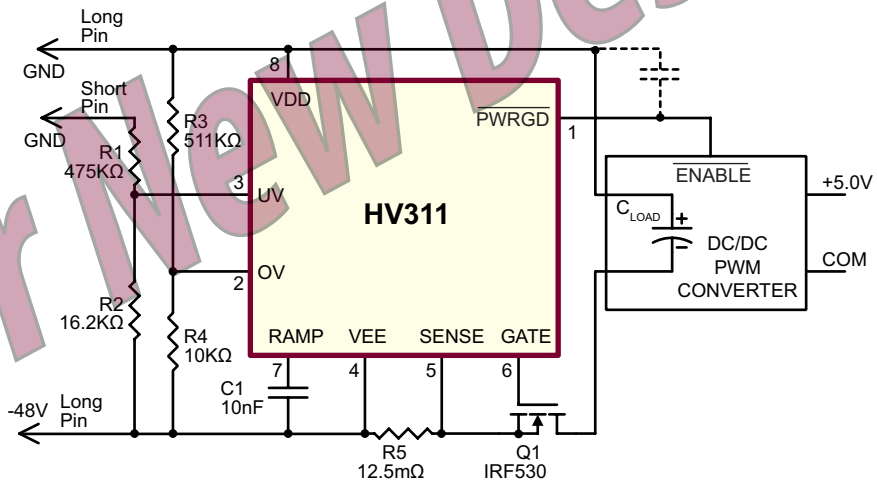


Note:

A capacitor may be needed to slow $\overline{PWRGD}$ dv/dt if gate oscillations are observed when V_{IN} is close to OV_{LO}.

Application Circuit 8

If separate resistor dividers are used for OV and UV, then only the positive (VDD) end of the UV resistor divider should be connected to the short pin.

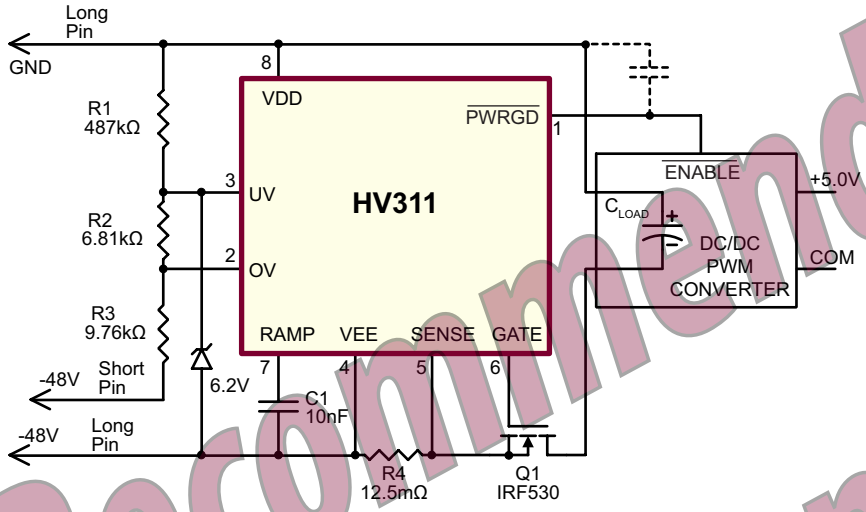


Note:

A capacitor may be needed to slow $\overline{PWRGD}$ dv/dt if gate oscillations are observed when V_{IN} is close to OV_{LO}.

Application Circuit 9

If a system requires the use of a short connector pin on the negative supply lead to guarantee that the power pins are fully mated before the hot swap control circuit is enabled and uses separate resistor dividers for UV and OV, then a 6.2 to 10V Zener diode must be connected from the OV pin to the VEE pin and only the OV divider should be connected to the short pin.

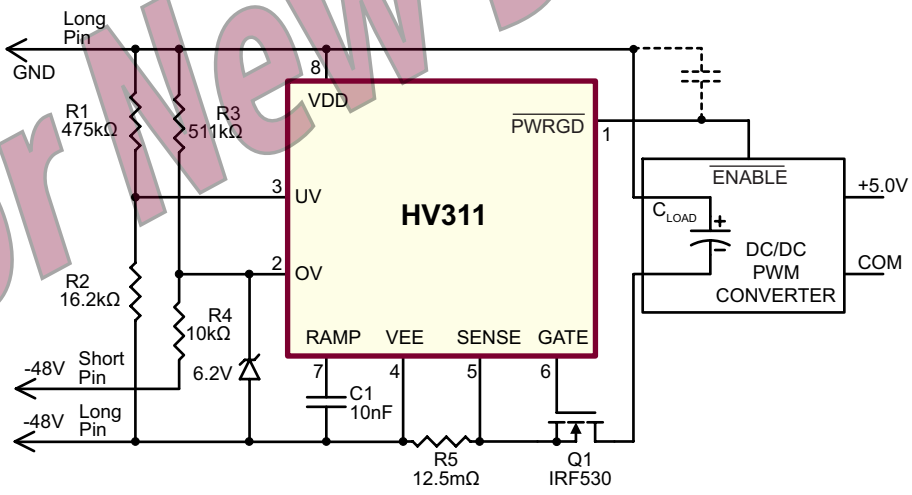


Note:

A capacitor may be needed to slow $\overline{PWRGD}$ dv/dt if gate oscillations are observed when V_{IN} is close to OV_{LO}.

Application Circuit 10

If a system requires the use of a short connector pin on the negative supply lead to guarantee that the power pins are fully mated before the hot swap control circuit is enabled and uses separate resistor dividers for UV and OV, then a 6.2V to 10V zener diode must be connected from the OV pin to the VEE pin and only the OV divider should be connected to the short pin.



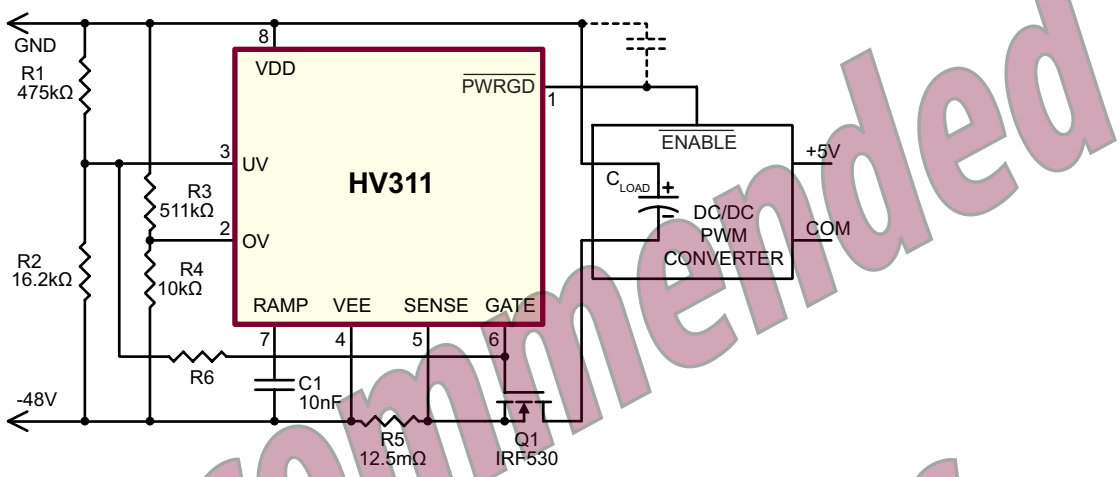
Note:

A capacitor may be needed to slow $\overline{PWRGD}$ dv/dt if gate oscillations are observed when V_{IN} is close to OV_{LO}.

Application Circuit 11

Increasing Under Voltage Hysteresis

If the internally fixed under voltage hysteresis is insufficient for a particular system application, then it may be increased by using separate resistor dividers for OV and UV and providing a resistor feedback path from the GATE pin to the UV pin.



Note:

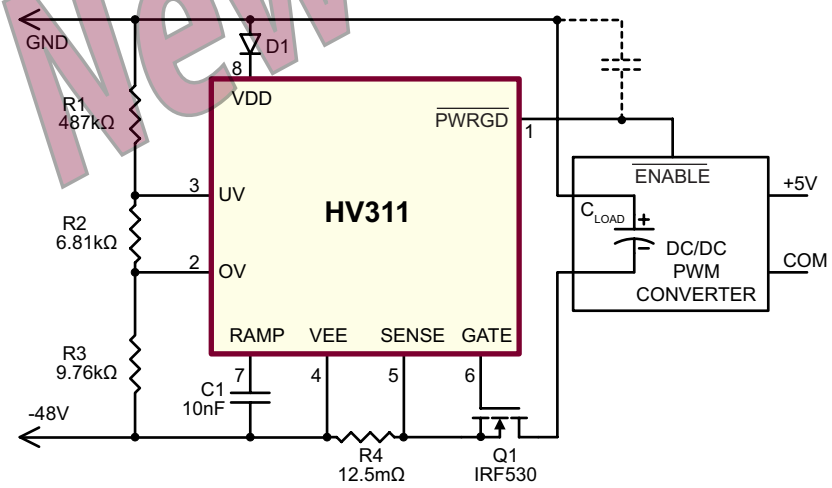
A capacitor may be needed to slow $\overline{PWRGD}$ dv/dt if gate oscillations are observed when V_{IN} is close to OV_{LO}.

Application Circuit 12

Reverse Polarity Protection

The UV and OV pins are protected against reverse polarity input supplies by internal clamping diodes and the fault currents are sufficiently limited by the impedance of the external resistor divider, however, a low current diode with a 100V breakdown rating must be inserted in series with the VDD pin.

This method (shown in **Application Circuit 12**) will protect the hot swap control circuit however, due to the intrinsic diode in the external MOSFET, the load will not be protected from reverse polarity voltages.



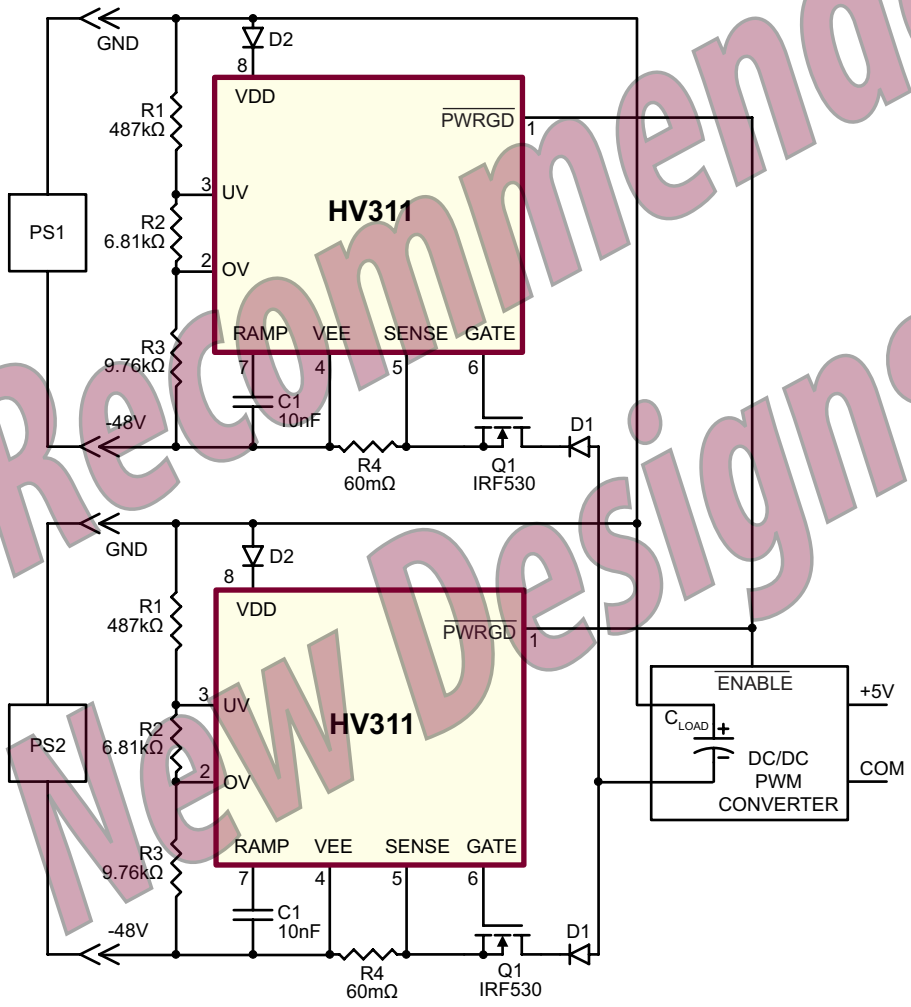
Note:

A capacitor may be needed to slow $\overline{PWRGD}$ dv/dt if gate oscillations are observed when V_{IN} is close to OV_{LO}.

Application Circuit 13

Redundant Supplies

Many systems use redundant primary power supplies or battery backup. When redundant AC powered sources are used they are generally diode OR'ed to the load on the hot terminal. For these systems, the use of independent hot swap controllers is recommended with the diode OR'ing provided after the hot swap controllers. The HV311 is ideally suited for such applications since two or more active low $\overline{\text{PWRGD}}$ signals can be connected to a single active low $\overline{\text{ENABLE}}$ pin, thus enabling the load as long as at least one primary power source is available. By adding low current 100V diodes in series with the VDD pins, full reverse polarity protection on either power source is also provided.



NOTES: 1. Undervoltage Shutdown (UV) set to 35V.
2. Overvoltage Shutdown (OV) set to 65V.
3. Current Limit set to 0.83A.

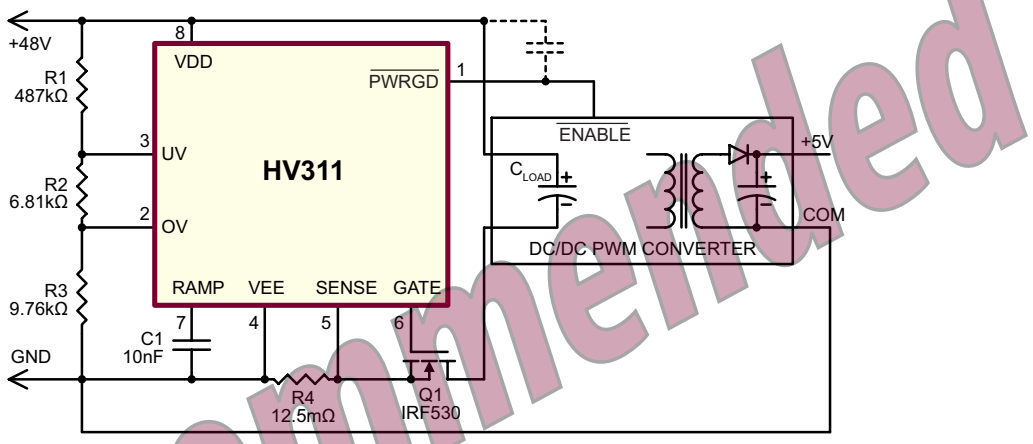
Note:

A capacitor may be needed to slow $\overline{\text{PWRGD}}$ dv/dt if gate oscillations are observed when V_{IN} is close to OV_{LO}.

Application Circuit 14

Use with Negative Ground

The HV311 may be used with many positive ground systems where DC/DC PWM converters have isolated outputs and their inputs need not be ground referenced.



Note:

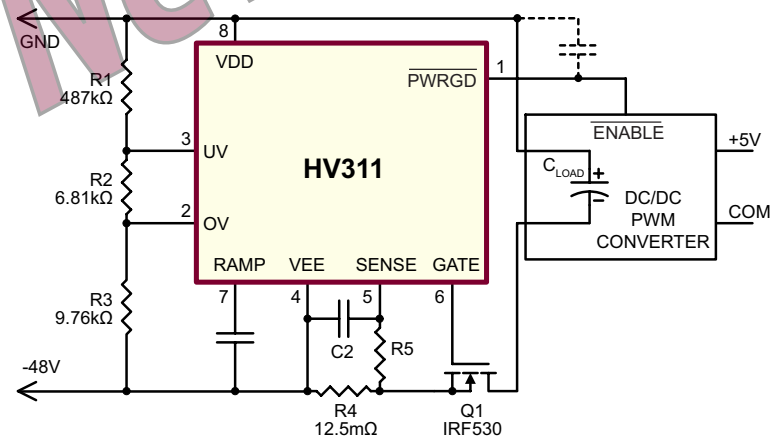
A capacitor may be needed to slow $\overline{PWRGD}$ dv/dt if gate oscillations are observed when V_{IN} is close to OV_{LO}.

Application Circuit 15

Extending Circuit Breaker Delay

Connecting a resistor in series with the SENSE pin and a capacitor between the SENSE and VEE pins as shown in the following diagram may be used to extend the circuit breaker delay time beyond the 5µs internally set delay time.

The time delay achievable by this method is limited since this **Application Circuit 7** delay circuit will also effect the current control feedback loop and will result in a current overshoot during the external pass device turn on transition to current limit. If the time delay required for the circuit breaker causes excessive current overshoot during the turn on transition then the following circuit may be used, where the RC filter is switched on after the completion of the current limit control function of the hot swap controller.



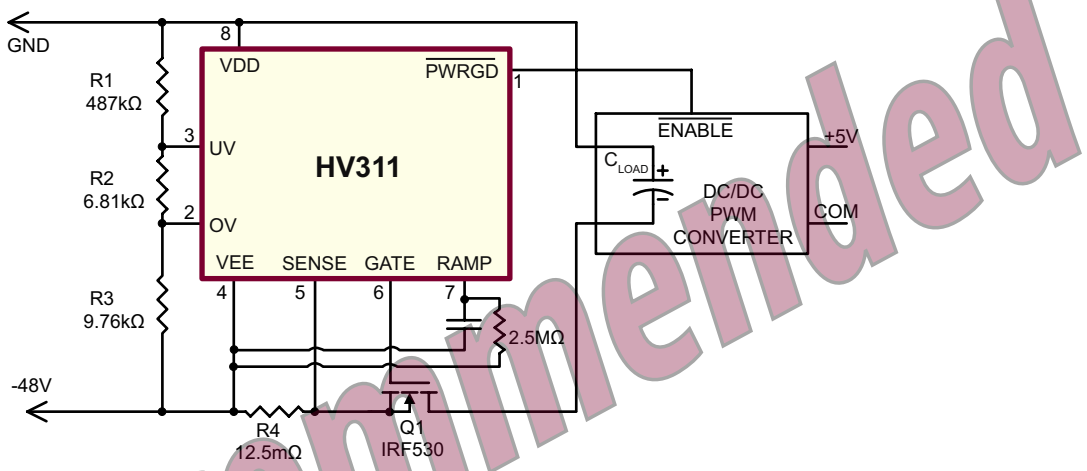
Note:

A capacitor may be needed to slow $\overline{PWRGD}$ dv/dt if gate oscillations are observed when V_{IN} is close to OV_{LO}.

Application Circuit 16

Latched Operations

For those applications that need to disable the auto retry capability, the following circuit disables the auto retry feature.



Note:

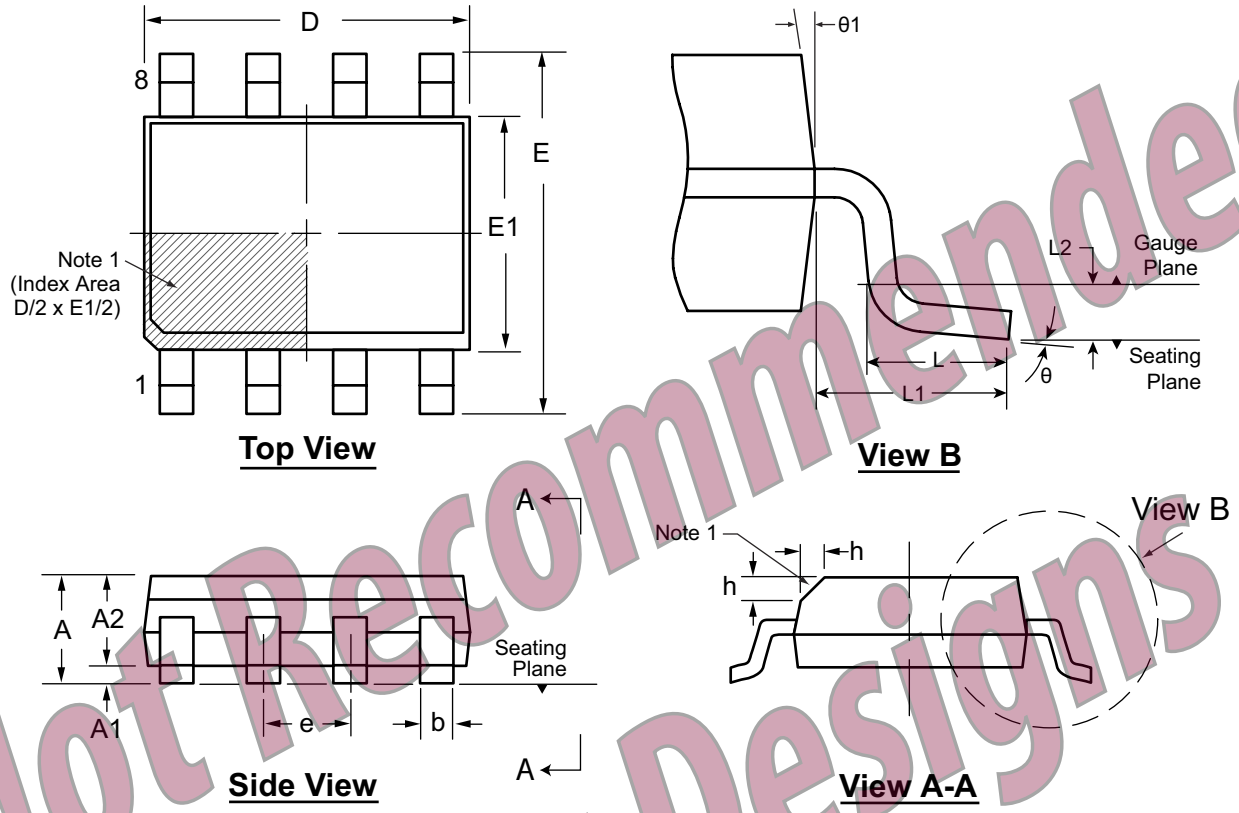
A capacitor may be needed to slow $\overline{PWRGD}$ dv/dt if gate oscillations are observed when V_{IN} is close to OV_{LO}.

Pin Description

Pin #	Name	Description
1	$\overline{PWRGD}$	The power good output pin. Pin is an open-drain output. Connect to power module enable pins and the like with internal or external pull-up resistor(s). This open-drain pin is high impedance during the start-up phase, during fault, and automatic retry periods, and low otherwise.
2	OV	The overvoltage input pin. Input to the OV/UV window comparator. Monitors the power supply voltage, for purpose of detecting the normal operating voltage condition.
3	UV	The undervoltage input pin. Input to the OV/UV window comparator. Monitors the power supply voltage, for purpose of detecting the normal operating voltage condition.
4	VEE	The negative power supply pin. Connect to the negative of the incoming power supply.
5	SENSE	The current sense pin. Connect the current sense resistor between the VEE and SENSE pins. Regulates the Inrush current to 50mV equivalent. Trips on over current at 100mV equivalent.
6	GATE	The gate output. Connect to the gate of external MOSFET. Connect the source of the MOSFET source to the VEE pin.
7	RAMP	The RAMP input pin. Connect a capacitor between this pin and VEE to control the ramp rate of the voltage at the GATE pin during power-up. Add a resistor of about 2.5MΩ to disable the autoretry feature.
8	VDD	The positive power supply pin. Connect to the positive of the incoming power supply.

8-Lead SOIC (Narrow Body) Package Outline (LG)

4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note:

1. *This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.

** This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.*

Drawings are not to scale.

Supertex Doc. #: *DSPD-8SOLGTG, Version H101708.*

(The package drawings in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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