

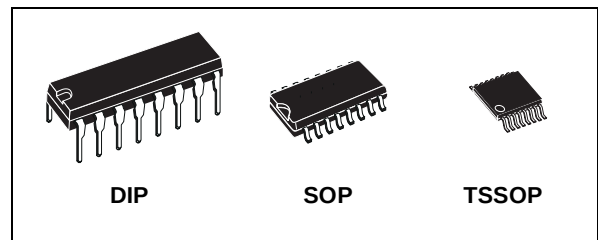
DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

- HIGH SPEED :
 $t_{PD} = 23 \text{ ns (TYP.) at } V_{CC} = 6V$
- LOW POWER DISSIPATION:
 STAND BY STATE :
 $I_{CC} = 4\mu A \text{ (MAX.) at } T_A = 25^\circ C$
 ACTIVE STATE :
 $I_{CC} = 200\mu A \text{ (MAX.) at } V_{CC} = 5V$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28 \% V_{CC} \text{ (MIN.)}$
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 4mA \text{ (MIN.)}$
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \approx t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
 $V_{CC} \text{ (OPR)} = 2V \text{ to } 6V$
- WIDE OUTPUT PULSE WIDTH RANGE :
 $t_{WOUT} = 120 \text{ ns} \sim 60 \text{ s OVER AT } V_{CC} = 4.5 V$
- PIN AND FUNCTION COMPATIBLE WITH
 74 SERIES 123

DESCRIPTION

The M74HC123A is an high speed CMOS MONOSTABLE MULTIVIBRATOR fabricated with silicon gate C²MOS technology.

There are two trigger inputs, A INPUT (negative edge) and B INPUT (positive edge). These inputs are valid for slow rising/falling signals, ($t_r = t_f = 1 \text{ sec}$). The device may also be triggered by using the CLR input (positive-edge) because of the Schmitt-trigger input; after triggering the output maintains the MONOSTABLE state for the time



ORDER CODES

PACKAGE	TUBE	T & R
DIP	M74HC123AB1R	
SOP	M74HC123AM1R	M74HC123ARM13TR
TSSOP		M74HC123ATTR

period determined by the external resistor Rx and capacitor Cx. When $C_x \geq 10nF$ and $R_x \geq 10K\Omega$, the output pulse width value is approximatively given by the formula : $t_W(OUT) = K \cdot C_x \cdot R_x$. ($K \approx 1$).

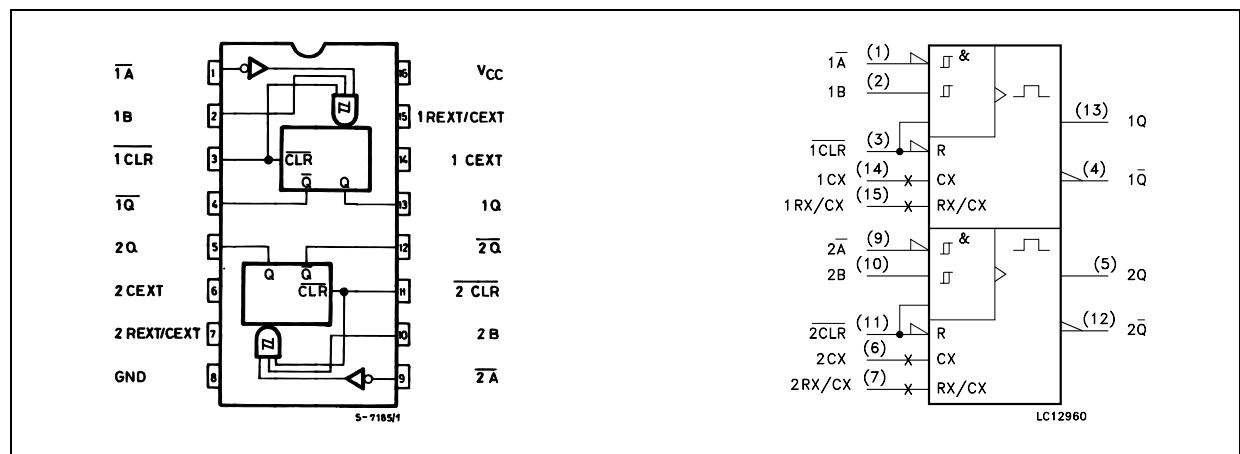
Taking CLR low breaks this MONOSTABLE STATE. If the next trigger pulse occurs during the MONOSTABLE period it makes the MONOSTABLE period longer. Limit for values of Cx and Rx : Cx : NO LIMIT

Rx : $V_{CC} < 3.0V$ 5K Ω to 1M Ω

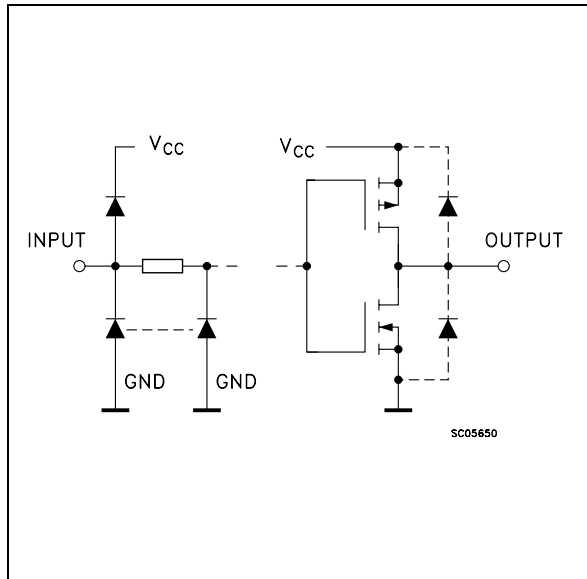
$V_{CC} \geq 3.0V$ 1K Ω to 1M Ω

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

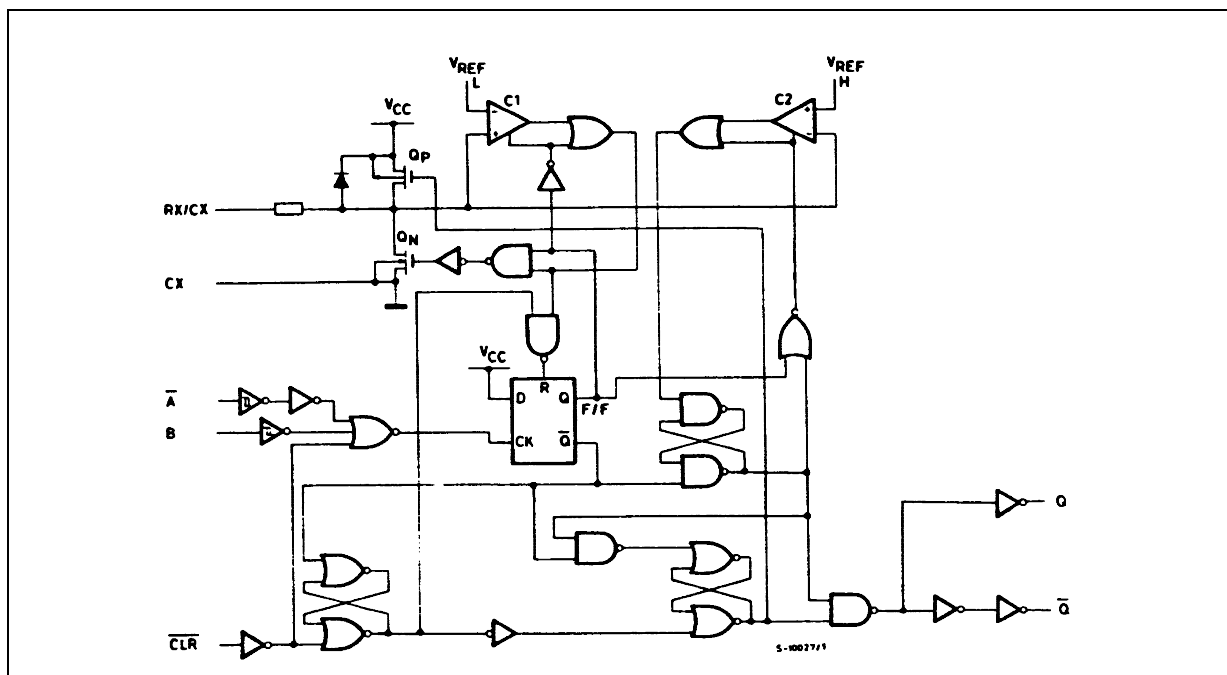
PIN No	SYMBOL	NAME AND FUNCTION
1, 9	$1\bar{A}, 2\bar{A}$	Trigger Inputs (Negative Edge Triggered)
2, 10	1B, 2B	Trigger Inputs (Positive Edge Triggered)
3, 11	$1\bar{CLR}$ 2 CLR	Direct Reset LOW and trigger Action at Positive Edge
4, 12	1Q, 2Q	Outputs (Active Low)
7	$2R_X/C_X$	External Resistor Capacitor Connection
13, 5	1Q, 2Q	Outputs (Active High)
14, 6	$1C_X$ 2C_X	External Capacitor Connection
15	$1R_X/C_X$	External Resistor Capacitor Connection
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

TRUTH TABLE

INPUTS			OUTPUTS		NOTE
$\bar{A}$	B	$\bar{CLR}$	Q	$\bar{Q}$	
	H	H			OUTPUT ENABLE
X	L	H	L	H	INHIBIT
H	X	H	L	H	INHIBIT
L		H			OUTPUT ENABLE
L	H				OUTPUT ENABLE
X	X	L	L	H	INHIBIT

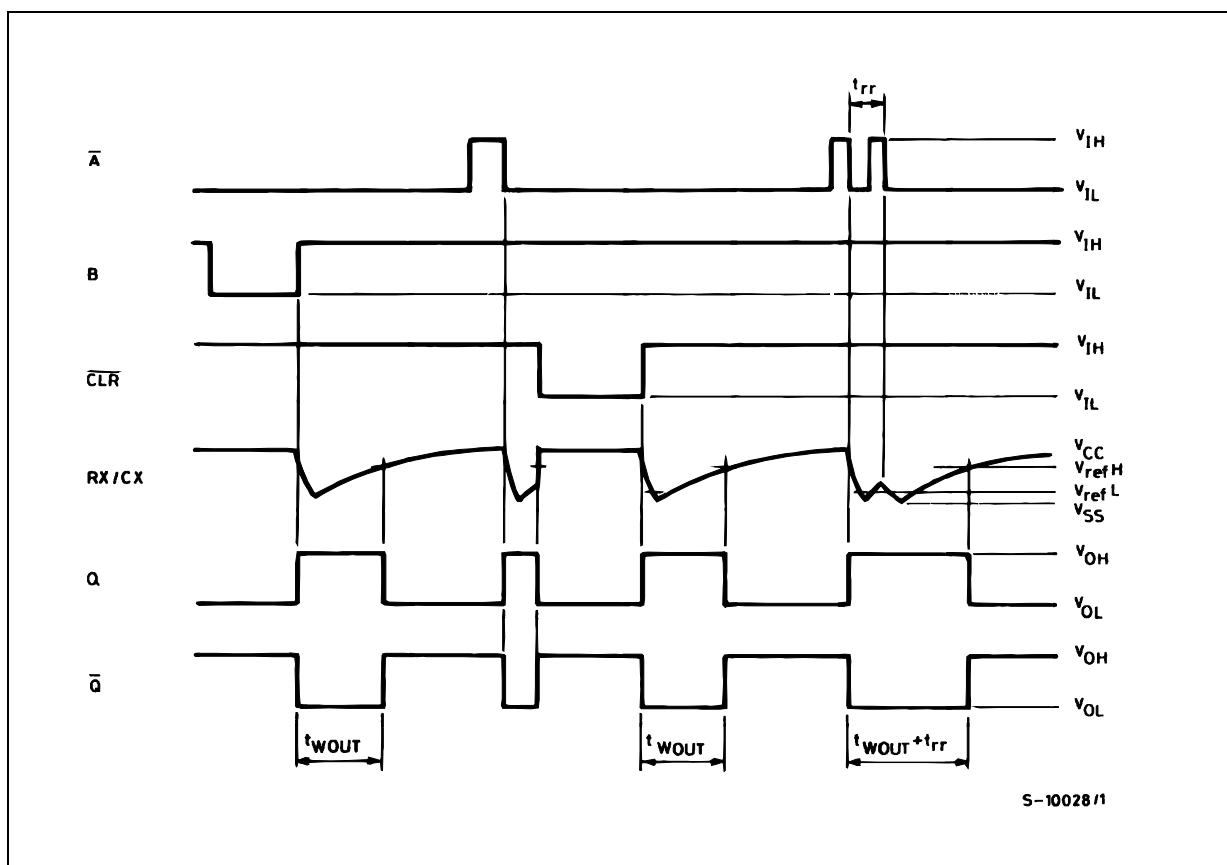
X : Don't Care

SYSTEM DIAGRAM

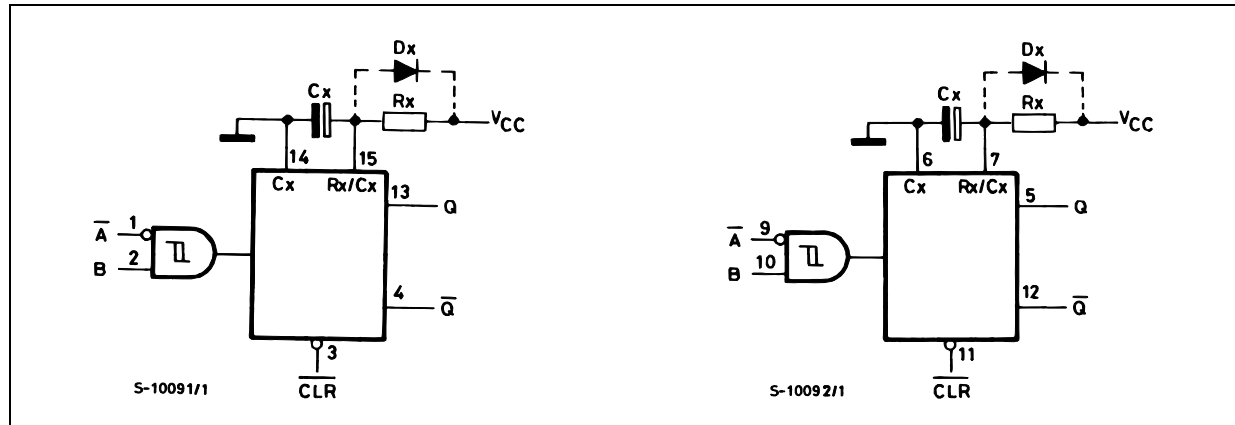


This logic diagram has not been used to estimate propagation delays

TIMING CHART



BLOCK DIAGRAM



(1) C_x , R_x , D_x are external components.

(2) D_x is a clamping diode.

The external capacitor is charged to V_{CC} in the stand-by-state, i.e. no trigger. When the supply voltage is turned off C_x is discharged mainly through an internal parasitic diode (see figures). If C_x is sufficiently large and V_{CC} decreases rapidly, there will be some possibility of damaging the I.C. with a surge current or latch-up. If the voltage supply filter capacitor is large enough and V_{CC} decrease slowly, the surge current is automatically limited and damage to the I.C. is avoided. The maximum forward current of the parasitic diode is approximately 20 mA. In cases where C_x is large the time taken for the supply voltage to fall to 0.4 V_{CC} can be calculated as follows:

$$t_f \geq (V_{CC} - 0.7) \times C_x / 20 \text{ mA}$$

In cases where t_f is too short an external clamping diode is required to protect the I.C. from the surge current.

FUNCTIONAL DESCRIPTION

STAND-BY STATE

The external capacitor, C_x , is fully charged to V_{CC} in the stand-by state. Hence, before triggering, transistor Q_p and Q_n (connected to the R_x/C_x node) are both turned-off. The two comparators that control the timing and the two reference voltage sources stop operating. The total supply current is therefore only leakage current.

TRIGGER OPERATION

Triggering occurs when:

- 1 st) A is "LOW" and B has a falling edge;
- 2 nd) B is "HIGH" and A has a rising edge;
- 3 rd) A is "LOW" and B is HIGH and C1 has a rising edge;

After the multivibrator has been retriggered comparator C1 and C2 start operating and Q_n is turned on. C_x then discharges through Q_n . The voltage at the node R/C external falls.

When it reaches V_{REFL} the output of comparator C1 becomes low. This in turn reset the flip-flop and Q_n is turned off.

At this point C1 stops functioning but C2 continues to operate.

The voltage at R/C external begins to rise with a time constant set by the external components R_x , C_x .

Triggering the multivibrator causes Q to go high after internal delay due to the flip-flop and the gate. Q remains high until the voltage at R/C external rises again to V_{REFH} . At this point C2

output goes low and O goes low. C2 stop operating. That means that after triggering when the voltage R/C external returns to V_{REFH} the multivibrator has returned to its MONOSTABLE STATE. In the case where $R_x \cdot C_x$ are large enough and the discharge time of the capacitor and the delay time in the I.C. can be ignored, the width of the output pulse $t_w(\text{out})$ is as follows:

$$t_w(\text{OUT}) = C_x \cdot R_x$$

RE - TRIGGERED OPERATION

When a second trigger pulse follows the first its effect will depend on the state of the multivibrator. If the capacitor C_x is being charged the voltage level of R/C external falls to V_{REFL} again and Q remains High i.e. the retrigger pulse arrives in a time shorter than the period $R_x \cdot C_x$ seconds, the capacitor charging time constant. If the second trigger pulse is very close to the initial trigger pulse it is ineffective; i.e. the second trigger must arrive in the capacitor discharge cycle to be ineffective; Hence the minimum time for a second trigger to be effective depends on V_{CC} and C_x .

RESET OPERATION

CL is normally high. If CL is low, the trigger is not effective because Q output goes low and trigger control flip-flop is reset.

Also transistor Q_p is turned on and C_x is charged quickly to V_{CC} . This means if CL input goes low the IC becomes waiting state both in operating and non operating state.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500(*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
t_r, t_f	Input Rise and Fall Time	$V_{CC} = 2.0V$	0 to 1000
		$V_{CC} = 4.5V$	0 to 500
		$V_{CC} = 6.0V$	0 to 400
Cx	External Capacitor	NO LIMITATION	pF
Rx	External Resistor	$V_{CC} < 3V$	5K to 1M
		$V_{CC} \geq 3V$	1K to 1M

The Maximum allowable values of Cx and Rx are a function of leakage of capacitor Cx, the leakage of device and leakage due to the board layout and surface resistance. Susceptibility to externally induced noise may occur for $R_x > 1M\Omega$

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit		
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C			
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.	
V _{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V	
		4.5		3.15			3.15		3.15			
		6.0		4.2			4.2		4.2			
V _{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V	
		4.5				1.35		1.35		1.35		
		6.0				1.8		1.8		1.8		
V _{OH}	High Level Output Voltage	2.0	I _O =-20 μA	1.9	2.0		1.9		1.9		V	
		4.5	I _O =-20 μA	4.4	4.5		4.4		4.4			
		6.0	I _O =-20 μA	5.9	6.0		5.9		5.9			
		4.5	I _O =-4.0 mA	4.18	4.31		4.13		4.10			
		6.0	I _O =-5.2 mA	5.68	5.8		5.63		5.60			
V _{OL}	Low Level Output Voltage	2.0	I _O =20 μA		0.0	0.1		0.1		0.1	V	
		4.5	I _O =20 μA		0.0	0.1		0.1		0.1		
		6.0	I _O =20 μA		0.0	0.1		0.1		0.1		
		4.5	I _O =4.0 mA		0.17	0.26		0.33		0.40		
		6.0	I _O =5.2 mA		0.18	0.26		0.33		0.40		
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND			± 0.1		± 1		± 1	μA	
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND			4		40		80	μA	
I _{CC} '	Active State Supply Current (1)	2.0	V _I = V _{CC} or GND Pin 7 or 15 V _{IN} = V _{CC} /2		45	200		260		320	μA	
		4.5			500	600		780		960	μA	
		6.0			0.7	1		1.3		1.6	mA	

(1) : Per Circuit

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t _{TLH} t _{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t _{PLH} t _{PHL}	Propagation Delay Time (A, B - Q, $\overline{Q}$)	2.0			102	210		265		315	ns
		4.5			29	42		53		63	
		6.0			22	36		45		54	
t _{PLH} t _{PHL}	Propagation Delay Time(CLR TRIGGER - Q, $\overline{Q}$)	2.0			102	235		295		355	ns
		4.5			31	47		59		71	
		6.0			23	40		50		60	
t _{PLH} t _{PHL}	Propagation Delay Time (CLR - Q, $\overline{Q}$)	2.0			68	160		200		240	ns
		4.5			20	32		40		48	
		6.0			16	27		34		41	
t _{WOUT}	Output Pulse Width	2.0	Cx = 100 pF Rx = 10KΩ		1.9						μs
		4.5			1.6						
		6.0			1.5						
		2.0	Cx = 0.1μF Rx = 100KΩ		9.8						ms
		4.5			9.5						
		6.0			9.4						
Δt _{WOUT}	Output Pulse Width Error Between Circuits in Same Package				±1						%
t _{W(H)} t _{W(L)}	Minimum Pulse Width	2.0				75		95		110	ns
		4.5				15		19		22	
		6.0				13		16		19	
t _{W(L)}	Minimum Pulse Width (CLR)	2.0				75		95		110	ns
		4.5				15		19		22	
		6.0				13		16		19	
t _{rr}	Minimum Retrigger Time	2.0	Cx = 100 pF Rx = 10KΩ		325						ns
		4.5			108						
		6.0			78						
		2.0	Cx = 0.1μF Rx = 100KΩ		5						μs
		4.5			1.4						
		6.0			1.2						

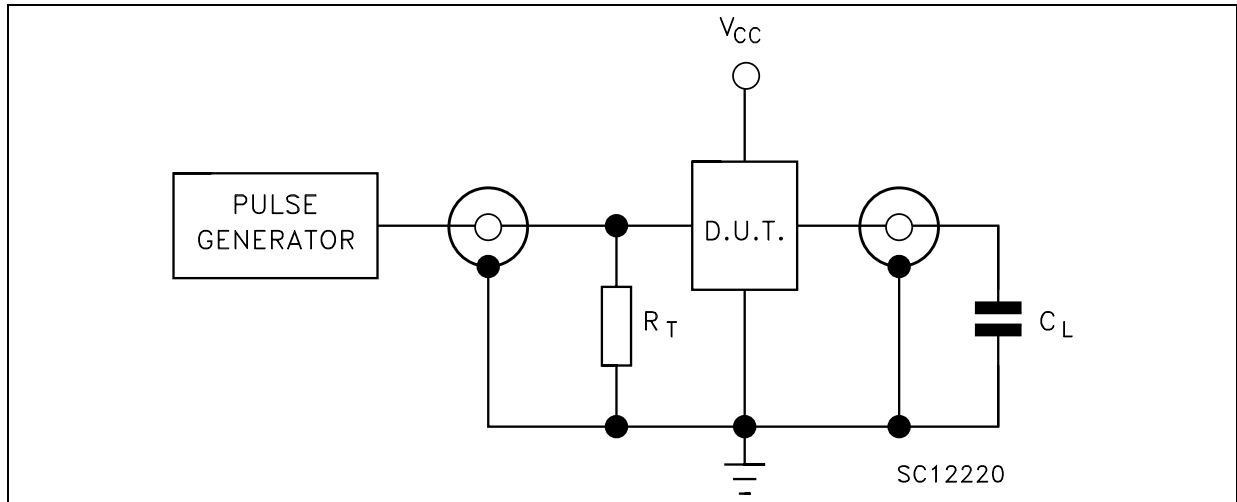
CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C _{IN}	Input Capacitance	5.0			5	10		10		10	pF
C _{PD}	Power Dissipation Capacitance (note 1)	5.0			162						pF

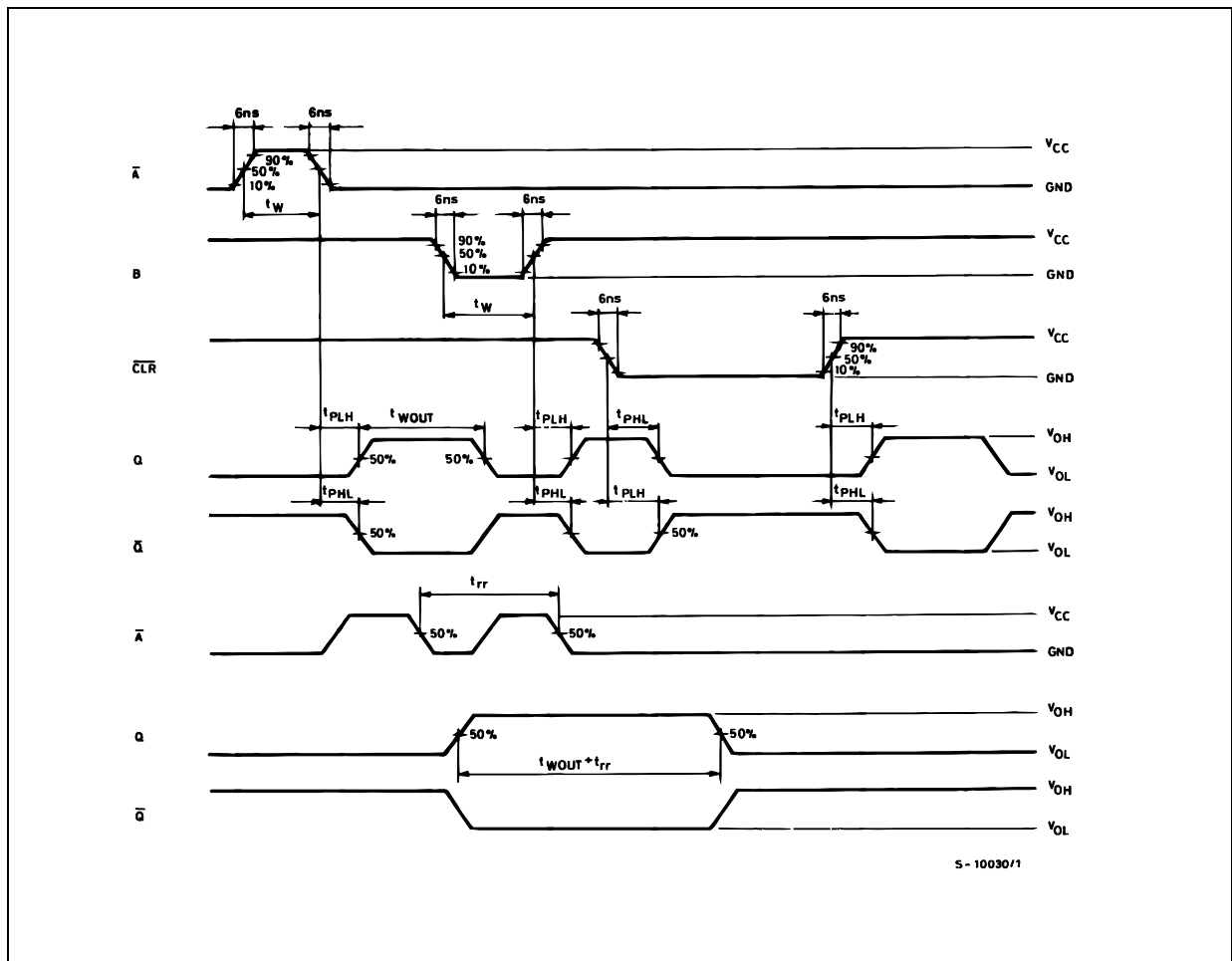
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}' \text{ Duty}/100 + I_{C2}/2$ (per monostable) (I_{CC}' : Active Supply current) (Duty : %)



TEST CIRCUIT

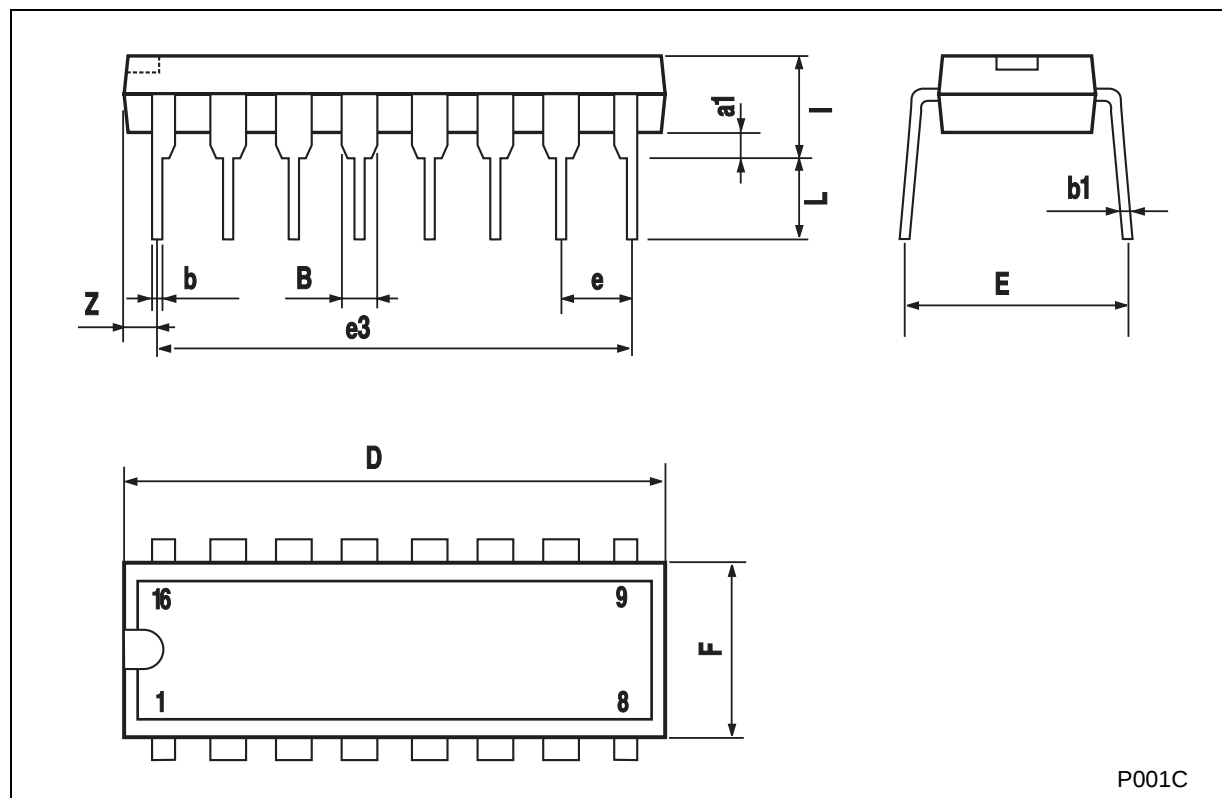


$C_L = 50\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

WAVEFORM 1: SWITCHING CHARACTERISTICS TEST WAVEFORM ($f=1\text{MHz}$; 50% duty cycle)

Plastic DIP-16 (0.25) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



SO-16 MECHANICAL DATA

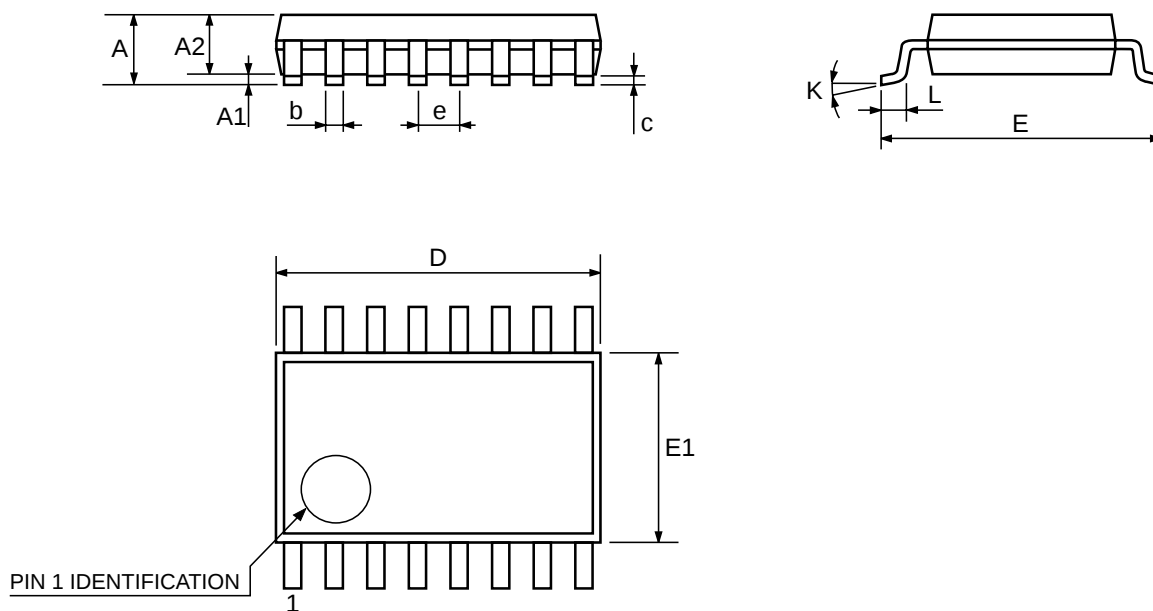
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



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