

## Features

- Very high speed: 70 ns
- Temperature ranges:
  - Industrial: -40 °C to +85 °C
- Wide voltage range: 1.65 V to 2.25 V
- Pin compatible with CY62256N
- Ultra low standby power
  - Typical standby current: 1 µA
  - Maximum standby current: 4 µA
- Ultra low active power
  - Typical active current: 1.3 mA at f = 1 MHz
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Offered in Pb-free 28-pin Narrow SOIC package

## Functional Description

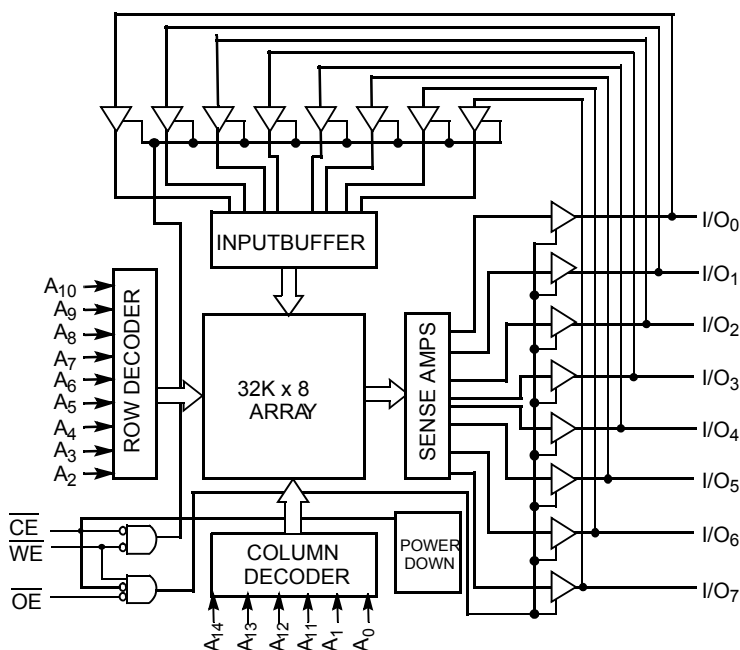
The CY62256EV18 is a high performance CMOS static RAM module organized as 32 K words by 8-bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption when addresses are not toggling. Placing the device in standby mode reduces power consumption by more than 99 percent when deselected ( $\overline{CE}$  HIGH). The eight input and output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) are placed in a high impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), or a write operation is in progress ( $\overline{CE}$  LOW and  $\overline{WE}$  LOW).

To write to the device, take chip enable ( $\overline{CE}$ ) LOW and write enable ( $\overline{WE}$ ) LOW. Data on the eight I/O pins is then written into the location specified on the address pin (A<sub>0</sub> through A<sub>14</sub>).

To read from the device, take chip enable ( $\overline{CE}$  LOW) and output enable ( $\overline{OE}$ ) LOW while forcing write enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

For a complete list of related documentation, [click here](#).

## Logic Block Diagram

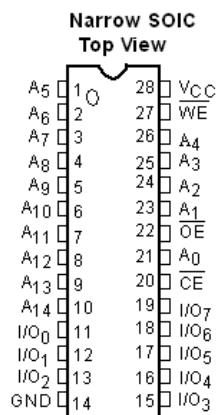


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## Pin Configuration

Figure 1. 28-pin Narrow SOIC



## Product Portfolio

Product	Range	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
						Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
		f = 1 MHz		f = f <sub>max</sub>							
Min	Typ <sup>[1]</sup>	Max		Typ <sup>[1]</sup>	Max	Typ <sup>[1]</sup>	Max	Typ <sup>[1]</sup>	Max		
CY62256EV18LL	Industrial	1.65	1.8	2.25	70	1.3	2.0	11	16	1	4

### Notes

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature with power applied ..... -55 °C to +125 °C

Supply voltage to ground potential ..... -0.2 V to 2.45 V

DC voltage applied to outputs in high Z State <sup>[2, 3]</sup> ..... -0.2 V to 2.45 V

DC input voltage <sup>[2, 3]</sup> ..... -0.2 V to 2.45 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

## Operating Range

Device	Range	Ambient Temperature	V <sub>CC</sub> <sup>[4]</sup>
CY62256EV18LL	Industrial	-40 °C to +85 °C	1.65 V to 2.25 V

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	70 ns			Unit
			Min	Typ <sup>[5]</sup>	Max	
V <sub>OH</sub>	Output HIGH voltage	I <sub>OH</sub> = -0.1 mA	1.4	—	—	V
V <sub>OL</sub>	Output LOW voltage	I <sub>OL</sub> = 0.1 mA	—	—	0.2	V
V <sub>IH</sub>	Input HIGH voltage	V <sub>CC</sub> = 1.65 V to 2.25 V	1.4	—	V <sub>CC</sub> + 0.2 V	V
V <sub>IL</sub>	Input LOW voltage	V <sub>CC</sub> = 1.65 V to 2.25 V	-0.2	—	0.4	V
I <sub>IX</sub>	Input leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	—	+1	μA
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , output disabled	-1	—	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	f = f <sub>max</sub> = 1/t <sub>RC</sub>	—	11	16	mA
		f = 1 MHz	—	1.3	2.0	
I <sub>SB1</sub>	Automatic CE power-down current — CMOS inputs	CE ≥ V <sub>CC</sub> - 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V, V <sub>IN</sub> ≤ 0.2 V f = f <sub>max</sub> (address and data only), f = 0 (OE and WE), V <sub>CC</sub> = 2.25 V	—	1	4	μA
I <sub>SB2</sub> <sup>[6]</sup>	Automatic CE power-down current — CMOS inputs	CE ≥ V <sub>CC</sub> - 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V or V <sub>IN</sub> < 0.2 V, f = 0, V <sub>CC</sub> = 2.25 V	—	1	4	μA

### Notes

2. V<sub>IL(min)</sub> = -2.0 V for pulse durations less than 20 ns.

3. V<sub>IH(max)</sub> = V<sub>CC</sub> + 0.5 V for pulse durations less than 20 ns.

4. Full device AC operation assumes a 100 μs ramp time from 0 to V<sub>CC(min)</sub> and 200 μs wait time after V<sub>CC</sub> stabilization.

5. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.

6. Chip enables (CE) must be at CMOS level to meet the I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Other inputs can be left floating.

## Capacitance

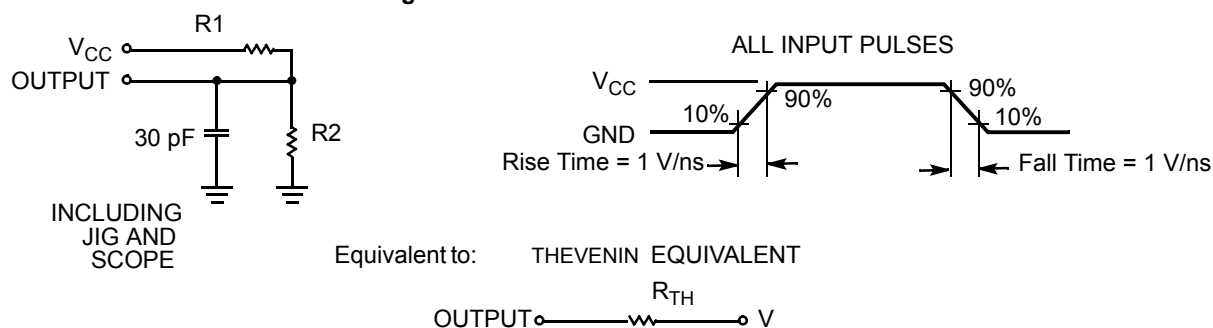
Parameter <sup>[7]</sup>	Description	Test Conditions	Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25\text{ }^{\circ}\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = V_{CC(typ)}$	10	pF
$C_{OUT}$	Output capacitance		10	pF

## Thermal Resistance

Parameter <sup>[7]</sup>	Description	Test Conditions	28-pin SOIC	Unit
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	76.56	$^{\circ}\text{C/W}$
$\Theta_{JC}$	Thermal resistance (junction to case)		36.07	$^{\circ}\text{C/W}$

## AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameters	1.8 V	Unit
R1	13500	$\Omega$
R2	10800	$\Omega$
$R_{TH}$	6000	$\Omega$
$V_{TH}$	0.8	V

### Note

7. Tested initially and after any design or process changes that may affect these parameters.

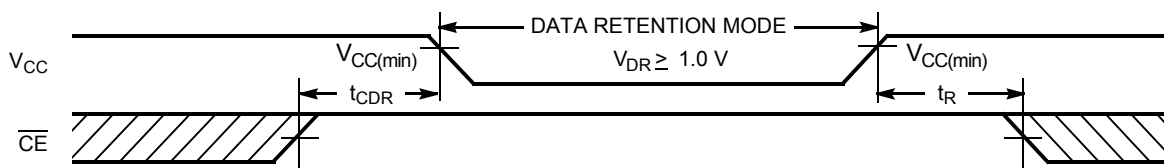
## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ <sup>[8]</sup>	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		1.0	–	–	V
$I_{CCDR}$ <sup>[9]</sup>	Data retention current	$V_{CC} = 1.0\text{ V}$ , $\overline{CE} \geq V_{CC} - 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	–	3	$\mu\text{A}$
$t_{CDR}$ <sup>[10]</sup>	Chip deselect to data retention time		0	–	–	ns
$t_R$ <sup>[11]</sup>	Operation recovery time		70	–	–	ns

## Data Retention Waveform

**Figure 3. Data Retention Waveform<sup>[12]</sup>**



### Notes

8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(yp)}$ ,  $T_A = 25\text{ }^\circ\text{C}$ .
9. Chip enables ( $\overline{CE}$ ) must be at CMOS level to meet the  $I_{SB2} / I_{CCDR}$  spec. Other inputs can be left floating.
10. Tested initially and after any design or process changes that may affect these parameters.
11. Full device AC operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$ .
12. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.

## Switching Characteristics

Over the Operating Range

Parameter <sup>[13]</sup>	Description	70 ns		Unit
		Min	Max	
Read Cycle				
t <sub>RC</sub>	Read cycle time	70	–	ns
t <sub>AA</sub>	Address to data valid	–	70	ns
t <sub>OHA</sub>	Data hold from address change	5	–	ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to data valid	–	70	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to data valid	–	35	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to low Z <sup>[14]</sup>	5	–	ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to high Z <sup>[14, 15]</sup>	–	25	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to low Z <sup>[14]</sup>	5	–	ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to high Z <sup>[14, 15]</sup>	–	25	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to power-up	0	–	ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to power-down	–	70	ns
Write Cycle <sup>[16]</sup>				
t <sub>WC</sub>	Write cycle time	70	–	ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to write end	60	–	ns
t <sub>AW</sub>	Address setup to write end	60	–	ns
t <sub>HA</sub>	Address hold from write end	0	–	ns
t <sub>SA</sub>	Address setup to write start	0	–	ns
t <sub>PWE</sub>	$\overline{WE}$ pulse width	50	–	ns
t <sub>SD</sub>	Data setup to write end	30	–	ns
t <sub>HD</sub>	Data hold from write end	0	–	ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to high Z <sup>[14, 15]</sup>	–	25	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to low Z <sup>[14]</sup>	5	–	ns

### Notes

13. Test Conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the [Figure 2 on page 5](#).

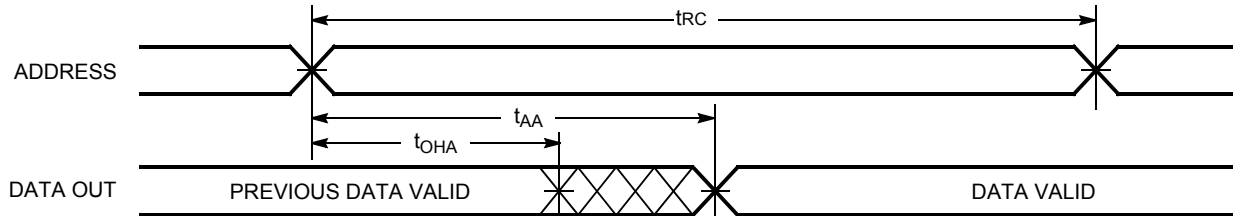
14. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.

15.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  transitions are measured when the output enter a high impedance state.

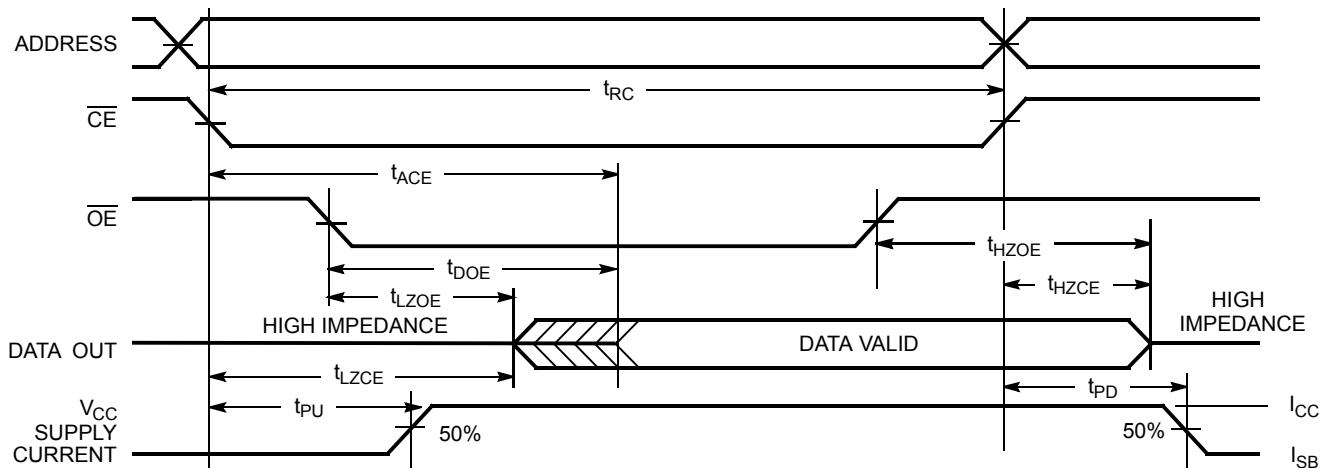
16. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

## Switching Waveforms

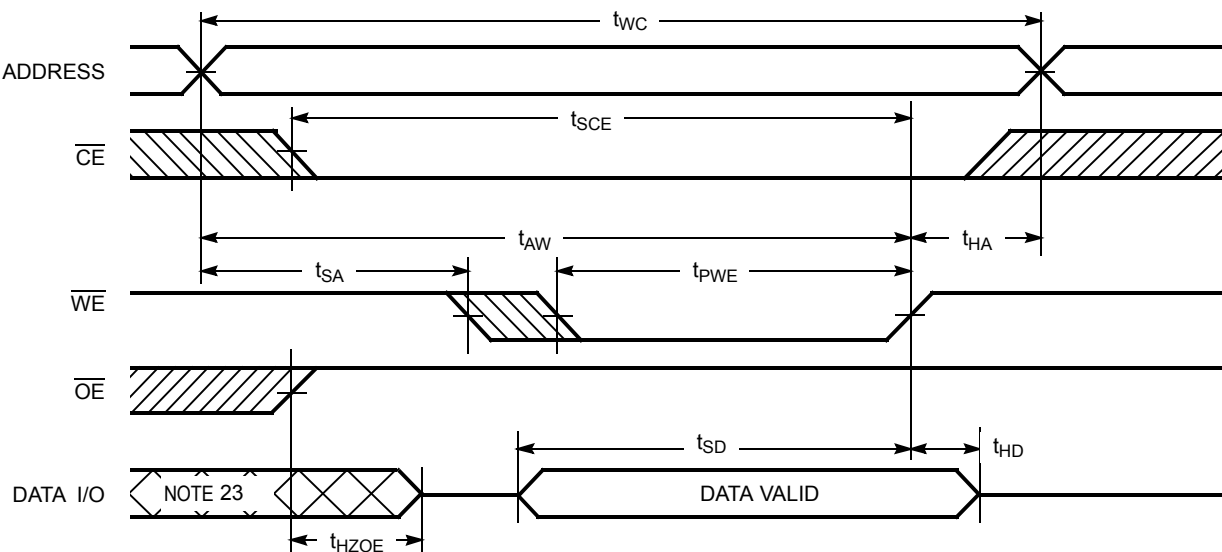
**Figure 4. Read Cycle No. 1 (Address Transition Controlled)** [17, 18]



**Figure 5. Read Cycle No. 2 (OE Controlled)** [18, 19]



**Figure 6. Write Cycle No. 1 (WE Controlled)** [20, 21, 22]



### Notes

17. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .

18. WE is HIGH for read cycle.

19. Address valid before or similar to  $\overline{CE}$  transition LOW.

20. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

21. Data I/O is high impedance if  $\overline{OE} = V_{IL}$ .

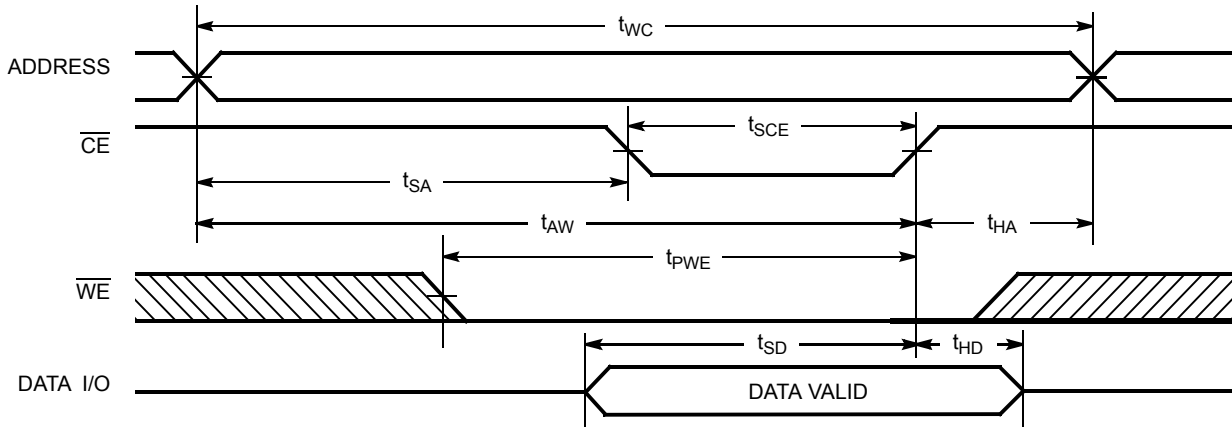
22. If  $\overline{CE}$  goes HIGH simultaneously with WE HIGH, the output remains in high impedance state.

23. During this period, the I/Os are in output state. Do not apply input signals.

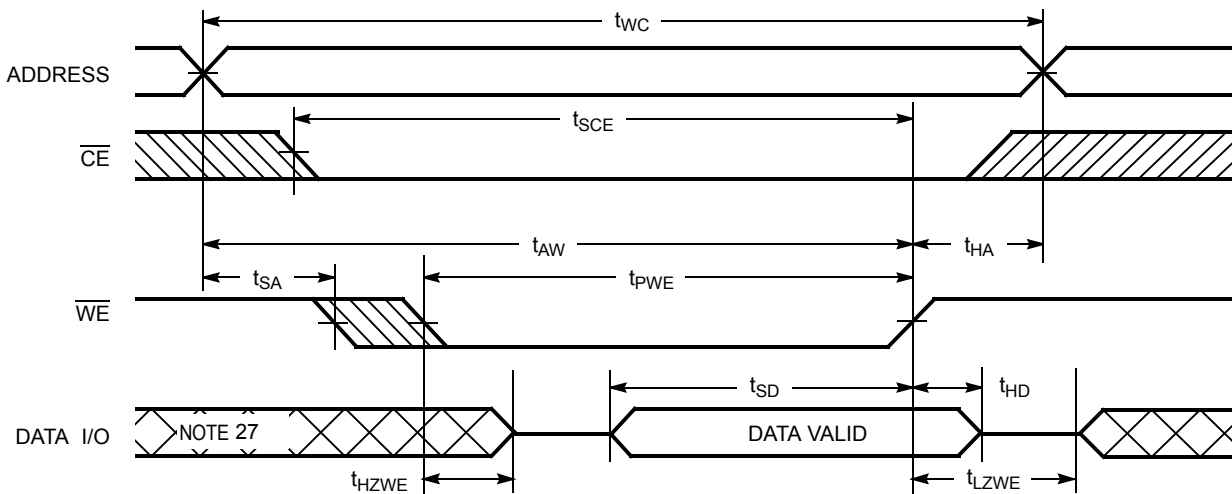


## Switching Waveforms (continued)

**Figure 7. Write Cycle No. 2 ( $\overline{\text{CE}}$  Controlled)** [24, 25, 26]



**Figure 8. Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)** [26]



### Notes

24. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}}$ ,  $\overline{\text{CE}} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

25. Data I/O is high impedance if  $\overline{\text{OE}} = V_{IH}$ .

26. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  HIGH, the output remains in high impedance state.

27. During this period, the I/Os are in output state. Do not apply input signals.

## Truth Table

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Inputs/Outputs	Mode	Power
H	X <sup>[28]</sup>	X <sup>[28]</sup>	High Z	Deselect/power-down	Standby ( $I_{\text{SB}}$ )
L	H	L	Data out	Read	Active ( $I_{\text{CC}}$ )
L	L	X <sup>[28]</sup>	Data in	Write	Active ( $I_{\text{CC}}$ )
L	H	H	High Z	Selected, outputs disabled	Active ( $I_{\text{CC}}$ )

### Note

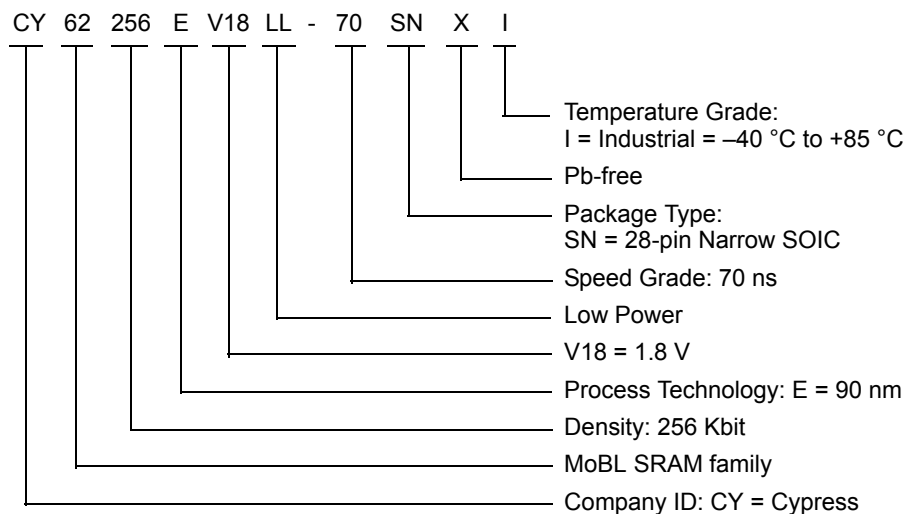
28. The 'X' (Don't care) state for the  $\overline{\text{CE}}$  /  $\overline{\text{OE}}$  /  $\overline{\text{WE}}$  in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

## Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
70	CY62256EV18LL-70SNXI	51-85092	28-pin (300-Mil) Narrow SOIC (Pb-free)	Industrial

Contact your local Cypress sales representative for availability of these parts.

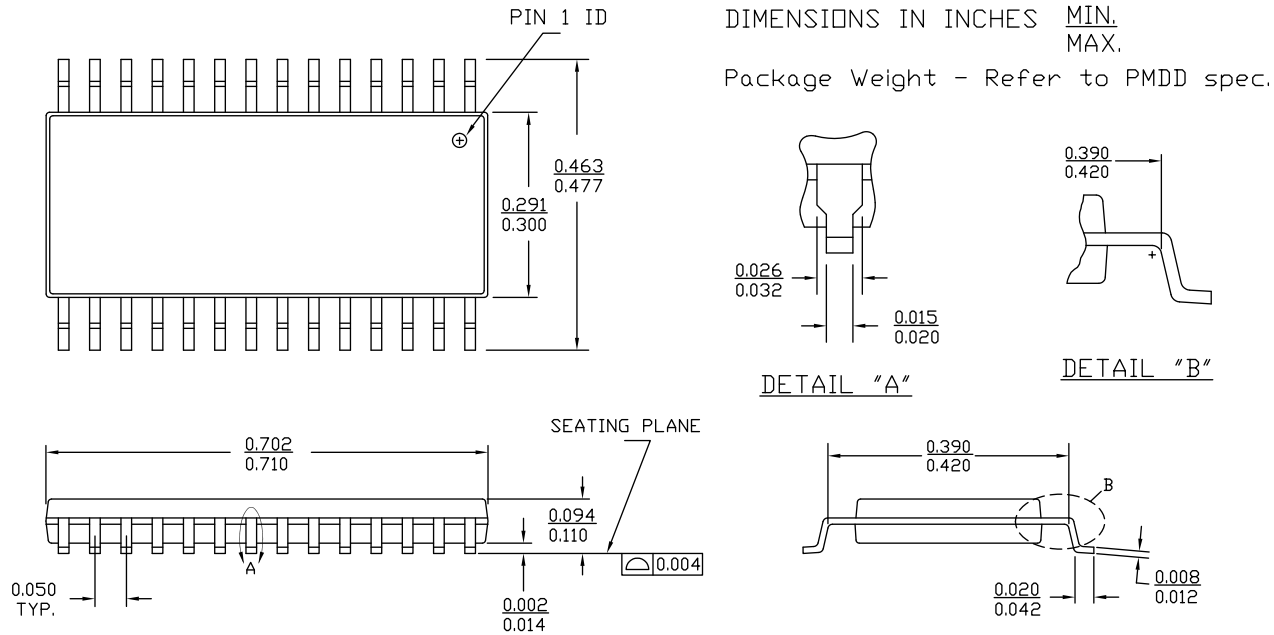
## Ordering Code Definitions



## Package Diagrams

**Figure 9. 28-pin SNC (300 Mils) SN28.3 (Narrow Body) Package Outline, 51-85092**

### SNC 28.300 WITH NARROW BODY



51-85092 \*E

## Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
$\overline{\text{CE}}$	chip enable
I/O	input/output
$\overline{\text{OE}}$	output enable
SRAM	static random access memory
SOIC	small outline integrated circuit
$\overline{\text{WE}}$	write enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY62256EV18 MoBL <sup>®</sup> , 256-Kbit (32 K × 8) Static RAM Document Number: 001-69650				
Revision	ECN	Submission Date	Orig. of Change	Description of Change
**	3334904	09/07/2011	RAME	New data sheet
*A	3413173	10/18/2011	RAME	Changed status from Preliminary to Final.
*B	3733339	09/04/2012	JISH	Fixed typo errors. Sunset review.
*C	4573121	11/18/2014	JISH	Added related documentation hyperlink in page 1.

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