

# SN54HC163, SN74HC163 4-BIT SYNCHRONOUS BINARY COUNTERS

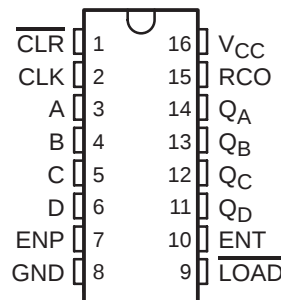
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- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 14$  ns
- $\pm 4$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable

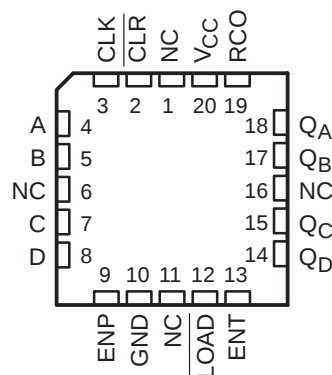
## description/ordering information

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 'HC163 devices are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes normally associated with synchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

SN54HC163 . . . J OR W PACKAGE  
SN74HC163 . . . D, DB, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54HC163 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## ORDERING INFORMATION

| T <sub>A</sub> | PACKAGE <sup>†</sup> |              | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|----------------------|--------------|-----------------------|------------------|
| –40°C to 85°C  | PDIP – N             | Tube of 25   | SN74HC163N            | SN74HC163N       |
|                | SOIC – D             | Tube of 40   | SN74HC163D            | HC163            |
|                |                      | Reel of 2500 | SN74HC163DR           |                  |
|                |                      | Reel of 250  | SN74HC163DT           |                  |
|                | SOP – NS             | Reel of 2000 | SN74HC163NSR          | HC163            |
|                | SSOP – DB            | Reel of 2000 | SN74HC163DBR          | HC163            |
| –55°C to 125°C | TSSOP – PW           | Tube of 90   | SN74HC163PW           | HC163            |
|                |                      | Reel of 2000 | SN74HC163PWR          |                  |
|                |                      | Reel of 250  | SN74HC163PWT          |                  |
|                | CDIP – J             | Tube of 25   | SNJ54HC163J           | SNJ54HC163J      |
|                | CFP – W              | Tube of 150  | SNJ54HC163W           | SNJ54HC163W      |
|                | LCCC – FK            | Tube of 55   | SNJ54HC163FK          | SNJ54HC163FK     |

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN54HC163, SN74HC163

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### description/ordering information (continued)

These counters are fully programmable; that is, they can be preset to any number between 0 and 9 or 15. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

The clear function for the 'HC163 devices is synchronous. A low level at the clear ( $\overline{\text{CLR}}$ ) input sets all four of the flip-flop outputs low after the next low-to-high transition of CLK, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to  $\overline{\text{CLR}}$  to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. ENP, ENT, and a ripple-carry output (RCO) are instrumental in accomplishing this function. Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. Enabling RCO produces a high-level pulse while the count is maximum (9 or 15 with  $Q_A$  high). This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or  $\overline{\text{LOAD}}$ ) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

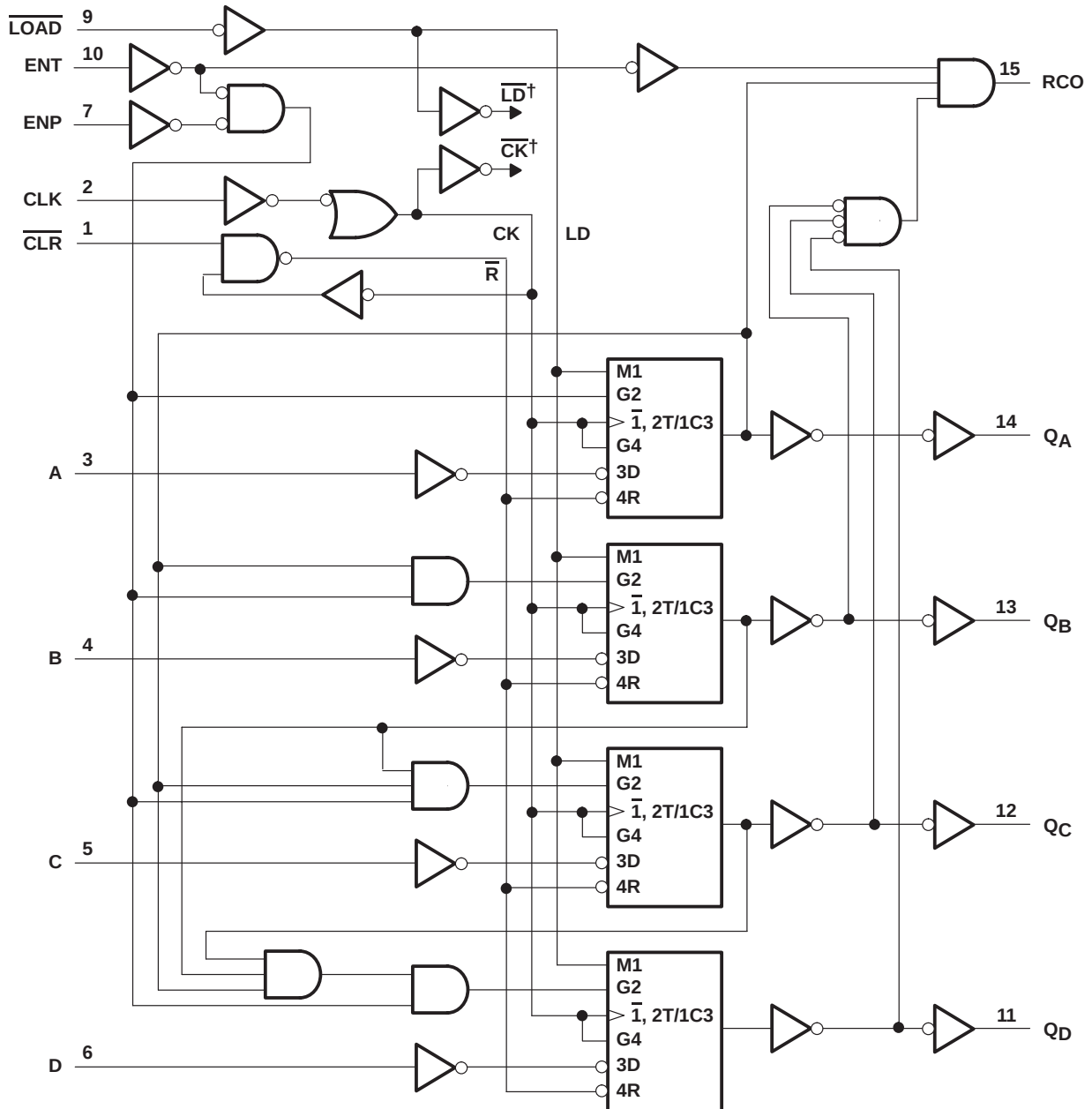


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## logic diagram (positive logic)



† For simplicity, routing of complementary signals  $\overline{LD}$  and  $\overline{CK}$  is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

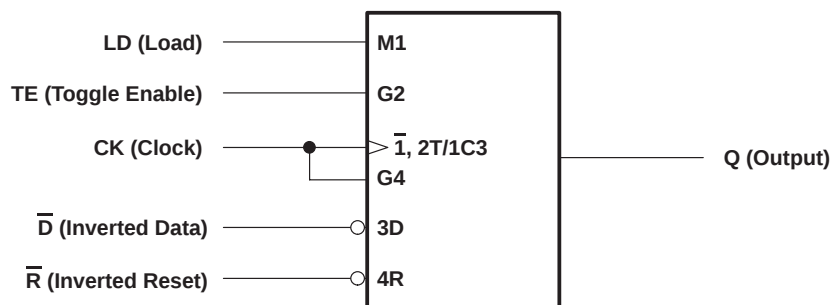
Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

# SN54HC163, SN74HC163

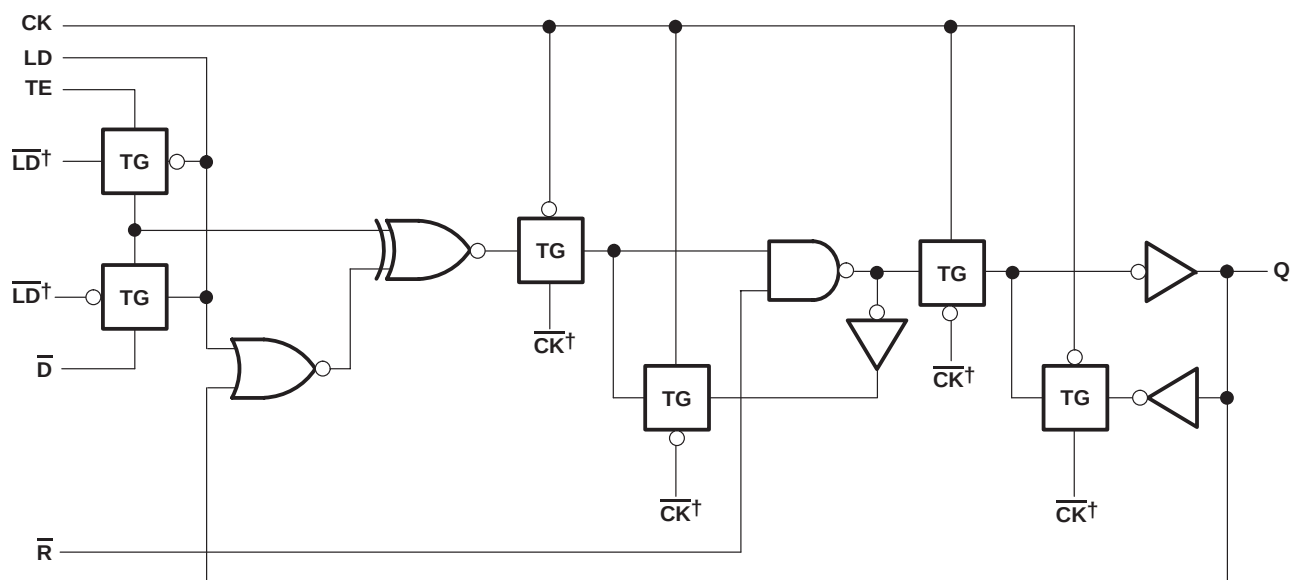
## 4-BIT SYNCHRONOUS BINARY COUNTERS

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### logic symbol, each D/T flip-flop



### logic diagram, each D/T flip-flop (positive logic)

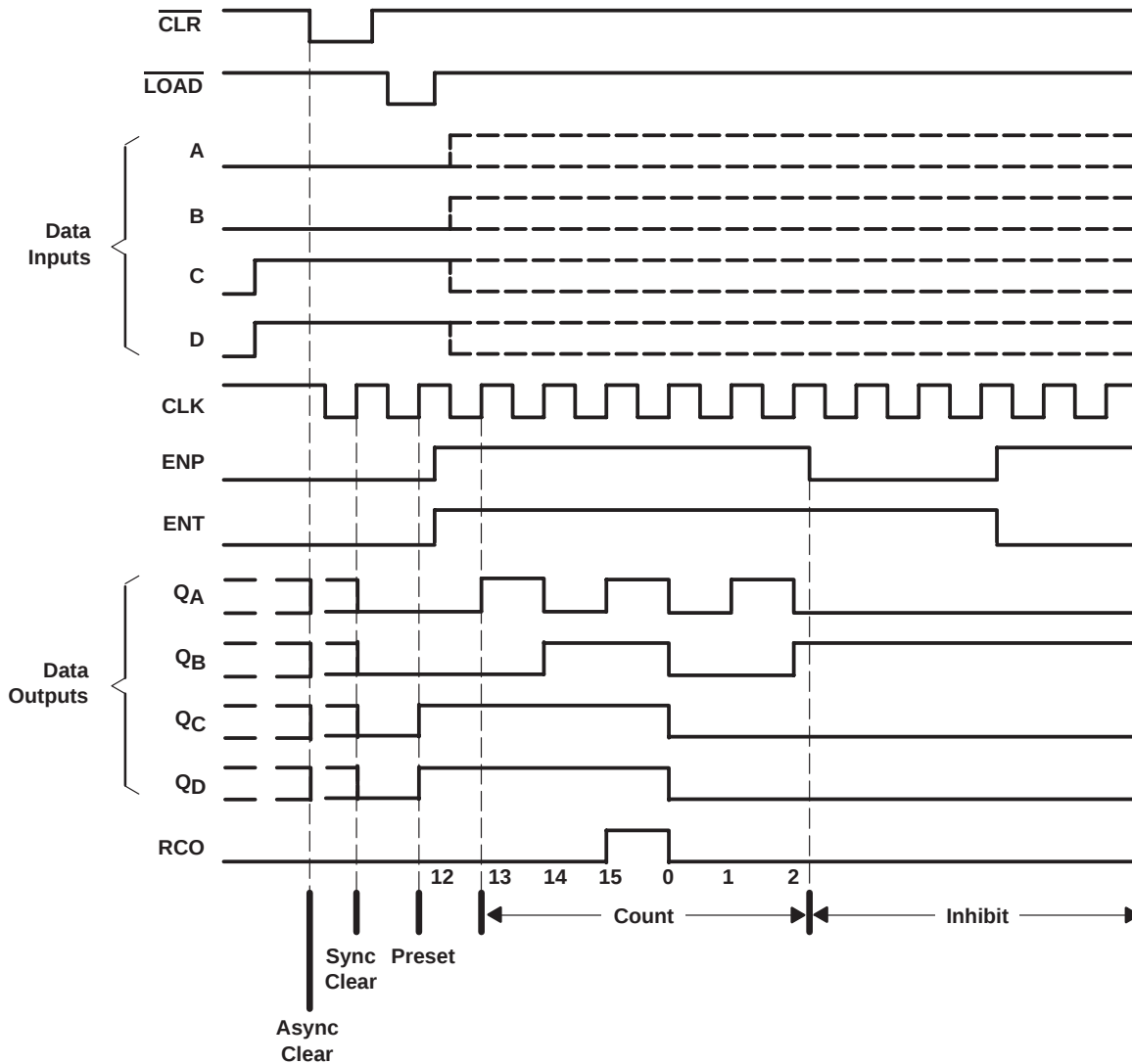


† The origins of  $\overline{LD}$  and  $\overline{CK}$  are shown in the logic diagram of the overall device.

### typical clear, preset, count, and inhibit sequence

The following sequence is illustrated below:

1. Clear outputs to zero (synchronous)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                             |                |
|-----------------------------------------------------------------------------|----------------|
| Supply voltage range, $V_{CC}$                                              | –0.5 V to 7 V  |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)  | ±20 mA         |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1) | ±20 mA         |
| Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )                  | ±25 mA         |
| Continuous current through $V_{CC}$ or GND                                  | ±50 mA         |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): D package            | 73°C/W         |
| DB package                                                                  | 82°C/W         |
| N package                                                                   | 67°C/W         |
| NS package                                                                  | 64°C/W         |
| PW package                                                                  | 108°C/W        |
| Storage temperature range, $T_{stg}$                                        | –65°C to 150°C |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 3)

|                    |                                 |                         | SN54HC163 |                 |     | SN74HC163 |                 |     | UNIT |
|--------------------|---------------------------------|-------------------------|-----------|-----------------|-----|-----------|-----------------|-----|------|
|                    |                                 |                         | MIN       | NOM             | MAX | MIN       | NOM             | MAX |      |
| V <sub>CC</sub>    | Supply voltage                  |                         | 2         | 5               | 6   | 2         | 5               | 6   | V    |
| V <sub>IH</sub>    | High-level input voltage        | V <sub>CC</sub> = 2 V   | 1.5       |                 |     | 1.5       |                 |     | V    |
|                    |                                 | V <sub>CC</sub> = 4.5 V | 3.15      |                 |     | 3.15      |                 |     |      |
|                    |                                 | V <sub>CC</sub> = 6 V   | 4.2       |                 |     | 4.2       |                 |     |      |
| V <sub>IL</sub>    | Low-level input voltage         | V <sub>CC</sub> = 2 V   | 0.5       |                 |     | 0.5       |                 |     | V    |
|                    |                                 | V <sub>CC</sub> = 4.5 V | 1.35      |                 |     | 1.35      |                 |     |      |
|                    |                                 | V <sub>CC</sub> = 6 V   | 1.8       |                 |     | 1.8       |                 |     |      |
| V <sub>I</sub>     | Input voltage                   |                         | 0         | V <sub>CC</sub> |     | 0         | V <sub>CC</sub> |     | V    |
| V <sub>O</sub>     | Output voltage                  |                         | 0         | V <sub>CC</sub> |     | 0         | V <sub>CC</sub> |     | V    |
| Δt/Δv <sup>‡</sup> | Input transition rise/fall time | V <sub>CC</sub> = 2 V   | 1000      |                 |     | 1000      |                 |     | ns   |
|                    |                                 | V <sub>CC</sub> = 4.5 V | 500       |                 |     | 500       |                 |     |      |
|                    |                                 | V <sub>CC</sub> = 6 V   | 400       |                 |     | 400       |                 |     |      |
| T <sub>A</sub>     | Operating free-air temperature  |                         | −55       | 125             |     | −40       | 85              |     | °C   |

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

<sup>‡</sup> If this device is used in the threshold region (from  $V_{ILmax} = 0.5$  V to  $V_{IHmin} = 1.5$  V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at  $t_t = 1000$  ns and  $V_{CC} = 2$  V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER       | TEST CONDITIONS                                           |                           | V <sub>CC</sub> | T <sub>A</sub> = 25°C |       |      | SN54HC163 |       | SN74HC163 |       | UNIT |
|-----------------|-----------------------------------------------------------|---------------------------|-----------------|-----------------------|-------|------|-----------|-------|-----------|-------|------|
|                 |                                                           |                           |                 | MIN                   | TYP   | MAX  | MIN       | MAX   | MIN       | MAX   |      |
| V <sub>OH</sub> | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>       | I <sub>OH</sub> = -20 µA  | 2 V             | 1.9                   | 1.998 |      | 1.9       |       | 1.9       |       | V    |
|                 |                                                           |                           | 4.5 V           | 4.4                   | 4.499 |      | 4.4       |       | 4.4       |       |      |
|                 |                                                           |                           | 6 V             | 5.9                   | 5.999 |      | 5.9       |       | 5.9       |       |      |
|                 |                                                           | I <sub>OH</sub> = -4 mA   | 4.5 V           | 3.98                  | 4.3   |      | 3.7       |       | 3.84      |       |      |
|                 |                                                           | I <sub>OH</sub> = -5.2 mA | 6 V             | 5.48                  | 5.8   |      | 5.2       |       | 5.34      |       |      |
| V <sub>OL</sub> | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>       | I <sub>OL</sub> = 20 µA   | 2 V             |                       | 0.002 | 0.1  |           | 0.1   |           | 0.1   | V    |
|                 |                                                           |                           | 4.5 V           |                       | 0.001 | 0.1  |           | 0.1   |           | 0.1   |      |
|                 |                                                           |                           | 6 V             |                       | 0.001 | 0.1  |           | 0.1   |           | 0.1   |      |
|                 |                                                           | I <sub>OL</sub> = 4 mA    | 4.5 V           |                       | 0.17  | 0.26 |           | 0.4   |           | 0.33  |      |
|                 |                                                           | I <sub>OL</sub> = 5.2 mA  | 6 V             |                       | 0.15  | 0.26 |           | 0.4   |           | 0.33  |      |
| I <sub>I</sub>  | V <sub>I</sub> = V <sub>CC</sub> or 0                     |                           | 6 V             |                       | ±0.1  | ±100 |           | ±1000 |           | ±1000 | nA   |
| I <sub>CC</sub> | V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0 |                           | 6 V             |                       |       | 8    |           | 160   |           | 80    | µA   |
| C <sub>i</sub>  |                                                           |                           | 2 V to 6 V      |                       | 3     | 10   |           | 10    |           | 10    | pF   |

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

|                    |                                              |  | V <sub>CC</sub>                  | T <sub>A</sub> = 25°C |       | SN54HC163 |     | SN74HC163 |     | UNIT |  |    |
|--------------------|----------------------------------------------|--|----------------------------------|-----------------------|-------|-----------|-----|-----------|-----|------|--|----|
|                    |                                              |  |                                  | MIN                   | MAX   | MIN       | MAX | MIN       | MAX |      |  |    |
| f <sub>clock</sub> | Clock frequency                              |  | 2 V                              | 6                     |       | 4.2       |     | 5         |     | MHz  |  |    |
|                    |                                              |  | 4.5 V                            | 31                    |       | 21        |     | 25        |     |      |  |    |
|                    |                                              |  | 6 V                              | 36                    |       | 25        |     | 29        |     |      |  |    |
| t <sub>w</sub>     | Pulse duration                               |  | CLK high or low                  |                       | 2 V   | 80        |     | 120       |     | 100  |  | ns |
|                    |                                              |  |                                  |                       | 4.5 V | 16        |     | 24        |     | 20   |  |    |
|                    |                                              |  |                                  |                       | 6 V   | 14        |     | 20        |     | 17   |  |    |
| t <sub>su</sub>    | Setup time before CLK↑                       |  | A, B, C, or D                    |                       | 2 V   | 150       |     | 225       |     | 190  |  | ns |
|                    |                                              |  |                                  |                       | 4.5 V | 30        |     | 45        |     | 38   |  |    |
|                    |                                              |  |                                  |                       | 6 V   | 26        |     | 38        |     | 32   |  |    |
|                    |                                              |  | $\overline{\text{LOAD}}$ low     |                       | 2 V   | 135       |     | 205       |     | 170  |  |    |
|                    |                                              |  |                                  |                       | 4.5 V | 27        |     | 41        |     | 34   |  |    |
|                    |                                              |  |                                  |                       | 6 V   | 23        |     | 35        |     | 29   |  |    |
|                    |                                              |  | ENP, ENT                         |                       | 2 V   | 170       |     | 255       |     | 215  |  |    |
|                    |                                              |  |                                  |                       | 4.5 V | 34        |     | 51        |     | 43   |  |    |
|                    |                                              |  |                                  |                       | 6 V   | 29        |     | 43        |     | 37   |  |    |
|                    |                                              |  | $\overline{\text{CLR}}$ low      |                       | 2 V   | 160       |     | 240       |     | 200  |  |    |
|                    |                                              |  |                                  |                       | 4.5 V | 32        |     | 48        |     | 40   |  |    |
|                    |                                              |  |                                  |                       | 6 V   | 27        |     | 41        |     | 34   |  |    |
|                    |                                              |  | $\overline{\text{CLR}}$ inactive |                       | 2 V   | 160       |     | 240       |     | 200  |  |    |
|                    |                                              |  |                                  |                       | 4.5 V | 32        |     | 48        |     | 40   |  |    |
|                    |                                              |  |                                  |                       | 6 V   | 27        |     | 41        |     | 34   |  |    |
| t <sub>h</sub>     | Hold time, all synchronous inputs after CLK↑ |  | 2 V                              | 0                     |       | 0         |     | 0         |     | ns   |  |    |
|                    |                                              |  | 4.5 V                            | 0                     |       | 0         |     | 0         |     |      |  |    |
|                    |                                              |  | 6 V                              | 0                     |       | 0         |     | 0         |     |      |  |    |



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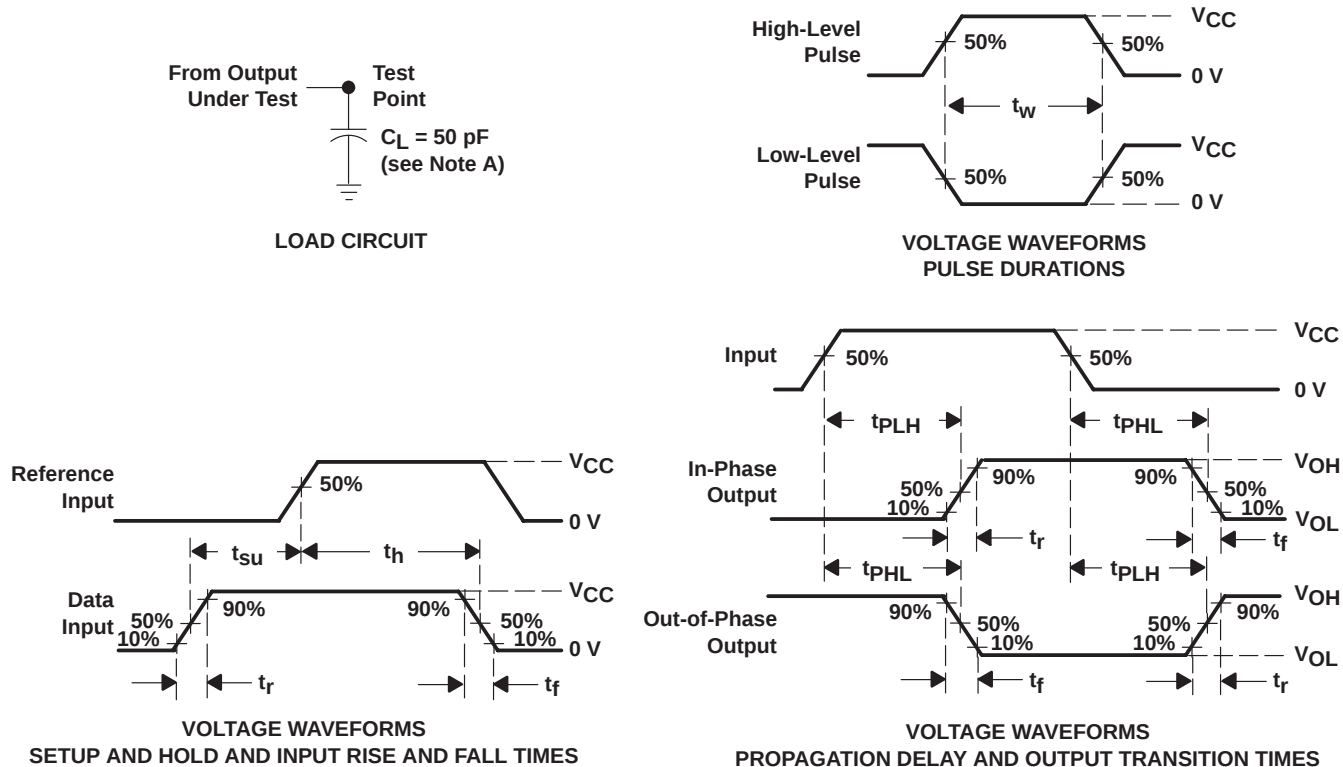
switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

| PARAMETER  | FROM<br>(INPUT) | TO<br>(OUTPUT) | $V_{CC}$ | $T_A = 25^\circ\text{C}$ |     |     | SN54HC163 |     | SN74HC163 |     | UNIT |
|------------|-----------------|----------------|----------|--------------------------|-----|-----|-----------|-----|-----------|-----|------|
|            |                 |                |          | MIN                      | TYP | MAX | MIN       | MAX | MIN       | MAX |      |
| $f_{\max}$ |                 |                | 2 V      | 6                        | 14  |     | 4.2       |     | 5         |     | MHz  |
|            |                 |                | 4.5 V    | 31                       | 40  |     | 21        |     | 25        |     |      |
|            |                 |                | 6 V      | 36                       | 44  |     | 25        |     | 29        |     |      |
| $t_{pd}$   | CLK             | RCO            | 2 V      |                          | 83  | 215 |           | 325 |           | 270 | ns   |
|            |                 |                | 4.5 V    |                          | 24  | 43  |           | 65  |           | 54  |      |
|            |                 |                | 6 V      |                          | 20  | 37  |           | 55  |           | 46  |      |
|            |                 | Any Q          | 2 V      |                          | 80  | 205 |           | 310 |           | 255 |      |
|            |                 |                | 4.5 V    |                          | 25  | 41  |           | 62  |           | 51  |      |
|            |                 |                | 6 V      |                          | 21  | 35  |           | 53  |           | 43  |      |
|            | ENT             | RCO            | 2 V      |                          | 62  | 195 |           | 295 |           | 245 |      |
|            |                 |                | 4.5 V    |                          | 17  | 39  |           | 59  |           | 49  |      |
|            |                 |                | 6 V      |                          | 14  | 33  |           | 50  |           | 42  |      |
| $t_t$      |                 | Any            | 2 V      |                          | 38  | 75  |           | 110 |           | 95  | ns   |
|            |                 |                | 4.5 V    |                          | 8   | 15  |           | 22  |           | 19  |      |
|            |                 |                | 6 V      |                          | 6   | 13  |           | 19  |           | 16  |      |

operating characteristics,  $T_A = 25^\circ\text{C}$

| PARAMETER |                               | TEST CONDITIONS | TYP | UNIT |
|-----------|-------------------------------|-----------------|-----|------|
| $C_{pd}$  | Power dissipation capacitance | No load         | 60  | pF   |

## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
  - C. For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

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### APPLICATION INFORMATION

#### n-bit synchronous counters

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 'HC163 devices count in binary. Virtually any count mode (modulo-N,  $N_1$ -to- $N_2$ ,  $N_1$ -to-maximum) can be used with this fast look-ahead circuit.

The application circuit shown in Figure 2 is not valid for clock frequencies above 18 MHz (at 25°C and 4.5-V  $V_{CC}$ ). The reason for this is that there is a glitch that is produced on the second stage's RCO and every succeeding stage's RCO. This glitch is common to all HC vendors that Texas Instruments has evaluated, in addition to the bipolar equivalents (LS, ALS, AS).



APPLICATION INFORMATION

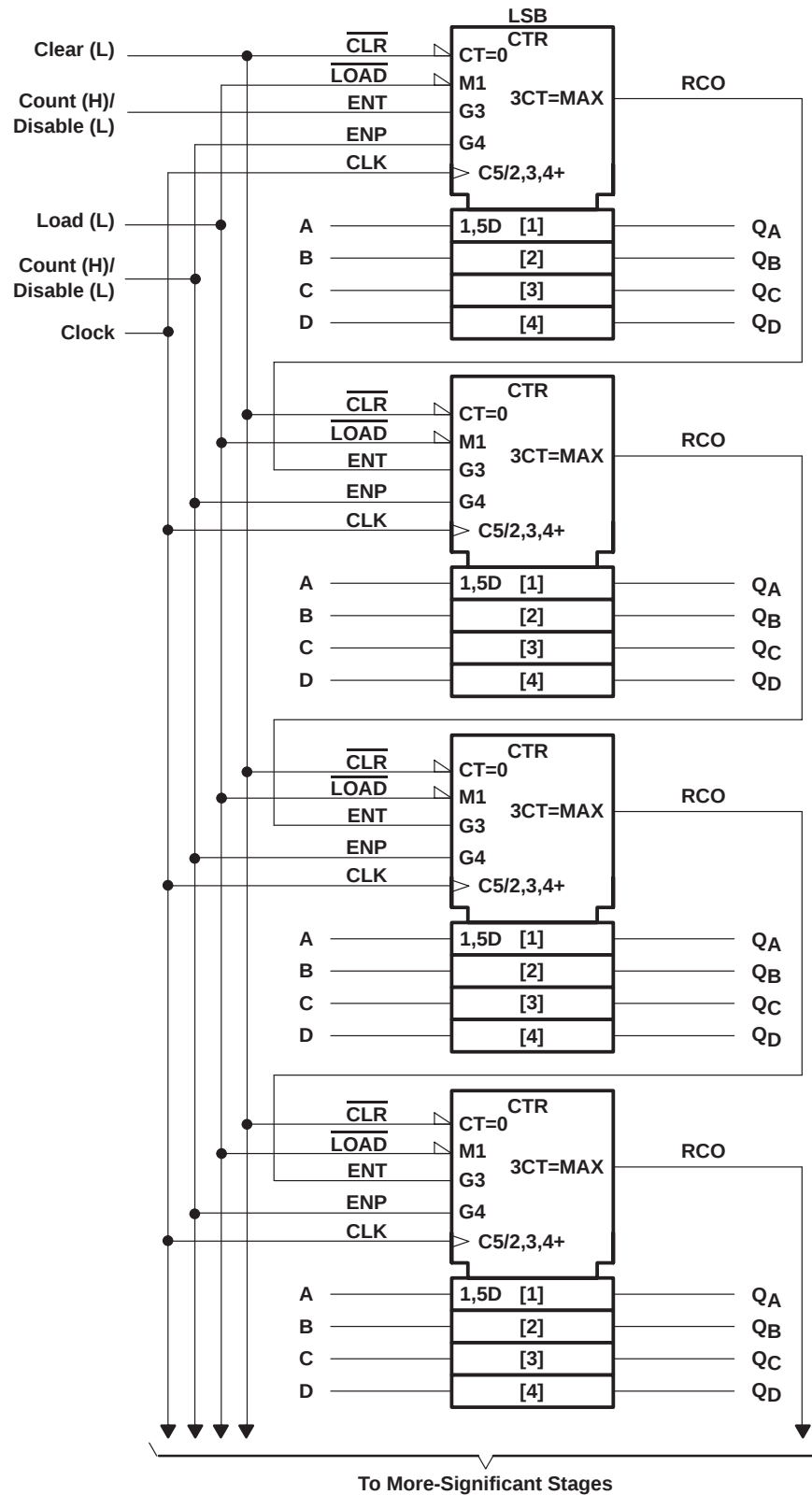


Figure 2

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### APPLICATION INFORMATION

#### n-bit synchronous counters (continued)

The glitch on RCO is caused because the propagation delay of the rising edge of  $Q_A$  of the second stage is shorter than the propagation delay of the falling edge of ENT. RCO is the product of ENT,  $Q_A$ ,  $Q_B$ ,  $Q_C$ , and  $Q_D$  ( $ENT \times Q_A \times Q_B \times Q_C \times Q_D$ ). The resulting glitch is about 7–12 ns in duration. Figure 3 shows the condition in which the glitch occurs. For simplicity, only two stages are being considered, but the results can be applied to other stages.  $Q_B$ ,  $Q_C$ , and  $Q_D$  of the first and second stage are at logic one, and  $Q_A$  of both stages are at logic zero (1110 1110) after the first clock pulse. On the rising edge of the second clock pulse,  $Q_A$  and RCO of the first stage go high. On the rising edge of the third clock pulse,  $Q_A$  and RCO of the first stage return to a low level, and  $Q_A$  of the second stage goes to a high level. At this time, the glitch on RCO of the second stage appears because of the race condition inside the chip.

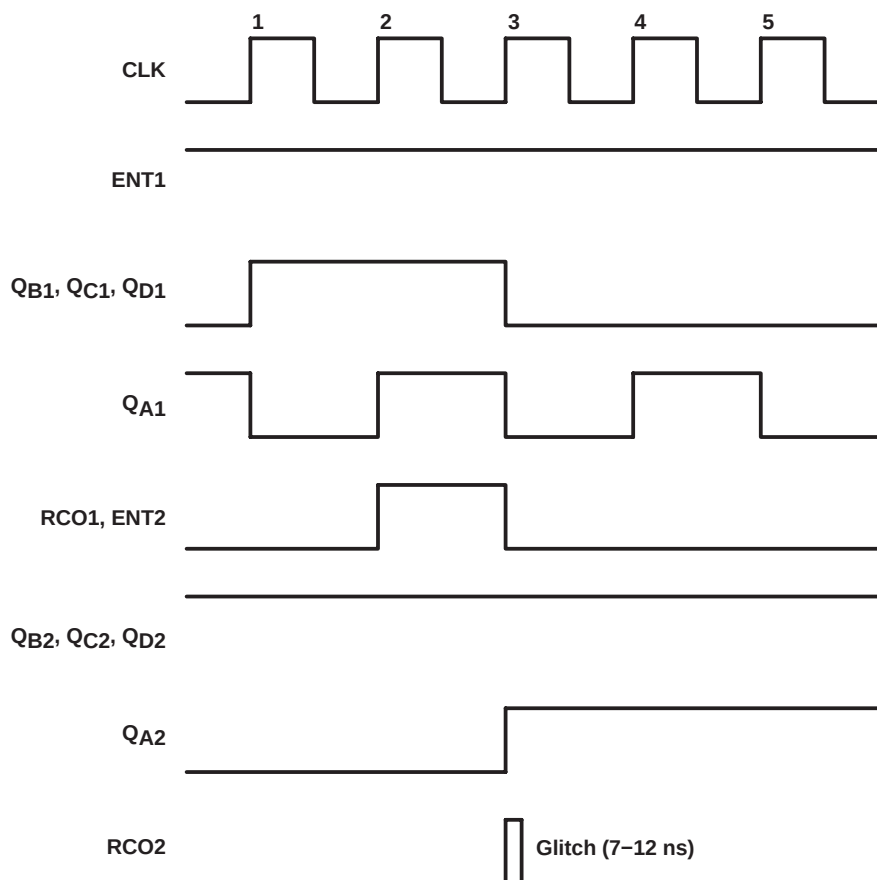


Figure 3

The glitch causes a problem in the next stage (stage three) if the glitch is still present when the next rising clock edge appears (clock pulse 4). To ensure that this does not happen, the clock frequency must be less than the inverse of the sum of the clock-to-RCO propagation delay and the glitch duration ( $t_g$ ). In other words,  $f_{max} = 1/(t_{pd} \text{ CLK-to-RCO} + t_g)$ . For example, at 25°C at 4.5-V  $V_{CC}$ , the clock-to-RCO propagation delay is 43 ns and the maximum duration of the glitch is 12 ns. Therefore, the maximum clock frequency that the cascaded counters can use is 18 MHz. The following tables contain the  $f_{clock}$ ,  $t_w$ , and  $f_{max}$  specifications for applications that use more than two 'HC163 devices cascaded together.

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## APPLICATION INFORMATION

### n-bit synchronous counters (continued)

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

|                    |                                 | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     | SN54HC163 |     | SN74HC163 |     | UNIT |
|--------------------|---------------------------------|-----------------|-----------------------|-----|-----------|-----|-----------|-----|------|
|                    |                                 |                 | MIN                   | MAX | MIN       | MAX | MIN       | MAX |      |
| f <sub>clock</sub> | Clock frequency                 | 2 V             | 3.6                   |     | 2.5       |     | 2.9       |     | MHz  |
|                    |                                 | 4.5 V           | 18                    |     | 12        |     | 14        |     |      |
|                    |                                 | 6 V             | 21                    |     | 14        |     | 17        |     |      |
| t <sub>w</sub>     | Pulse duration, CLK high or low | 2 V             | 140                   |     | 200       |     | 170       |     | ns   |
|                    |                                 | 4.5 V           | 28                    |     | 40        |     | 36        |     |      |
|                    |                                 | 6 V             | 24                    |     | 36        |     | 30        |     |      |

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Note 4)

| PARAMETER        | FROM<br>(INPUT) | TO<br>(OUTPUT) | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     | SN54HC163 |     | SN74HC163 |     | UNIT |
|------------------|-----------------|----------------|-----------------|-----------------------|-----|-----------|-----|-----------|-----|------|
|                  |                 |                |                 | MIN                   | MAX | MIN       | MAX | MIN       | MAX |      |
| f <sub>max</sub> |                 |                | 2 V             | 3.6                   |     | 2.5       |     | 2.9       |     | MHz  |
|                  |                 |                | 4.5 V           | 18                    |     | 12        |     | 14        |     |      |
|                  |                 |                | 6 V             | 21                    |     | 14        |     | 17        |     |      |

NOTE 4: These limits apply only to applications that use more than two 'HC163 devices cascaded together.

If the 'HC163 devices are used as a single unit, or only two cascaded together, then the maximum clock frequency that the devices can use is not limited because of the glitch. In these situations, the devices can be operated at the maximum specifications.

A glitch can appear on RCO of a single 'HC163 device, depending on the relationship of ENT to CLK. Any application that uses RCO to drive any input, except an ENT of another cascaded 'HC163 device, must take this into consideration.



**PACKAGING INFORMATION**

| Orderable part number            | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)           |
|----------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|-------------------------------|
| <a href="#">86076012A</a>        | Active        | Production           | LCCC (FK)   20  | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 86076012A<br>SNJ54HC<br>163FK |
| <a href="#">8607601EA</a>        | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8607601EA<br>SNJ54HC163J      |
| <a href="#">JM38510/66304BEA</a> | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | JM38510/<br>66304BEA          |
| JM38510/66304BEA.A               | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | JM38510/<br>66304BEA          |
| <a href="#">M38510/66304BEA</a>  | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | JM38510/<br>66304BEA          |
| <a href="#">SN54HC163J</a>       | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | SN54HC163J                    |
| SN54HC163J.A                     | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | SN54HC163J                    |
| <a href="#">SN74HC163D</a>       | Obsolete      | Production           | SOIC (D)   16   | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | HC163                         |
| <a href="#">SN74HC163DR</a>      | Active        | Production           | SOIC (D)   16   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HC163                         |
| SN74HC163DR.A                    | Active        | Production           | SOIC (D)   16   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HC163                         |
| SN74HC163DRE4                    | Active        | Production           | SOIC (D)   16   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HC163                         |
| <a href="#">SN74HC163DT</a>      | Obsolete      | Production           | SOIC (D)   16   | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | HC163                         |
| <a href="#">SN74HC163N</a>       | Active        | Production           | PDIP (N)   16   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | SN74HC163N                    |
| SN74HC163N.A                     | Active        | Production           | PDIP (N)   16   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | SN74HC163N                    |
| SN74HC163NE4                     | Active        | Production           | PDIP (N)   16   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | SN74HC163N                    |
| <a href="#">SN74HC163NSR</a>     | Active        | Production           | SOP (NS)   16   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HC163                         |
| SN74HC163NSR.A                   | Active        | Production           | SOP (NS)   16   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HC163                         |
| <a href="#">SN74HC163PW</a>      | Obsolete      | Production           | TSSOP (PW)   16 | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | HC163                         |
| <a href="#">SN74HC163PWR</a>     | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HC163                         |
| SN74HC163PWR.A                   | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HC163                         |
| <a href="#">SN74HC163PWT</a>     | Obsolete      | Production           | TSSOP (PW)   16 | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | HC163                         |
| <a href="#">SNJ54HC163FK</a>     | Active        | Production           | LCCC (FK)   20  | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 86076012A<br>SNJ54HC<br>163FK |

| Orderable part number       | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)           |
|-----------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|-------------------------------|
| SNJ54HC163FK.A              | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 86076012A<br>SNJ54HC<br>163FK |
| <a href="#">SNJ54HC163J</a> | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8607601EA<br>SNJ54HC163J      |
| SNJ54HC163J.A               | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8607601EA<br>SNJ54HC163J      |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN54HC163, SN74HC163 :**

- Catalog : [SN74HC163](#)
- Automotive : [SN74HC163-Q1](#), [SN74HC163-Q1](#)
- Military : [SN54HC163](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HC163DR  | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| SN74HC163NSR | SOP          | NS              | 16   | 2000 | 330.0              | 16.4               | 8.45    | 10.55   | 2.5     | 12.0    | 16.2   | Q1            |
| SN74HC163PWR | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

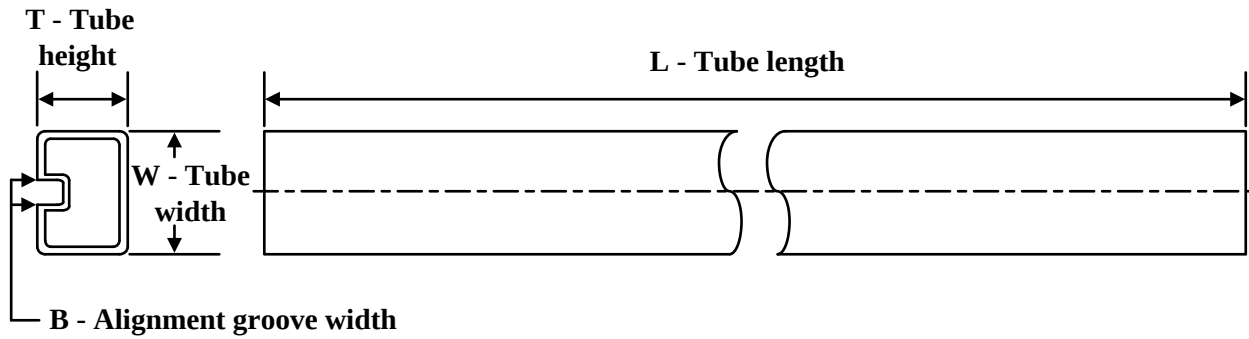
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HC163DR  | SOIC         | D               | 16   | 2500 | 353.0       | 353.0      | 32.0        |
| SN74HC163NSR | SOP          | NS              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74HC163PWR | TSSOP        | PW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |

## TUBE



\*All dimensions are nominal

| Device         | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 86076012A      | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| SN74HC163N     | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74HC163N     | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74HC163N.A   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74HC163N.A   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74HC163NE4   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74HC163NE4   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SNJ54HC163FK   | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| SNJ54HC163FK.A | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |



# PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE

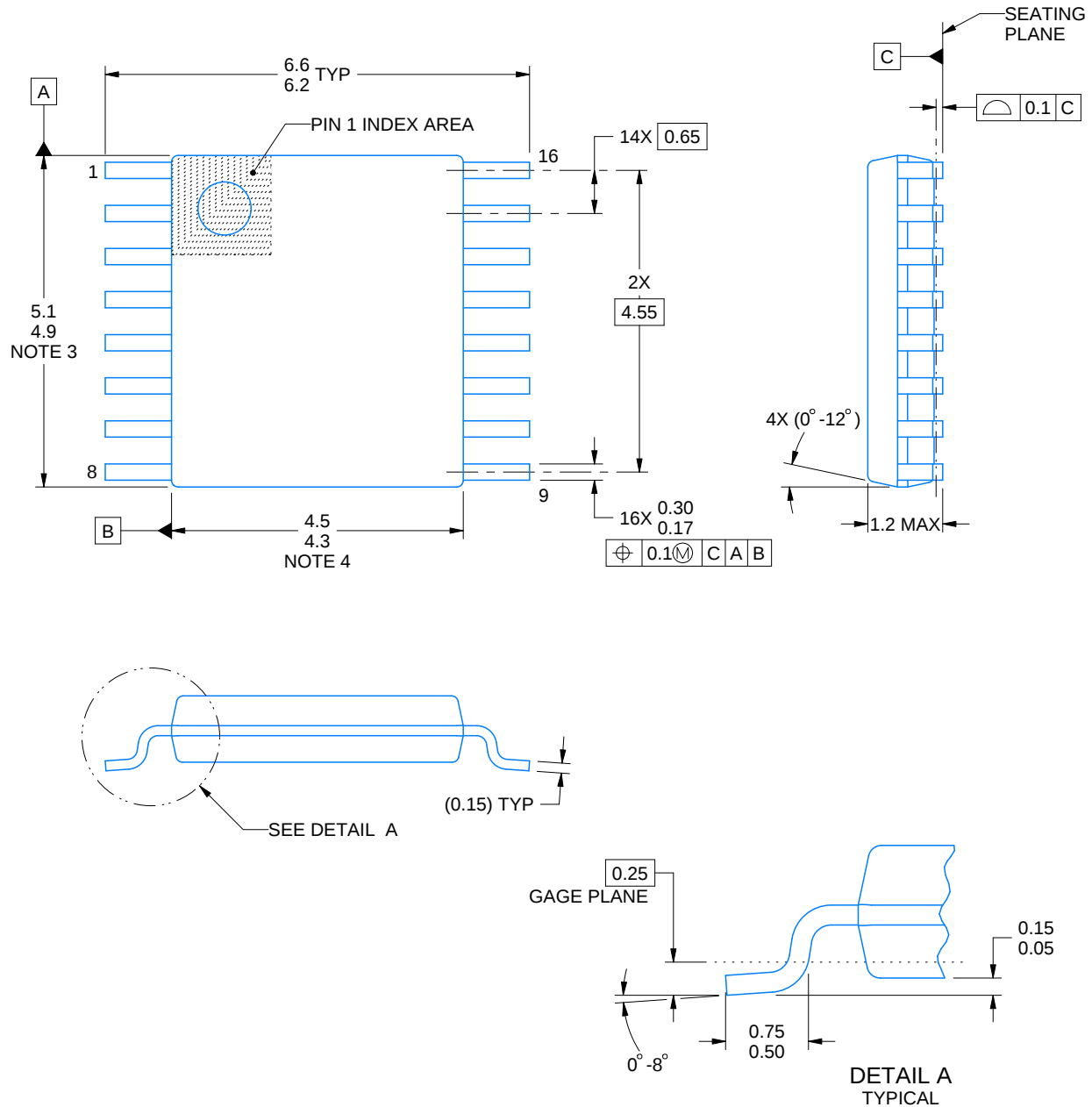


| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



4220204/B 12/2023

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

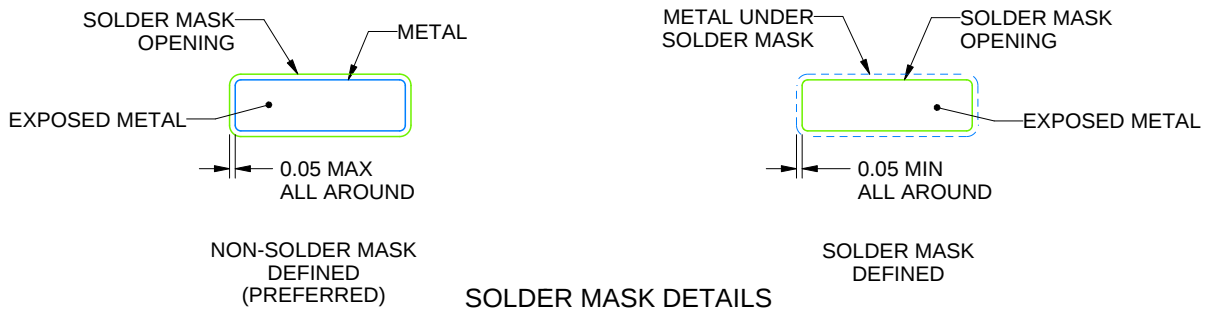
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

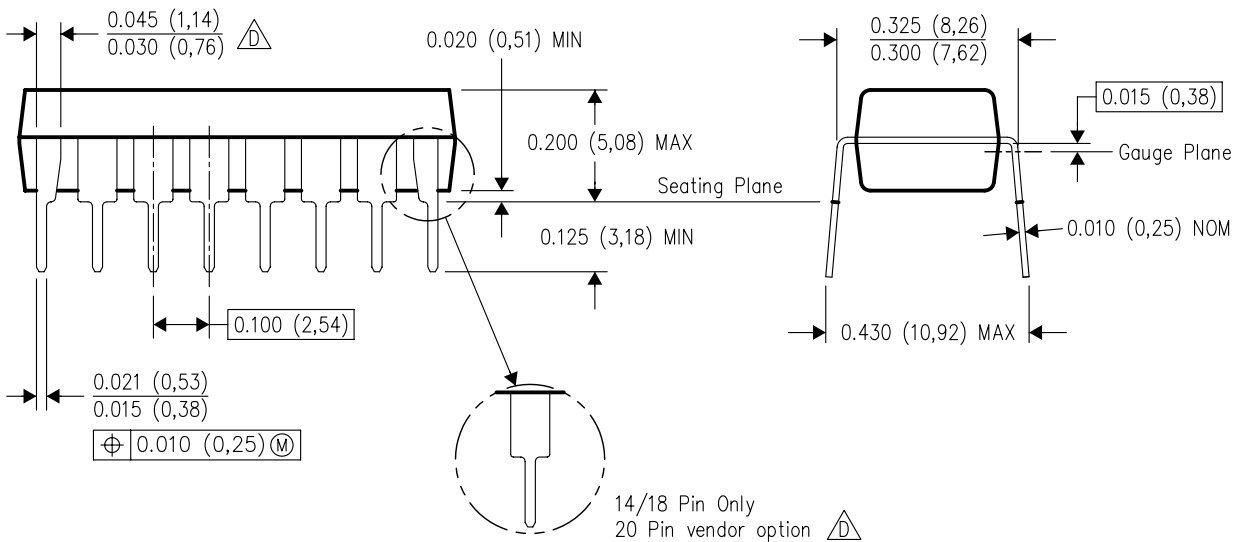
## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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