MN6761S

External Synchronization Control LSI for Color Video Cameras

■ Overview

The MN6761S is an external synchronization control LSI for color video cameras.

When used in combination with a synchronizing signal generator (MN67601NS or MN67602PS), it provides external synchronization control for NTSC and PAL video systems.
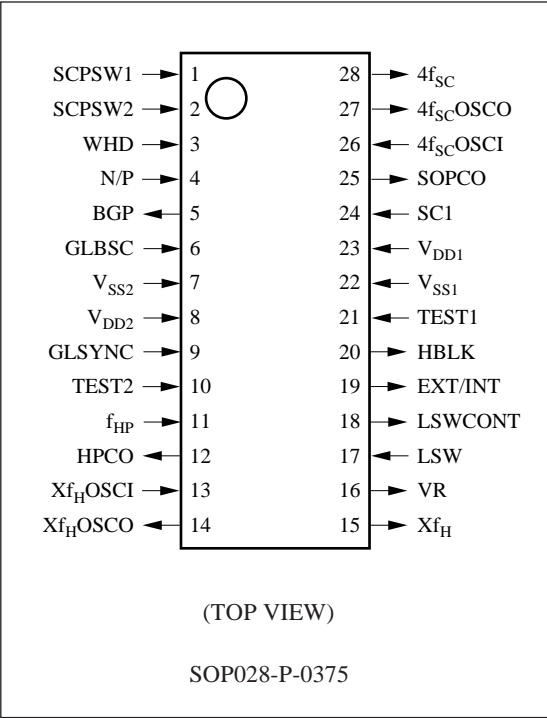
■ Features

- Synchronization of both the video camera and the VCR
- External synchronization inputs:

  Composite synchronizing signal and burst subcarrier

- External synchronization techniques
  - Horizontal synchronization: phase-locked loop
  - Vertical synchronization: reset technique
  - Subcarrier synchronization: phase-locked loop
- Support for both NTSC and PAL systems
- Built-in feature for automatically switching between external and internal synchronization
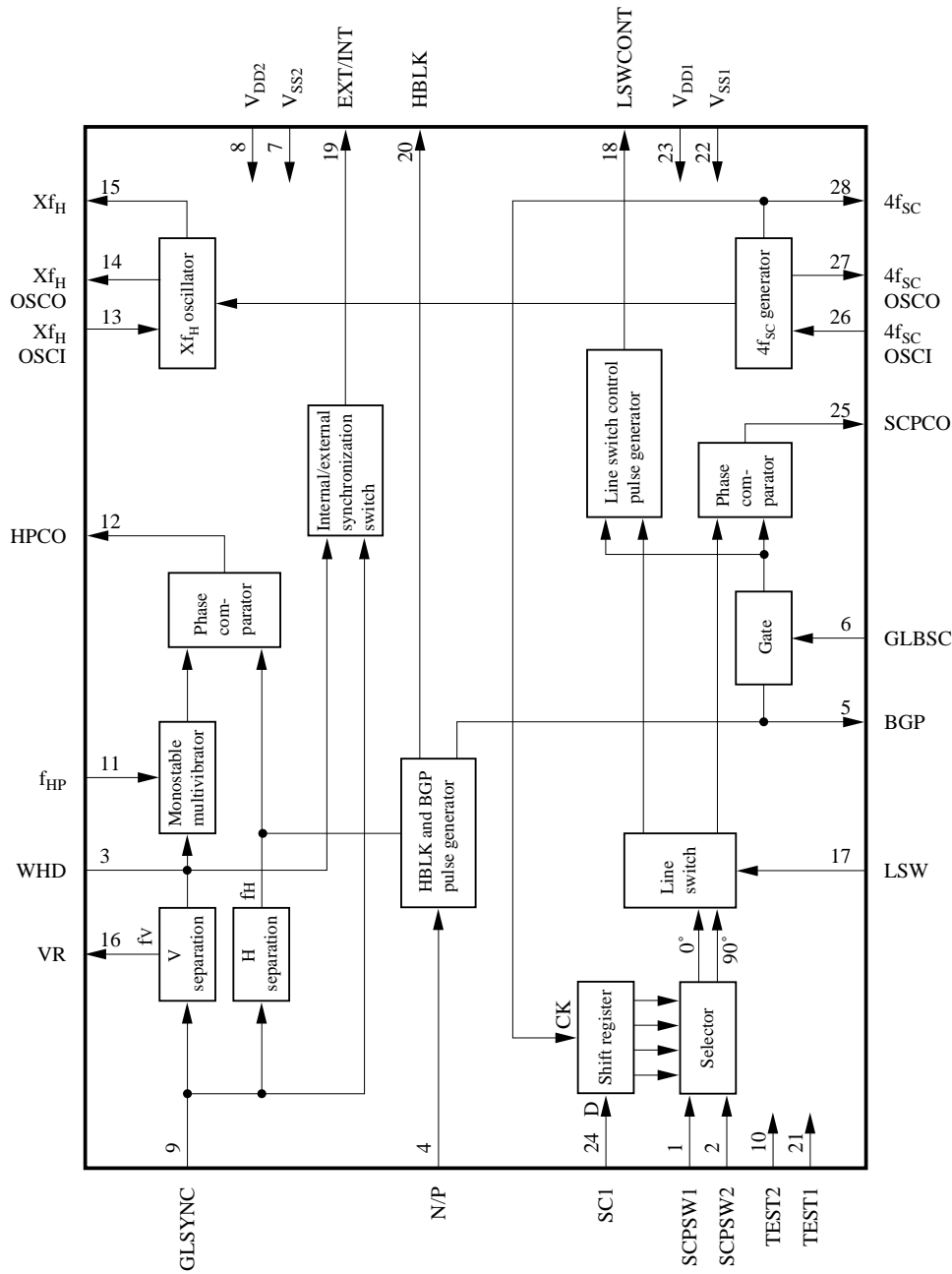- Built-in horizontal phase adjustment circuit

■ Applications

- Color video cameras

■ Pin Assignment

SCPSW1 →	1	28 → $4f_{SC}$
SCPSW2 →	2	27 → $4f_{SC}$OSCO
WHD →	3	26 ← $4f_{SC}$OSCI
N/P →	4	25 → SOPCO
BGP ←	5	24 ← SC1
GLBSC →	6	23 ← V_{DD1}
V_{SS2} →	7	22 ← V_{SS1}
V_{DD2} →	8	21 ← TEST1
GLSYNC →	9	20 → HBLK
TEST2 →	10	19 → EXT/INT
f_{HP} →	11	18 → LSWCONT
HPCO ←	12	17 ← LSW
Xf_HOSCI →	13	16 → VR
Xf_HOSCO ←	14	15 → Xf_H

(TOP VIEW)

SOP028-P-0375

■ Block Diagram

VDD2   VSS2   EXT/INT   HBLK   LSWCONT   VDD1   VSS1

8   7   19   20   18   23   22

XfH   15

28   4fSC

XfH oscillator

XfH OSCO   14

27   4fSC OSCO

XfH OSCI   13

4fSC generator

26   4fSC OSCI

Internal/external synchronization switch

Line switch control pulse generator

25   SCPCO

HPCO   12

Phase com-parator

Phase com-parator

Gate

6   GLBSC

5   BGP

fHP   11

Monostable multivibrator

HBLK and BGP pulse generator

WHD   3

fH

Line switch

17   LSW

VR   16

fV

V separation

H separation

0°   90°

CK

Shift register

Selector

9   4   24 D   1   2   10   21

GLSYNC   N/P   SC1   SCPSW1   SCPSW2   TEST2   TEST1

■ Pin Descriptions

| Pin No.	Symbol	Pin Name	Function Description
23	V_{DD1}	Power supply	"H" level (5V) power supply for subcarrier circuits
22	V_{SS1}	Power supply	"L" level (GND) power supply for subcarrier circuits
8	V_{DD2}	Power supply	"H" level (5V) power supply for synchronizing signal circuits
7	V_{SS2}	Power supply	"L" level (GND) power supply for synchronizing signal circuits
9	GLSYNC	External synchronizing signal input	Input pin for composite synchronizing signal derived from video signal (reference for horizontal and vertical signals)
6	CLBSC	External burst subcarrier input	Input pin for burst subcarrier signal derived from video signal (reference for subcarrier signals)
3	WHD	Horizontal synchroni-zation input	Input pin for WHD signal from synchronizing signal generator
11	f_{HP}	Monostable multi-vibrator input	Pin for connecting CR circuit for adjusting delay for analog monostable multivibrator (thus adjusting horizontal phase)
24	SC1	Subcarrier input	Input pin for SC1 signal from synchronizing signal generator
1 2	SCPSW1 SCPSW2	Subcarrier phase switch inputs	Pin selecting which of the four phase signals generated from the SC1 signal goes to the phase comparator
17	LSW	Line switch input	For a PAL system, supply the LSW signal from the synchronizing signal generator. For an NTSC system, keep this pin at "H" level.
4	N/P	NTSC/PAL selection input	"H" level selects NTSC operation; "L" level, PAL operation.
12	HPCO	Horizontal phase comparator output	This pin is at "L" level when the WHD signal, after passing through the monostable multivibrator, leads the rising edge of the HSYNC signal derived by separating off the horizontal component of the GLSYNC signal and is at "H" level when the signal lags. At all other times, it is in the high-impedance state.
13	$Xf_H OSCI$	Oscillator input for the synchronization circuits	Clock oscillator pins for the synchronization circuits. Connect these pins to an inductor, capacitor, and variable capacitor. (The pins have built-in feedback resistors.)
14	$Xf_H OSCO$	Oscillator output for the synchronization circuits	The circuit oscillates during external synchronization mode. The oscillation stops for internal synchronization mode. The oscillator frequency, Xf_H is 14.31818 MHz ($910f_H$) for NTSC and 4.406 MHz ($282f_H$) for PAL.
15	Xf_H	Clock output for synchronizing signal circuits	Clock output pin for synchronizing signal circuits. This pin provides the clock (Xf_H) for the external synchronization mode and stays at "L" level for the internal synchronization mode. Connect to the $EX910f_H I$ pin of the synchronizing signal generator for NTSC operation and to the $EX282f_H I$ pin for PAL operation.

■ Pin Descriptions (continued)

Pin No.	Symbol	Pin Name	Function Description
16	VR	Vertical reset output	This pin generates a vertical reset pulse for the V-SERATION interval detected in the GLSYNC signal. Connect it to the VR pin of the synchronizing signal generator.
25	SCPCO	Subcarrier phase comparator output	This pin is at "L" level when the SC1 signal leads the GLBSC signal and is at "H" level when the signal lags. At all other times, it is in the high-impedance state.
26	$4f_{SC}$OSCI	Oscillator input for subcarrier circuits	Clock oscillator pins for the subcarrier circuits. Connect these pins to a crystal oscillator, capacitor, and variable capacitor. (The pins have built-in feedback resistors.)
27	$4f_{SC}$OSCO	Oscillator output for subcarrier circuits	The circuit oscillates during external synchronization mode. The oscillation stops for internal synchronization mode. The oscillator frequency, $4f_{SC}$, is 14.31818 MHz for NTSC and 14.734 MHz for PAL.
28	$4f_{SC}$	Subcarrier clock output	Clock output from subcarrier circuits. In external synchronization mode, this pin provides the ($4f_{SC}$) clock signal; in internal synchronization mode, it remains at "L" level. Connect this pin to the EX$4f_{SC}$I pin on the synchronizing signal generator.
18	LSWCONT	Line switch polarity control output	During PAL operation, this pin emits an error detection pulse if the LSW polarity is wrong, and the chip reverses the LSW polarity. During internal synchronization mode, this pin remains at "L" level. Connect this pin to the LSWCONT pin on the synchronizing signal generator.
19	EXT/INT	Automatic internal/external switching output	If the chip detects GLSYNC input, it switches to external synchronization mode and drives this pin at "H" level. Otherwise, it switches to internal synchronization mode and drives this pin at "L" level. Connect this pin to the EXT/INT pin on the synchronizing signal generator.
5	BGP	Burst gate pulse output	These pulses have a width of 2.5 μs (NTSC) or 2.3 μs (PAL) and trail the rising edge of the HSYNC signal by 5.3 μs (NTSC) or 5.6 μs. They are generated for only 10 H to 256 H (NTSC) or 304 H (PAL) after the VR pulse.
20	HBLK	Horizontal blanking output	These pulses have a width of 8.9 μs (NTSC) or 8.8 μs (PAL) and follow the rising edge of the HSYNC signal.
21 10	TEST1 TEST2	Test inputs	Leave these test inputs open. (The pins include built-in pull-up resistors.)

■ Timing Chart

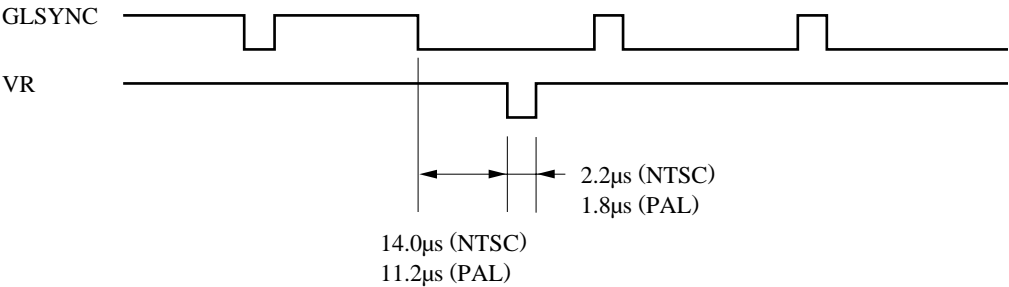### 1. Horizontal synchronization block

This block compares the phases of the HSYNC signal derived by separating off the horizontal component of the GLSYNC input and the WHD signal from the synchronizing signal generator after it has passed through the monostable multivibrator. It is thus possible to adjust the horizontal phase by adjusting the CR integral circuit's time constant.
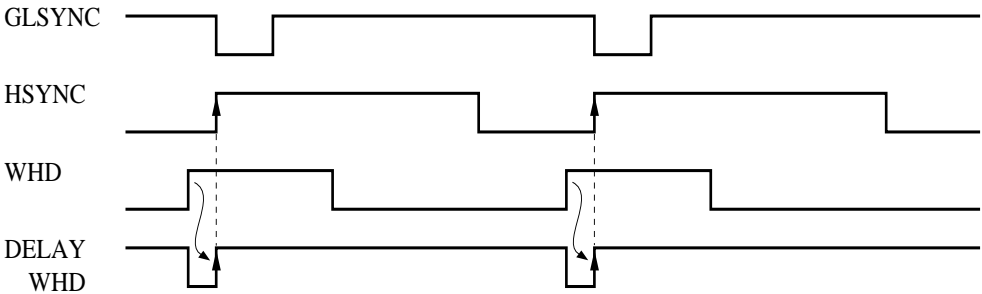
Timing chart for horizontal pulse phase comparison

2. Vertical synchronization block

This block detects the V-SERATION interval in the GLSYNC input and generates a vertical reset (VR) pulse with 0.5 H of the start of that interval. It then issues no pulses for 256 H (NTSC) or 304 H (PAL) after this VR pulse.

2.2μs (NTSC)
1.8μs (PAL)

14.0μs (NTSC)
11.2μs (PAL)

Vertical reset pulse timing chart

3. Subcarrier synchronization block

This block converts the SC1 output from the synchronizing signal generator into four signals with the same frequency as the burst subcarrier, but different phases. In this phase-locked loop circuit, the phase of GLBSC is compared with the phase selected by 2 bits (SCPSW1 and SCPSW2).

During PAL operation, if the LSW polarity is wrong, this block sends an error detection pulse (LSWCONT) to the synchronizing signal generator and reverses the LSW polarity. It also adjusts the relationship between fields 1 through 4.

4. Oscillator blocks

The Xf_H and $4f_{SC}$ oscillator blocks operate only during external synchronization mode. Connecting a variable capacitor creates voltage-controlled oscillators that generate the synchronization signal circuit clock (Xf_H) and subcarrier circuit clock ($4f_{SC}$) for output to the synchronization signal generator.

5. Automatic internal/external switching block

If it detects a minimum of ten edges from the GLSYNC input, this block switches the chip to the external synchronization mode and drives the EXT/INT pin at "H" level. If there are no edges in the GLSYNC input for 10 H, this block switches the chip to the internal synchronization mode and drives this pin at "L" level.

HBLK and BGP plus generator

GLSYNC

HBLK

BGP

5.3μs (NTSC)
5.6μs (PAL)

2.5μs (NTSC)
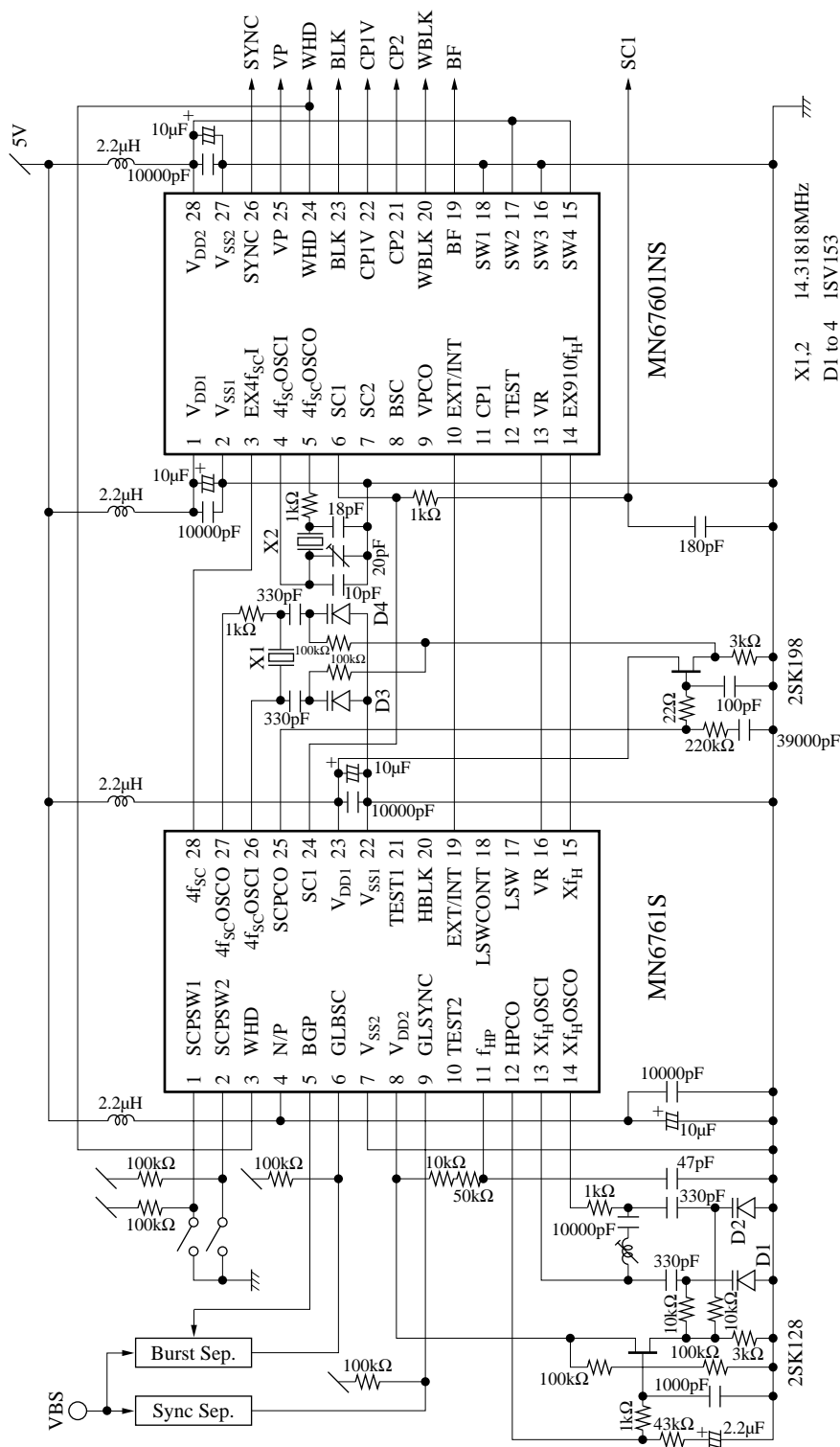2.3μs (PAL)

8.9μs (NTSC)
8.8μs (PAL)
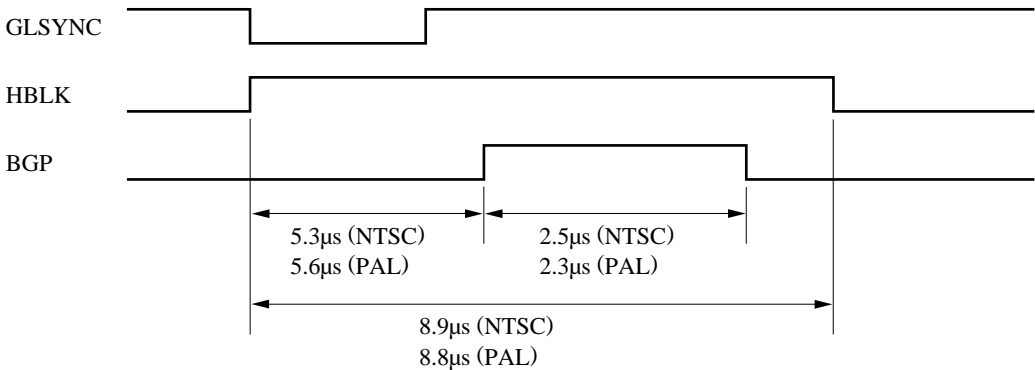
HBLK and BGP pulse timing chart

There is an HBLK pulse for each H.

BGP pulses are generated for only 10 H to 256 H (NTSC) or 304 H (PAL) after the VR pulse.

■ Application Circuit Example

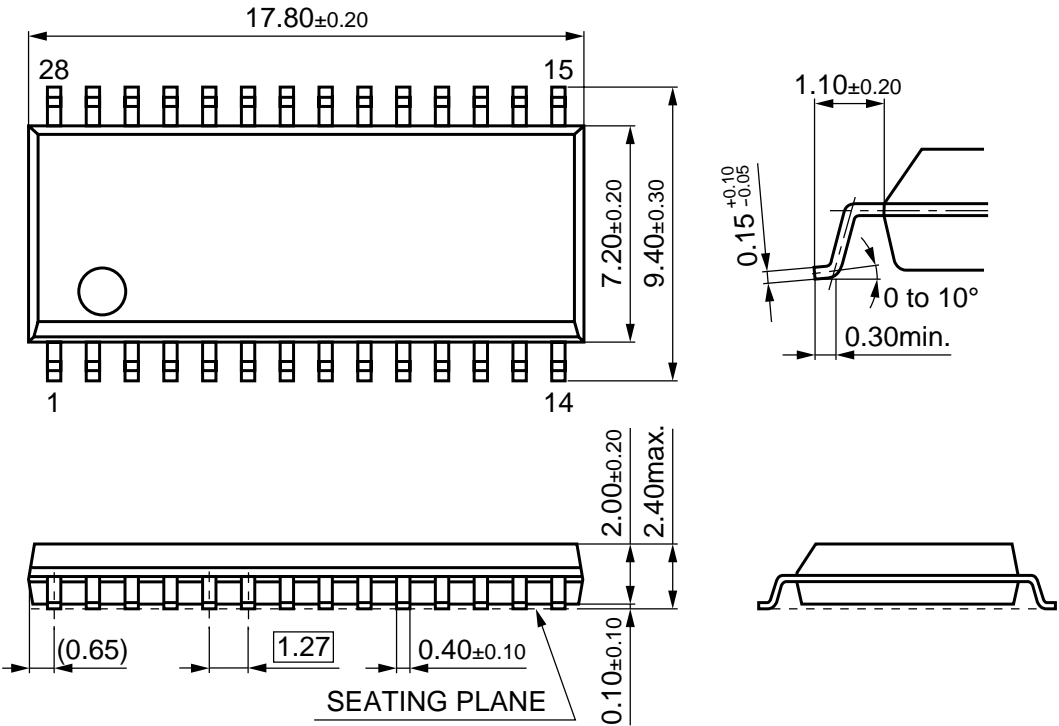1. External synchronization for NTSC system

■ Application Circuit Example

2. External synchronization for PAL system

SYNC VP WHD BLK CP1V CP2 WBLK BF

MN67602PS

V_DD2 28
V_SS2 27
SYNC 26
VP 25
WHD 24
BLK 23
CP1V 22
CP2 21
WBLK 20
BF 19
SCBLK 18
HPCO 17
282f_HOSCI 16
282f_HOSCO 15

V_DD1 1
V_SS1 2
EX4f_SCI 3
4f_SCOSCI 4
4f_SCOSCO 5
SC1 6
SC2 7
BSC 8
VPCO 9
EXT/INT 10
LSWCONT 11
LSW 12
VR 13
EX282f_HI 14

D1 to 5 1SV153
Q1 to 3 2SK198
X1,2   17.734MHz

7.5kΩ 2.2μF
1200pF 1kΩ
Q3 3kΩ
SC2 SC1
1000pF 10kΩ 15pF
1kΩ 330pF D5

5V
2.2μH
2.2μF 10μF
10000pF

1kΩ
180pF
1kΩ
180pF
12pF

MN6761S

4f_SC 28
4f_SCOSCO 27
4f_SCOSCI 26
SCPCO 25
SC1 24
V_DD1 23
V_SS1 22
TEST1 21
HBLK 20
EXT/INT 19
LSWCONT 18
LSW 17
VR 16
Xf_H 15

SCPSW1 1
SCPSW2 2
WHD 3
N/P 4
BGP 5
GLBSC 6
V_SS2 7
V_DD2 8
GLSYNC 9
TEST2 10
f_HP 11
HPCO 12
Xf_HOSCI 13
Xf_HOSCO 14

2.2μH
10μF
10000pF

X2
1kΩ 18pF
20pF
1kΩ 330pF 10pF D4
X1
100kΩ
100kΩ
330pF D3

3kΩ
Q2
22Ω 100pF
220kΩ 39000pF

10000pF
10μF

2.2μH

100kΩ
100kΩ
100kΩ
100kΩ

10kΩ
50kΩ

47pF
1kΩ
10000pF 330pF D2 D1
330pF

Q1 10kΩ 10kΩ
100kΩ 100kΩ 3kΩ
1000pF
1kΩ 43kΩ 2.2μF

Burst Sep.

VBS

Sync Sep.

100kΩ

■ Package Dimensions (Unit: mm)

SOP028-P-0375

17.80±0.20

28   15

7.20±0.20
9.40±0.30

1   14

1.10±0.20

0.15 +0.10 -0.05

0 to 10°

0.30min.

2.00±0.20
2.40max.

(0.65)   1.27   0.40±0.10

SEATING PLANE

0.10±0.10

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