

Diagonal 4.5mm (Type 1/4) Progressive Scan CCD Image Sensor with Square Pixel for Color Cameras

Description

The ICX098BQ is a diagonal 4.5mm (Type 1/4) interline CCD solid-state image sensor with a square pixel array which supports VGA format. Progressive scan allows all pixels signals to be output independently within approximately 1/30 second. Also, the adoption of monitoring mode allows output to an NTSC monitor without passing through the memory. This chip features an electronic shutter with variable charge-storage time which makes it possible to realize full-frame still image without a mechanical shutter. High resolution and high color reproducibility are achieved through the use of R, G, B primary color mosaic filters. Further, high sensitivity and low dark current are achieved through the adoption of HAD (Hole-Accumulation Diode) sensors.

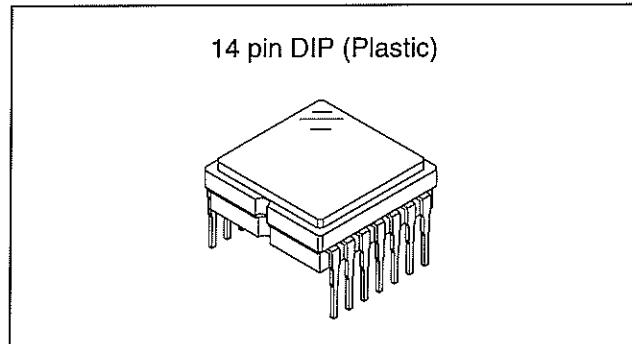
This chip is suitable for applications such as electronic still cameras, PC input cameras, etc.

Features

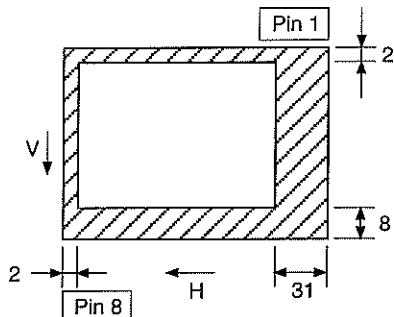
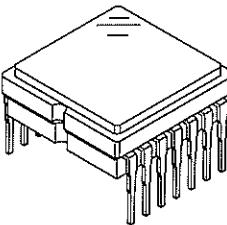
- Progressive scan allows individual readout of the image signals from all pixels.
- High horizontal and vertical resolution (both approx. 400TV-lines) still image without a mechanical shutter.
- Supports monitoring mode
- Square pixel
- Supports VGA format
- Horizontal drive frequency: 12.27MHz
- No voltage adjustments (Reset gate and substrate bias need no adjustment.)
- R, G, B primary color mosaic filters on chip
- High resolution, high color reproducibility, high sensitivity, low dark current
- Continuous variable-speed shutter
- Low smear
- Excellent antiblooming characteristics
- Horizontal register: 3.3V drive
- 14-pin high precision plastic package (enables dual-surface standard)

Device Structure

- Interline CCD image sensor
- Image size: Diagonal 4.5mm (Type 1/4)
- Number of effective pixels: 659 (H) x 494 (V) approx. 330K pixels
- Total number of pixels: 692 (H) x 504 (V) approx. 350K pixels
- Chip size: 4.60mm (H) x 3.97mm (V)
- Unit cell size: 5.6 μ m (H) x 5.6 μ m (V)
- Optical black: Horizontal (H) direction: Front 2 pixels, rear 31 pixels
Vertical (V) direction: Front 8 pixels, rear 2 pixels
- Number of dummy bits: Horizontal 16
Vertical 5
- Substrate material: Silicon



14 pin DIP (Plastic)

Optical black position
(Top View)

WfineCCD®

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Represents a CCD adopting progressive scan, primary color filter and square pixel.

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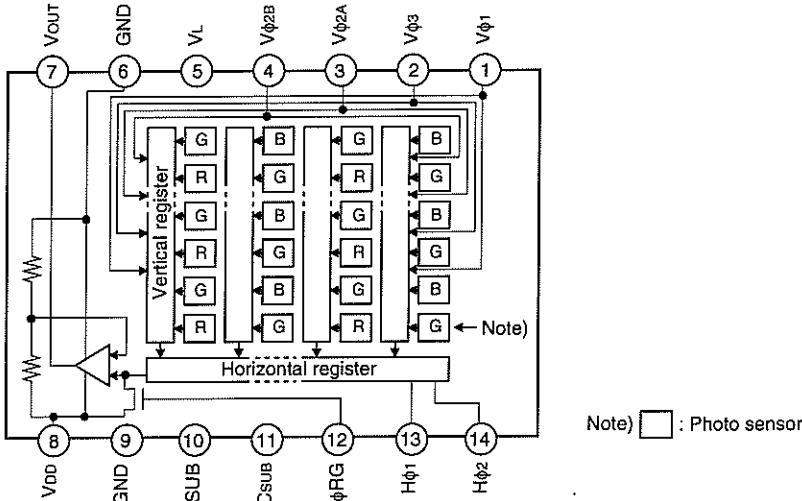
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Block Diagram and Pin Configuration

(Top View)



Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	Vφ1	Vertical register transfer clock	8	VDD	Supply voltage
2	Vφ3	Vertical register transfer clock	9	GND	GND
3	Vφ2A	Vertical register transfer clock	10	φSUB	Substrate clock
4	Vφ2B	Vertical register transfer clock	11	Csub	Substrate bias*1
5	V_L	Protective transistor bias	12	φRG	Reset gate clock
6	GND	GND	13	Hφ1	Horizontal register transfer clock
7	Vout	Signal output	14	Hφ2	Horizontal register transfer clock

*1 DC bias is generated within the CCD, so that this pin should be grounded externally through a capacitance of 0.1μF.

Absolute Maximum Ratings

	Item	Ratings	Unit	Remarks
Against φSUB	VDD, Vout, φRG – φSUB	–40 to +10	V	
	Vφ2A, Vφ2B – φSUB	–50 to +15	V	
	Vφ1, Vφ3, V_L – φSUB	–50 to +0.3	V	
	Hφ1, Hφ2, GND – φSUB	–40 to +0.3	V	
	Csub – φSUB	–25 to	V	
Against GND	VDD, Vout, φRG, Csub – GND	–0.3 to +18	V	
	Vφ1, Vφ2A, Vφ2B, Vφ3 – GND	–10 to +18	V	
	Hφ1, Hφ2 – GND	–10 to +5	V	
Against V_L	Vφ2A, Vφ2B – V_L	–0.3 to +28	V	
	Vφ1, Vφ3, Hφ1, Hφ2, GND – V_L	–0.3 to +15	V	
Between input clock pins	Voltage difference between vertical clock input pins	to +15	V	*2
	Hφ1 – Hφ2	–5 to +5	V	
	Hφ1, Hφ2 – Vφ3	–13 to +13	V	
Storage temperature		–30 to +80	°C	
Operating temperature		–10 to +60	°C	

*2 +24V (Max.) when clock width < 10μs, clock duty factor < 0.1%.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V _{DD}	14.55	15.0	15.45	V	
Protective transistor bias	V _L		*1			
Substrate clock	φ _{SUB}		*2			
Reset gate clock	φ _{RG}		*2			

*1 V_L setting is the V_{VL} voltage of the vertical transfer clock waveform, or the same power supply as the V_L power supply for the V driver should be used.

*2 Do not apply a DC bias to the substrate clock and reset gate clock pins, because a DC bias is generated within the CCD.

DC Characteristics

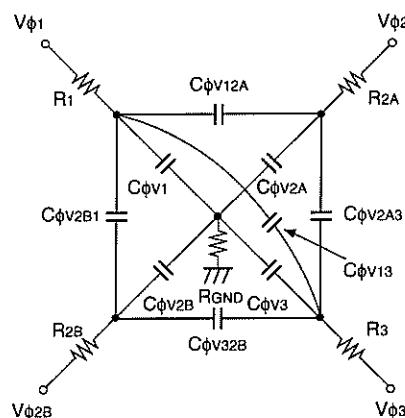
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply current	I _{DD}		6.0		mA	

Clock Voltage Conditions

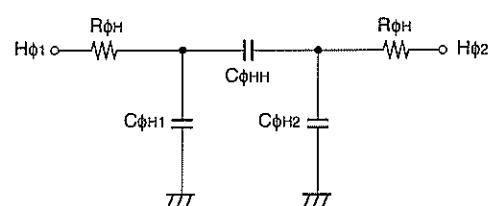
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Readout clock voltage	V _{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V _{VH02A}	-0.05	0	0.05	V	2	V _{VH} = V _{VH02A}
	V _{VH1} , V _{VH2A} , V _{VH2B} , V _{VH3}	-0.2	0	0.05	V	2	
	V _{VL1} , V _{VL2A} , V _{VL2B} , V _{VL3}	-5.8	-5.5	-5.2	V	2	V _{VL} = (V _{VL1} +V _{VL3})/2
	V _{φ1} , V _{φ2A} , V _{φ2B} , V _{φ3}	5.2	5.5	5.8	V	2	
	V _{VL1} - V _{VL3}			0.1	V	2	
	V _{VH}			0.3	V	2	High-level coupling
	V _{VHL}			1.0	V	2	High-level coupling
	V _{VLH}			0.5	V	2	Low-level coupling
	V _{VLL}			0.5	V	2	Low-level coupling
Horizontal transfer clock voltage	V _{φH}	3.0	3.3	5.25	V	3	
	V _{HL}	-0.05	0	0.05	V	3	
Reset gate clock voltage	V _{φRG}	3.0	3.3	5.5	V	4	
	V _{RGHL} - V _{RGLL}			0.4	V	4	Low-level coupling
	V _{RG} - V _{RGlm}			0.5	V	4	Low-level coupling
Substrate clock voltage	V _{φSUB}	19.75	20.5	21.25	V	5	

Clock Equivalent Circuit Constant

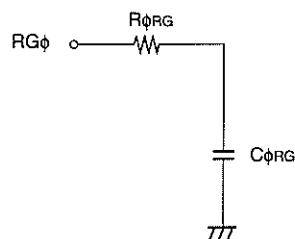
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1}$		2200		pF	
	$C_{\phi V2A}, C_{\phi V2B}$		1500		pF	
	$C_{\phi V3}$		1000		pF	
Capacitance between vertical transfer clocks	$C_{\phi V12A}, C_{\phi V2B1}$		390		pF	
	$C_{\phi V2A3}, C_{\phi V32B}$		680		pF	
	$C_{\phi V13}$		820		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}, C_{\phi H2}$		15		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		47		pF	
Capacitance between reset gate clock and GND	$C_{\phi RG}$		3		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		270		pF	
Vertical transfer clock series resistor	R_1		15		Ω	
	R_{2A}, R_{2B}		100		Ω	
	R_3		62		Ω	
Vertical transfer clock ground resistor	R_{GND}		47		Ω	
Horizontal transfer clock series resistor	$R_{\phi H}$		15		Ω	
Reset gate clock series resistor	$R_{\phi RG}$		62		Ω	



Vertical transfer clock equivalent circuit



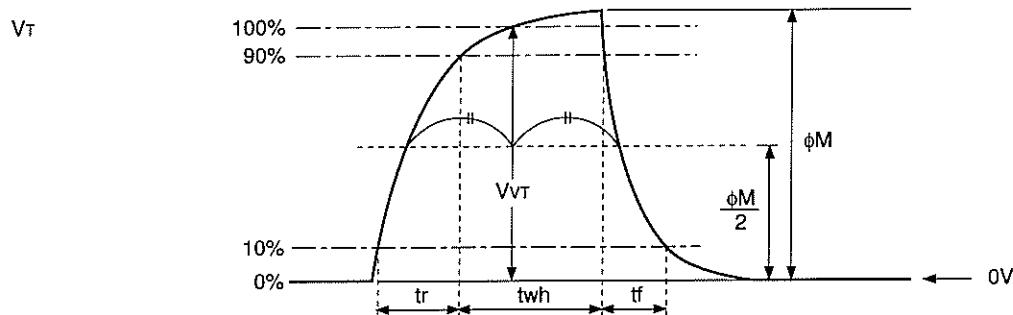
Horizontal transfer clock equivalent circuit



Reset gate clock equivalent circuit

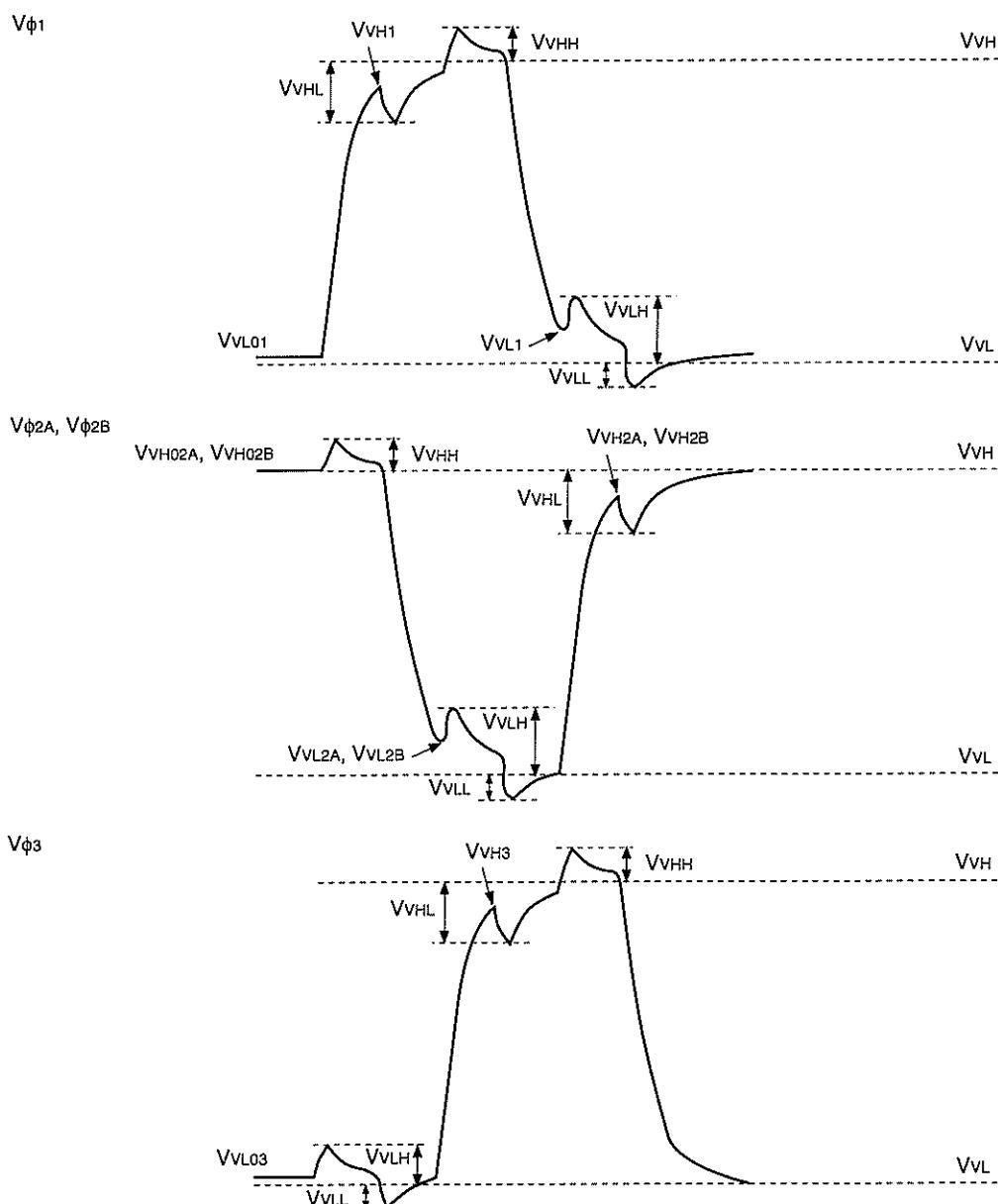
Drive Clock Waveform Conditions

(1) Readout clock waveform



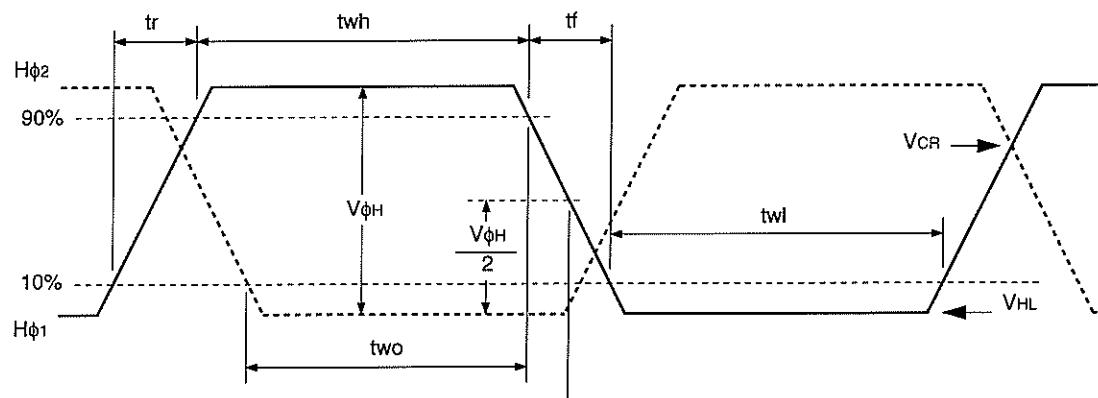
Note) Readout clock is used by composing vertical transfer clocks $V\phi_{2A}$ and $V\phi_{2B}$.

(2) Vertical transfer clock waveform

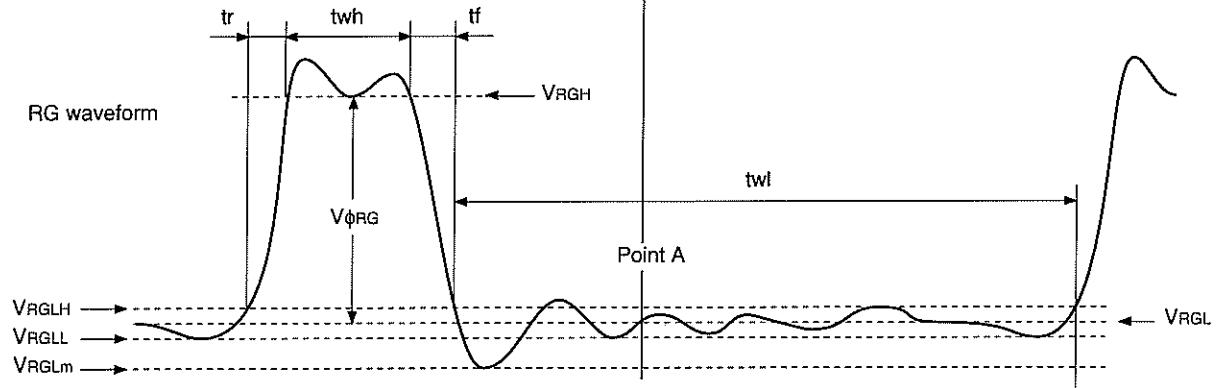


$$\begin{aligned} V_{VH} &= V_{VH02A} \\ V_{VL} &= (V_{VL01} + V_{VL03}) / 2 \\ V_{VL3} &= V_{VL03} \end{aligned}$$

$$\begin{aligned} V\phi_1 &= V_{VH1} - V_{VL01} \\ V\phi_2A &= V_{VH02A} - V_{VL2A} \\ V\phi_2B &= V_{VH02B} - V_{VL2B} \\ V\phi_3 &= V_{VH3} - V_{VL03} \end{aligned}$$

(3) Horizontal transfer clock waveform

Cross-point voltage for the $H\phi_1$ rising side of the horizontal transfer clocks $H\phi_1$ and $H\phi_2$ waveforms is V_{CR} . The overlap period for twh and twl of horizontal transfer clocks $H\phi_1$ and $H\phi_2$ is two.

(4) Reset gate clock waveform

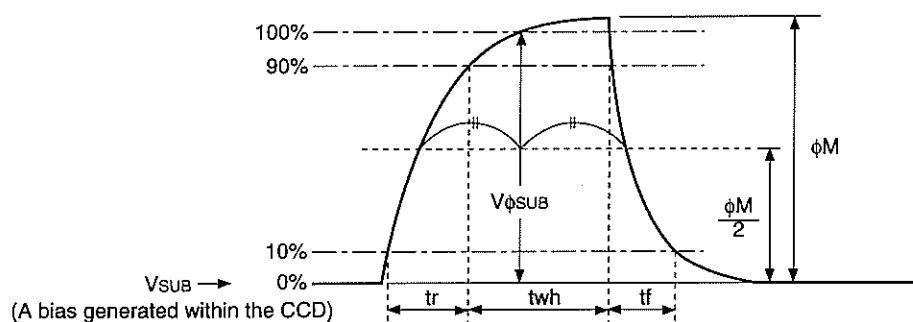
$VRGLH$ is the maximum value and $VRGLL$ is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG . In addition, $VRGL$ is the average value of $VRGLH$ and $VRGLL$.

$$VRGL = (VRGLH + VRGLL)/2$$

Assuming $VRGH$ is the minimum value during the interval twh , then:

$$V\phi_{RG} = VRGH - VRGL$$

Negative overshoot level during the falling edge of RG is $VRGLm$.

(5) Substrate clock waveform

Clock Switching Characteristics

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock	V _T	2.3	2.5					0.5			0.5			μs	During readout
Vertical transfer clock	V _{Φ1} , V _{Φ2A} , V _{Φ2B} , V _{Φ3}										15		350	ns	*1
Horizontal transfer clock	During imaging	H _{Φ1}	25.5	30.5		28	33		9	16.5		9	16.5	ns	*2
	During parallel-serial conversion	H _{Φ2}	28	33		25.5	30.5		9	14		9	14		
Reset gate clock	φ _{RG}	11	12		63.5			3			3			ns	
Substrate clock	φ _{SUB}	1.5	1.8								0.5		0.5	μs	When draining charge

*1 When vertical transfer clock driver CXD1267AN is used.

*2 $tf \geq tr - 2\text{ns}$, and the cross-point voltage (V_{CR}) for the H_{Φ1} rising side of the H_{Φ1} and H_{Φ2} waveforms must be at least V_{ΦH}/2 [V].

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	H _{Φ1} , H _{Φ2}	21.5	25.5		ns	

Spectral Sensitivity Characteristics (excludes lens characteristics and light source characteristics)

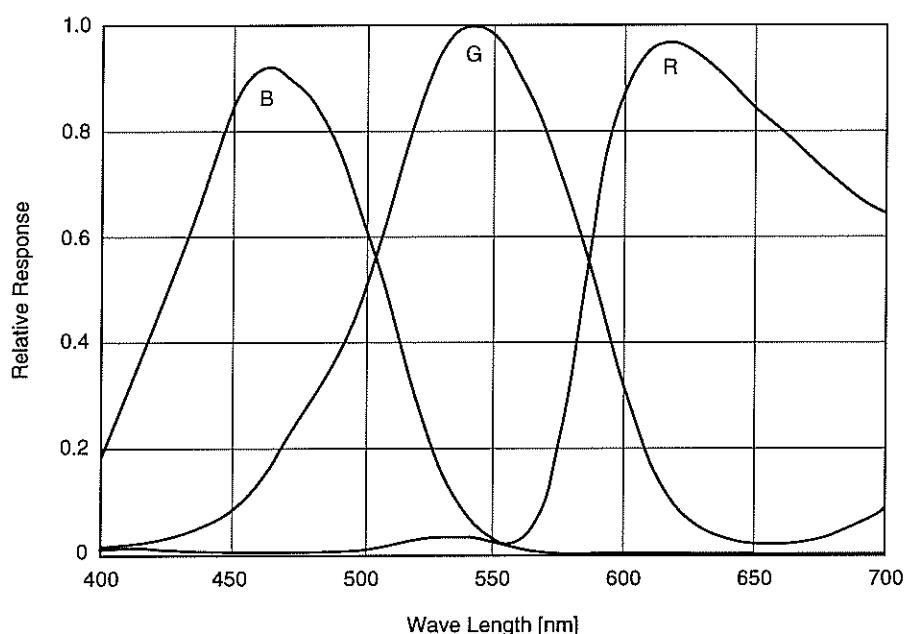
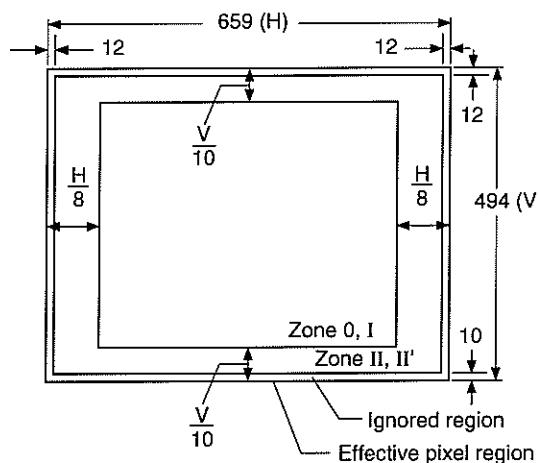


Image Sensor Characteristics

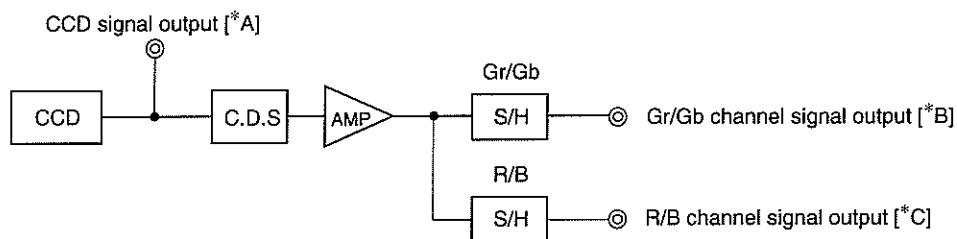
(Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
G sensitivity	Sg	460	580		mV	1	
Sensitivity comparison	R	0.4	0.55	0.7		1	
	B	0.3	0.45	0.6		1	
Saturation signal	Vsat	500			mV	2	Ta = 60°C
Smear	Sm		0.0008	0.0025	%	3	
Video signal shading	SHg			20	%	4	Zone 0 and I
				25	%	4	Zone 0 to II'
Uniformity between video signal channels	ΔSrg			8	%	5	
	ΔSbg			8	%	5	
Dark signal	Vdt			4	mV	6	Ta = 60°C
Dark signal shading	ΔVdt			1	mV	7	Ta = 60°C
Line crawl G	Lcg			3.8	%	8	
Line crawl R	Lcr			3.8	%	8	
Line crawl B	Lcb			3.8	%	8	
Lag	Lag			0.5	%	9	

Zone Definition of Video Signal Shading



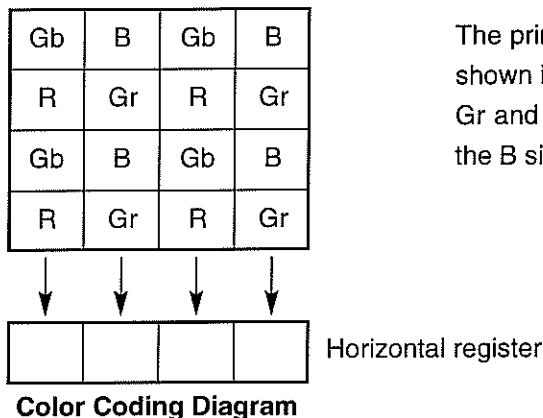
Measurement System



Note) Adjust the amplifier gain so that the gain between [*A] and [*B], and between [*A] and [*C] equals 1.

Image Sensor Characteristics Measurement Method

◎ Color coding and readout of this image sensor



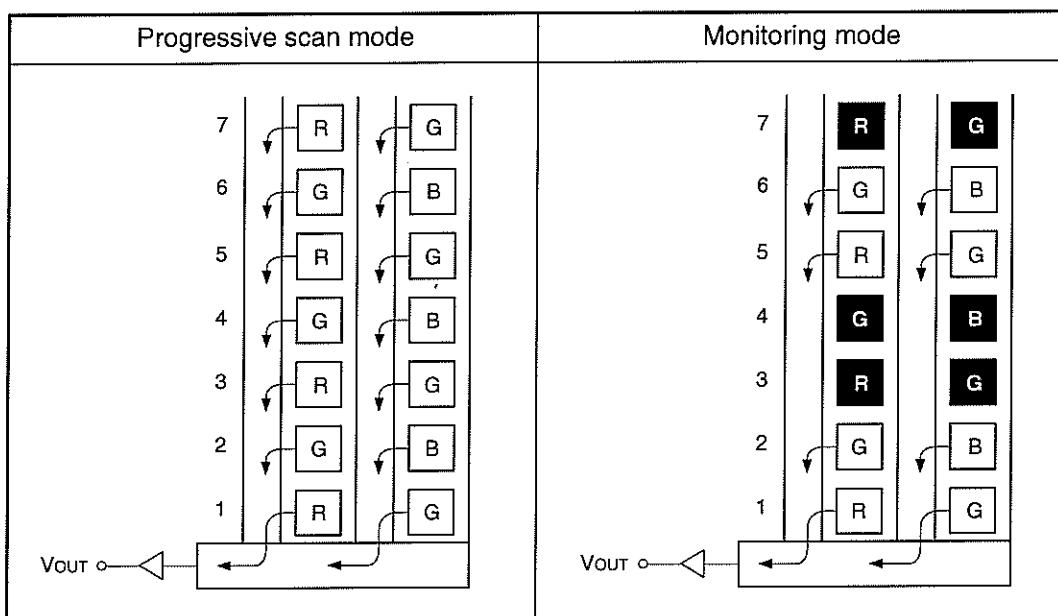
The primary color filters of this image sensor are arranged in the layout shown in the figure on the left (Bayer arrangement). Gr and Gb denote the G signals on the same line as the R signal and the B signal, respectively.

All pixels signals are output successively in a 1/30s period.

The R signal and Gr signal lines and the Gb signal and B signal lines are output successively.

◎ Readout modes

The diagram below shows the output methods for the following two readout modes.



Note) Blacked out portions in the diagram indicate pixels which are not read out.

1. Progressive scan mode

In this mode, all pixel signals are output in non-interlace format in 1/30s.

The vertical resolution is approximately 400TV-lines and all pixel signals within the same exposure period are read out simultaneously, making this mode suitable for high resolution image capturing.

2. Monitoring mode

The signals for all effective areas are output during a single field period of NTSC standard (approximately 1/60s) by repeating readout pixels and non-readout pixels every two lines. The vertical resolution is approximately 200TV-lines. Note that the same pixel signal is output for both odd and even fields.

Since signals are output in a format which conforms to NTSC, the external circuit can be simplified when monitoring using an NTSC monitor.

◎ Measurement conditions

- 1) In the following measurements, the device drive conditions are at the typical values of the bias and clock voltage conditions.
- 2) In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black level (OB) is used as the reference for the signal output, which is taken as the value of the Gr/Gb signal output or the R/B signal output of the measurement system.

◎ Definition of standard imaging conditions

1) Standard imaging condition I:

Use a pattern box (luminance 706cd/m², color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

2) Standard imaging condition II:

Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. G sensitivity, sensitivity comparison

Set to standard imaging condition I. After selecting the electronic shutter mode with a shutter speed of 1/100s, measure the signal outputs (V_{Gr}, V_{Gb}, V_R and V_B) at the center of each Gr, Gb, R and B channel screens, and substitute the values into the following formula.

$$V_G = (V_{Gr} + V_{Gb})/2$$

$$Sg = V_G \times \frac{100}{30} \text{ [mV]}$$

$$Rr = V_R/V_G$$

$$Rb = V_B/V_G$$

2. Saturation signal

Set to standard imaging condition II. After adjusting the luminous intensity to 20 times the intensity with the average value of the Gr signal output, 150mV, measure the minimum values of the Gr, Gb, R and B signal outputs.

3. Smear

Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, first adjust the average value of the Gr signal output to 150mV. Measure the average values of the Gr signal output, Gb signal output, R signal output and B signal output (Gra, Gba, Ra, Ba), and then adjust the luminous intensity to 500 times the intensity with average value of the Gr signal output, 150mV. After the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value (V_{sm} [mV]), independent of the Gr, Gb, R and B signal outputs, and substitute the values into the following formula.

$$Sm = V_{sm} \div \frac{Gra + Gba + Ra + Ba}{4} \times \frac{1}{500} \times \frac{1}{10} \times 100 \text{ [%]} \text{ (1/10V method conversion value)}$$

4. Video signal shading

Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity so that the average value of the Gr signal output is 150mV. Then measure the maximum (Grmax [mV]) and minimum (Grmin [mV]) values of the Gr signal output and substitute the values into the following formula.

$$SHg = (Grmax - Grmin)/150 \times 100 \text{ [%]}$$

5. Uniformity between video signal channels

After measuring 4, measure the maximum (R_{max} [mV]) and minimum (R_{min} [mV]) values of the R signal and the maximum (B_{max} [mV]) and minimum (B_{min} [mV]) values of the B signal, and substitute the values into the following formula.

$$\Delta S_{Rg} = (R_{max} - R_{min})/150 \times 100 [\%]$$

$$\Delta S_{Bg} = (B_{max} - B_{min})/150 \times 100 [\%]$$

6. Dark signal

Measure the average value of the signal output (V_{dt} [mV]) with the device ambient temperature 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

7. Dark signal shading

After measuring 6, measure the maximum (V_{dmax} [mV]) and minimum (V_{dmin} [mV]) values of the dark signal output and substitute the values into the following formula.

$$\Delta V_{dt} = V_{dmax} - V_{dmin} [\text{mV}]$$

8. Line crawl

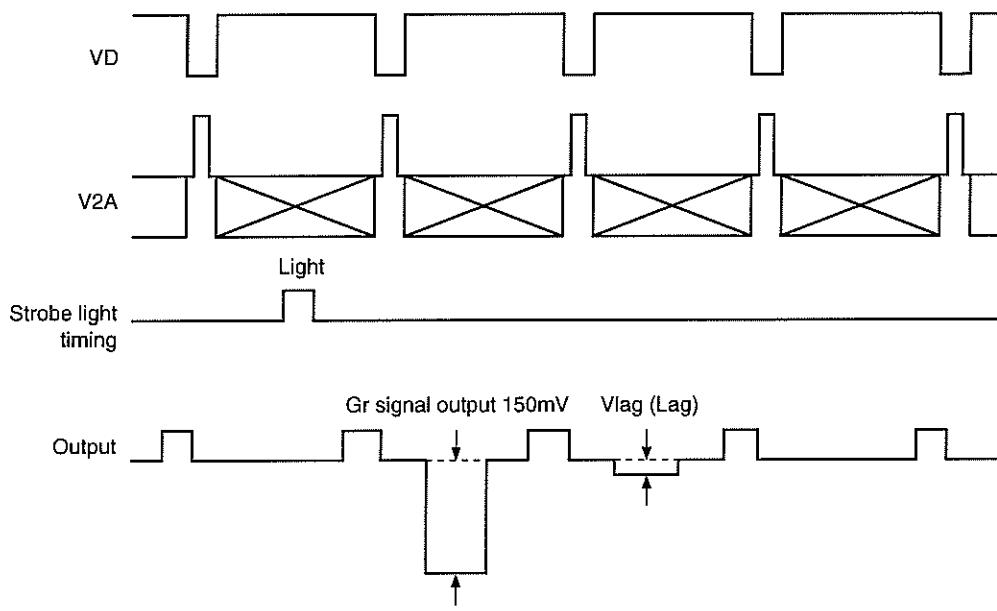
Set to standard imaging condition II. Adjusting the luminous intensity so that the average value of the Gr signal output is 150mV, and then insert R, G, and B filters and measure the difference between G signal lines (ΔG_{lr} , ΔG_{lg} , ΔG_{lb} [mV]) as well as the average value of the G signal output (G_{ar} , G_{ag} , G_{ab}). Substitute the values into the following formula.

$$L_{ci} = \frac{\Delta G_{li}}{G_{ai}} \times 100 [\%] \quad (i = r, g, b)$$

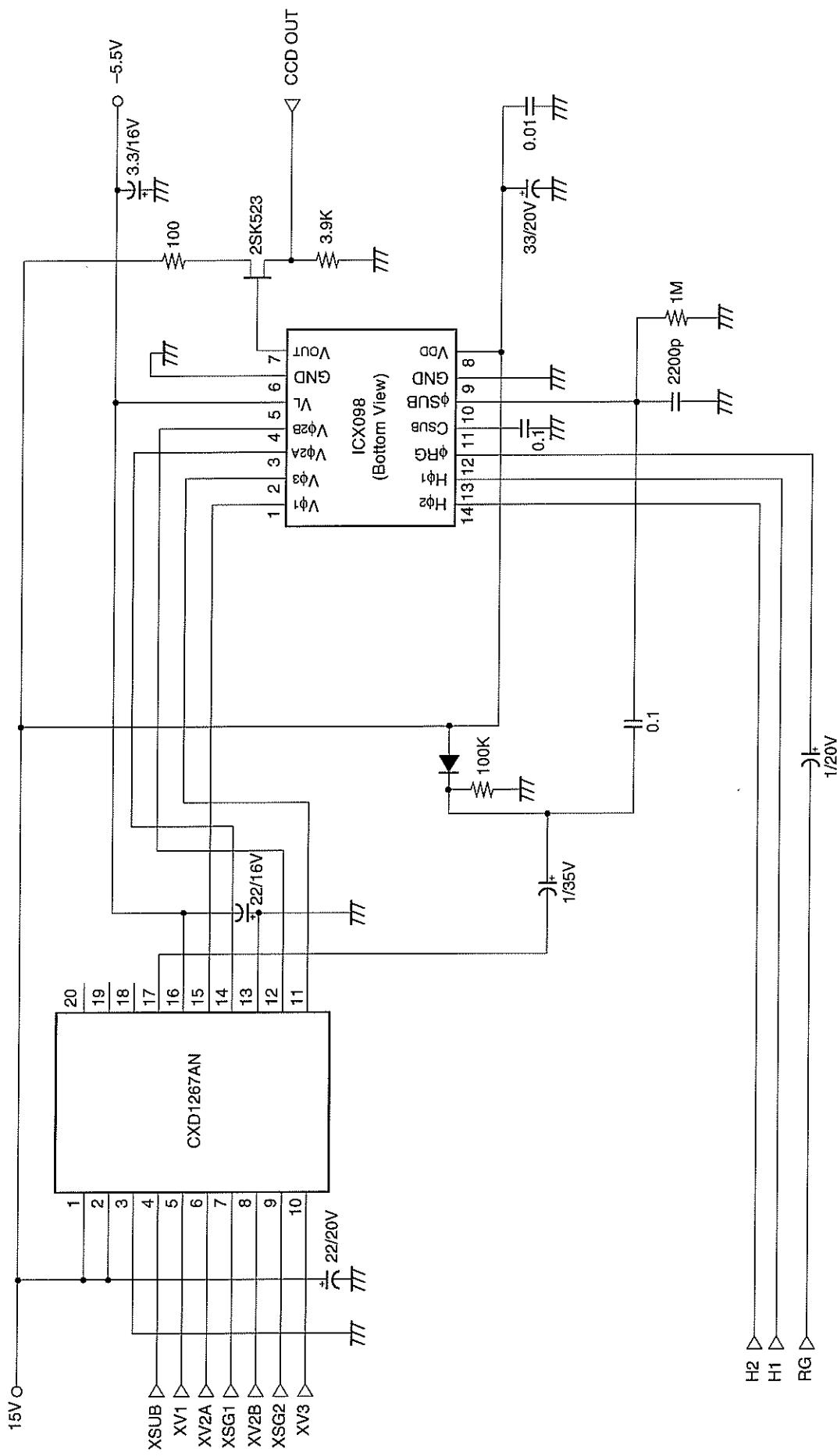
9. Lag

Adjust the Gr signal output value generated by strobe light to 150mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal (V_{lag}). Substitute the value into the following formula.

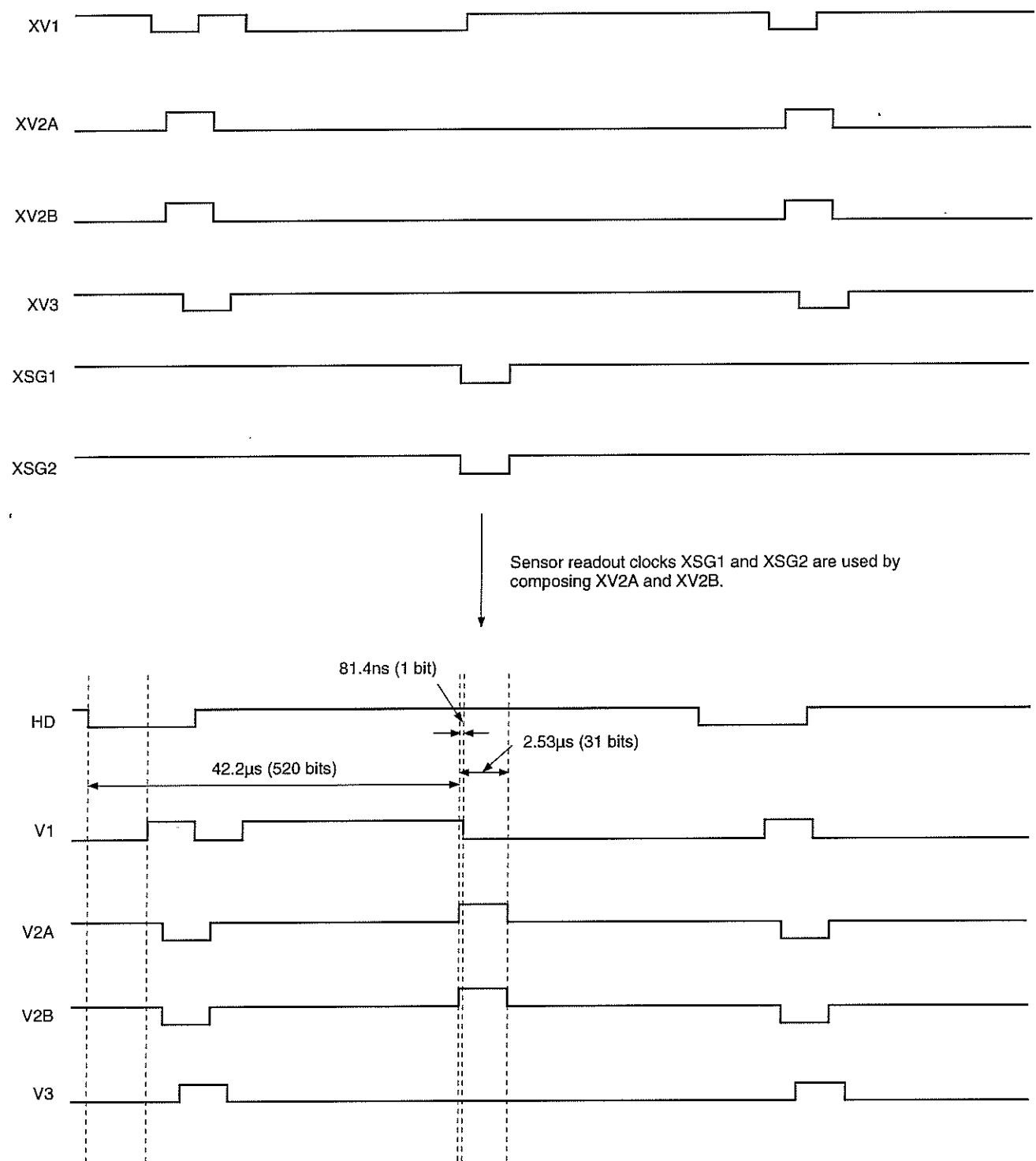
$$\text{Lag} = (V_{lag}/150) \times 100 [\%]$$



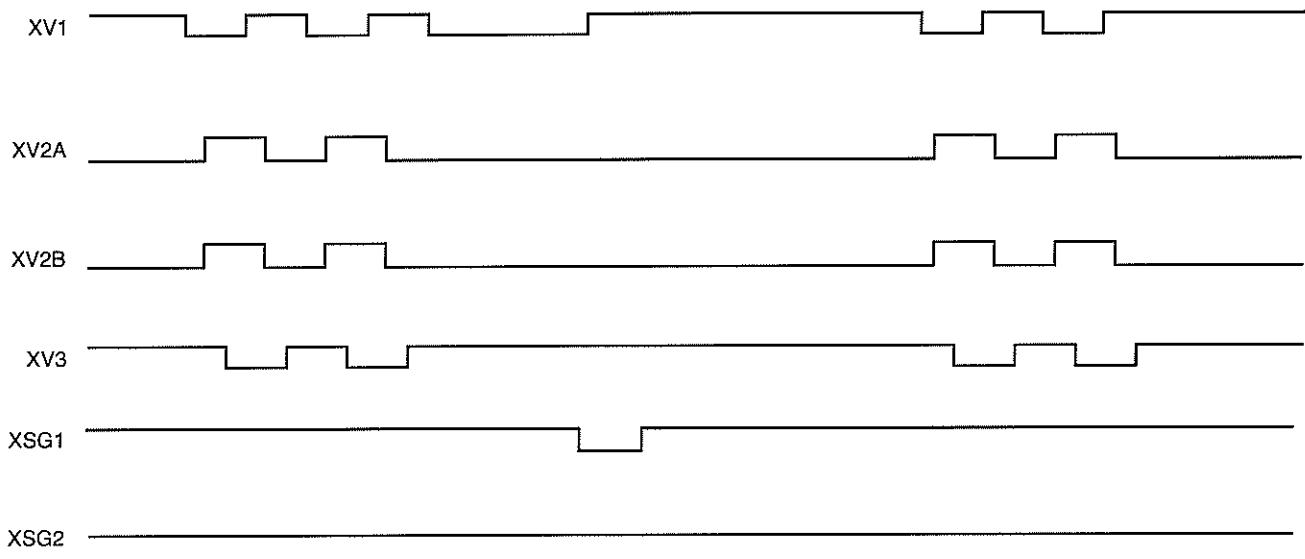
Drive Circuit



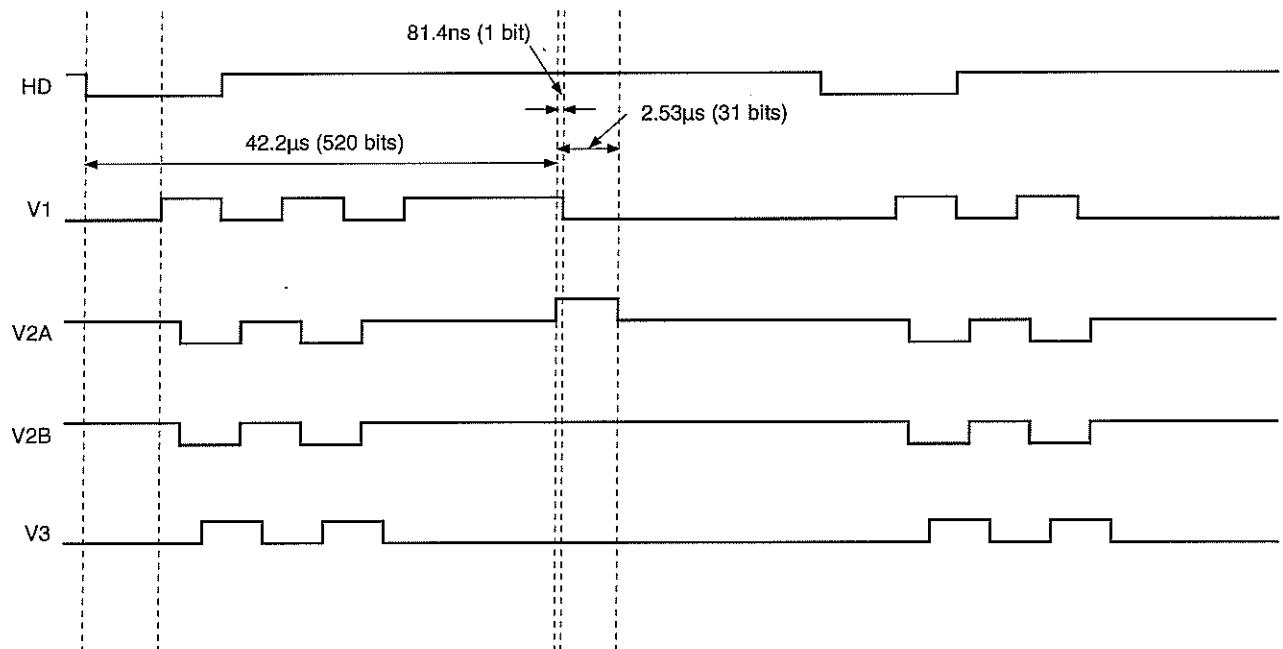
Sensor Readout Clock Timing Chart Progressive Scan Mode



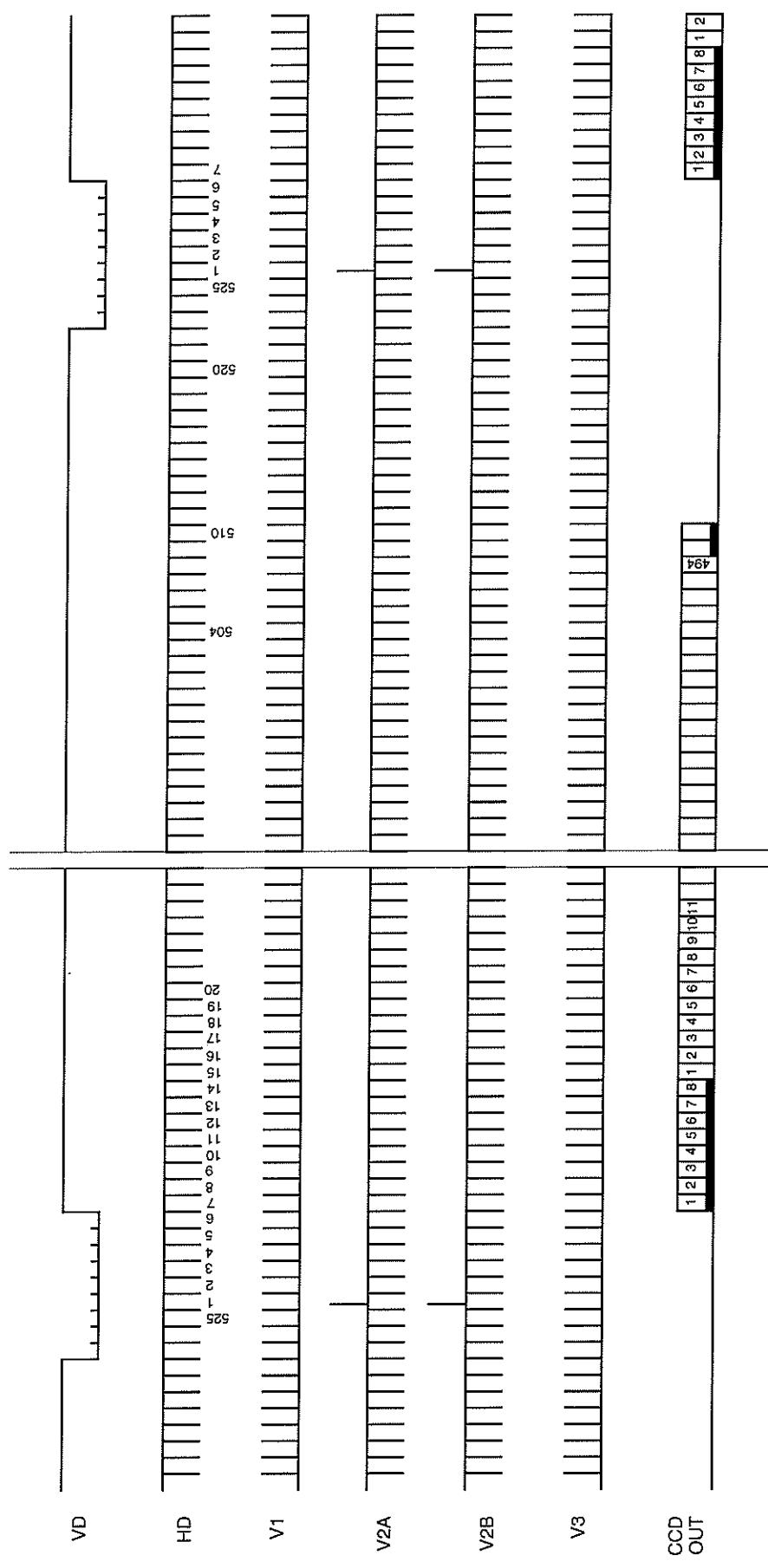
Sensor Readout Clock Timing Chart Monitoring Mode



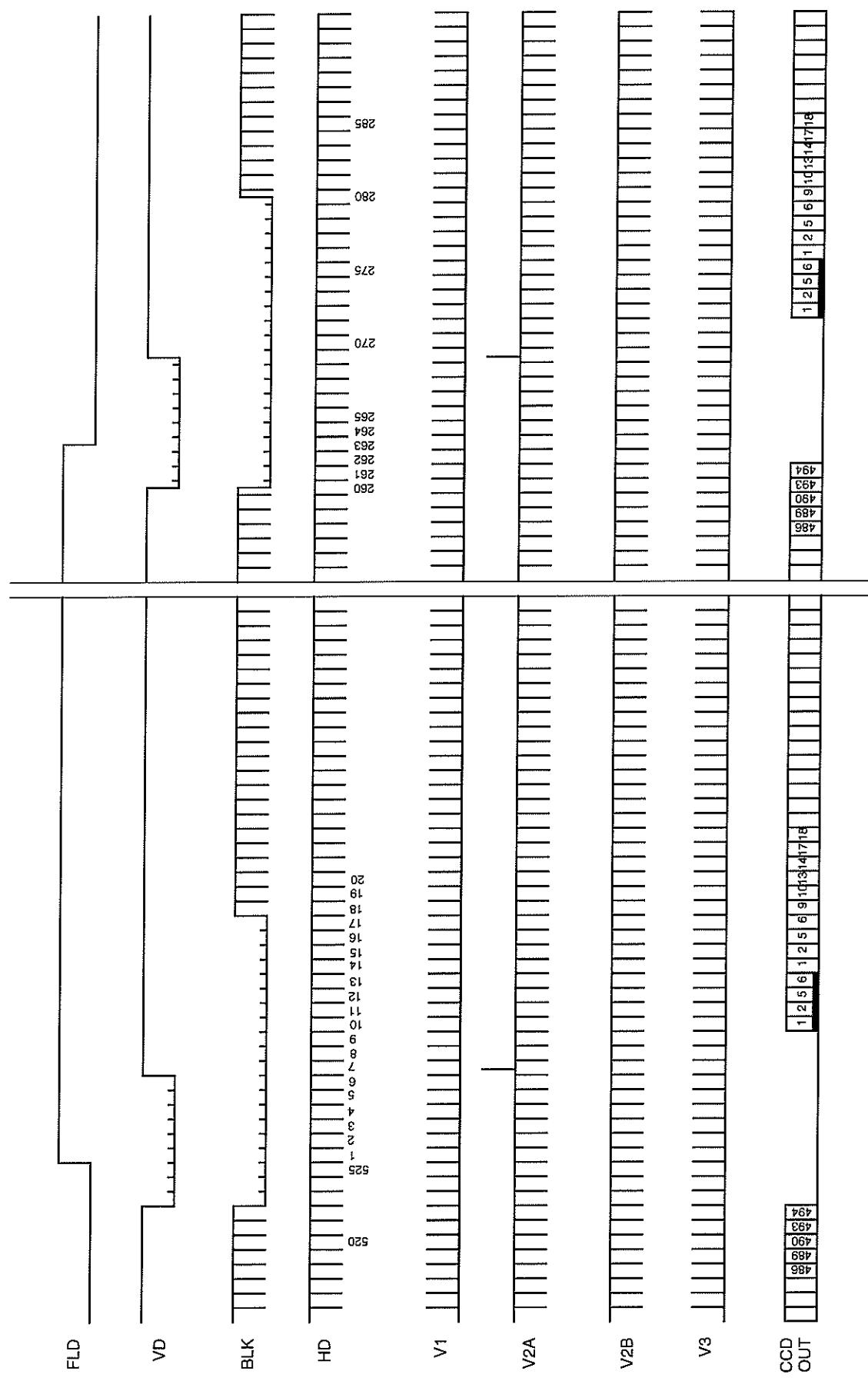
Sensor readout clock XSG1 is used by composing XV2A.



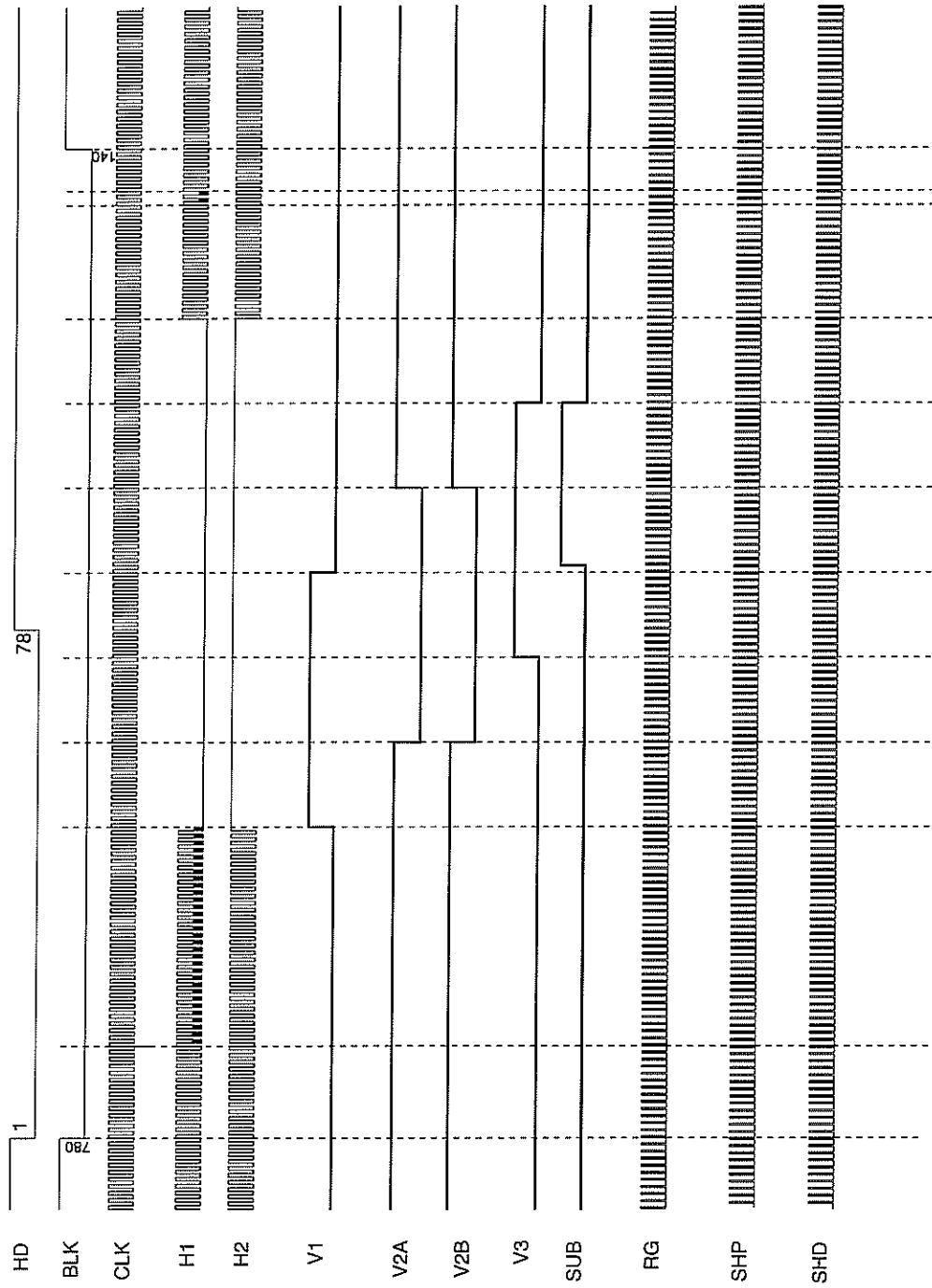
Drive Timing Chart (Vertical Sync) Progressive Scan Mode



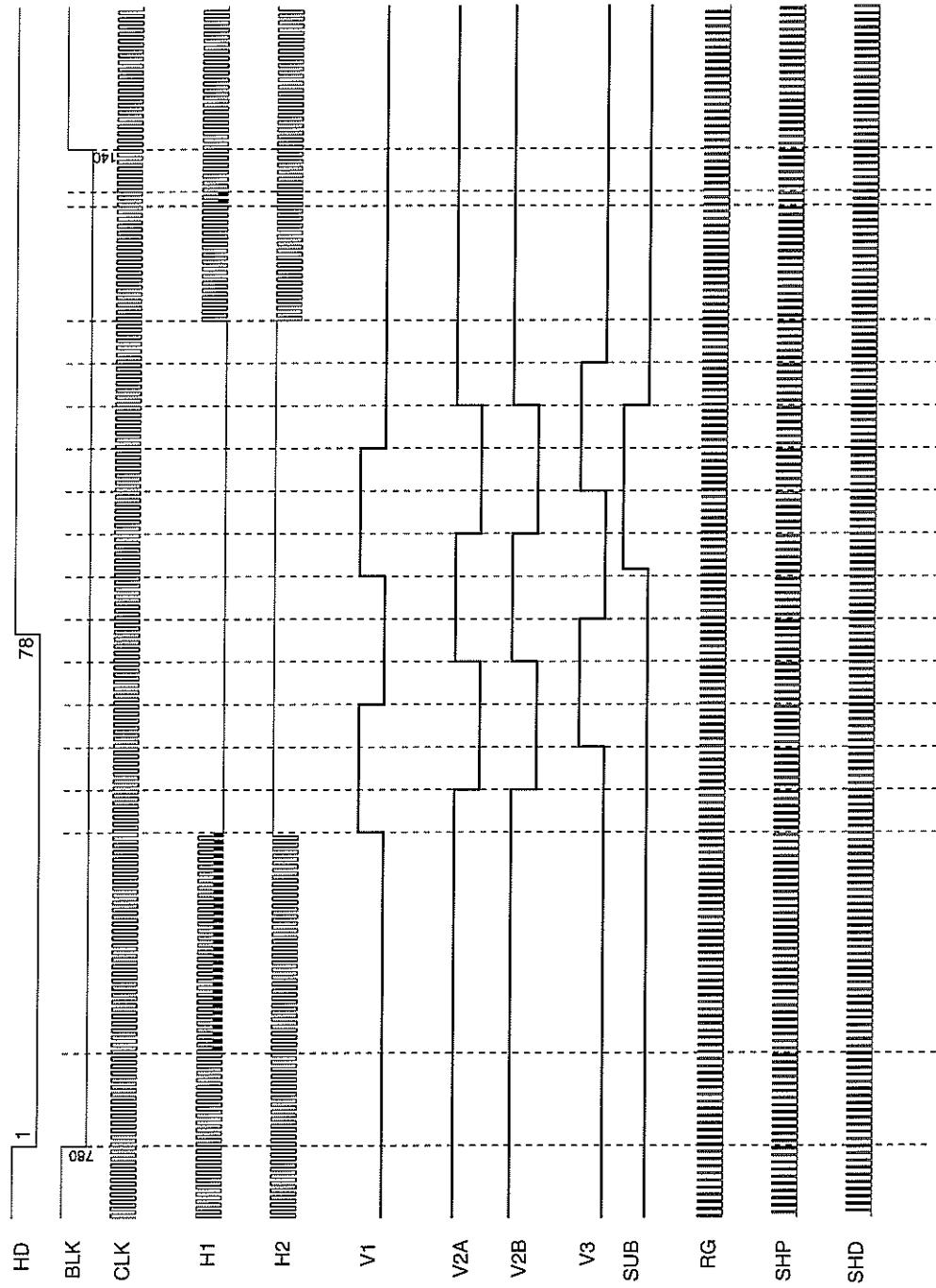
Drive Timing Chart (Vertical Sync) Monitoring Mode



Drive Timing Chart (Horizontal Sync) Progressive Scan Mode



Drive Timing Chart (Horizontal Sync) Monitoring Mode



Notes on Handling

1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

- Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
- When handling directly use an earth band.
- Install a conductive mat on the floor or working table to prevent the generation of static electricity.
- Ionized air is recommended for discharge when handling CCD image sensor.
- For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2) Soldering

- Make sure the package temperature does not exceed 80°C.
- Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a ground 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
- To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero cross On/Off type and connect it to ground.

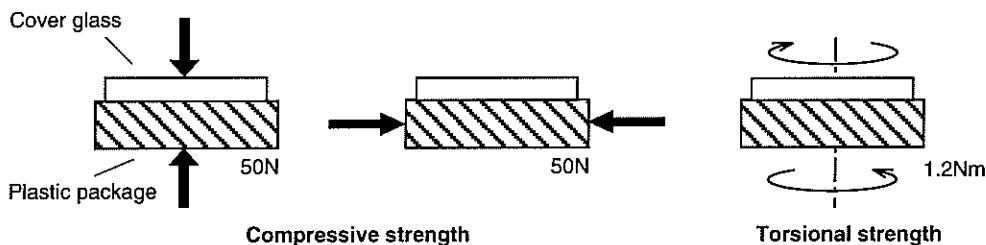
3) Dust and dirt protection

Image sensors are packed and delivered by taking care of protecting its glass plates from harmful dust and dirt. Clean glass plates with the following operation as required, and use them.

- Perform all assembly operations in a clean room (class 1000 or less).
- Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
- Clean with a cotton bud and ethyl alcohol if the grease stained. Be careful not to scratch the glass.
- Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
- When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Installing (attaching)

- Remain within the following limits when applying a static load to the package. Do not apply any load more than 0.7mm inside the outer perimeter of the glass portion, and do not apply any load or impact to limited portions. (This may cause cracks in the package.)

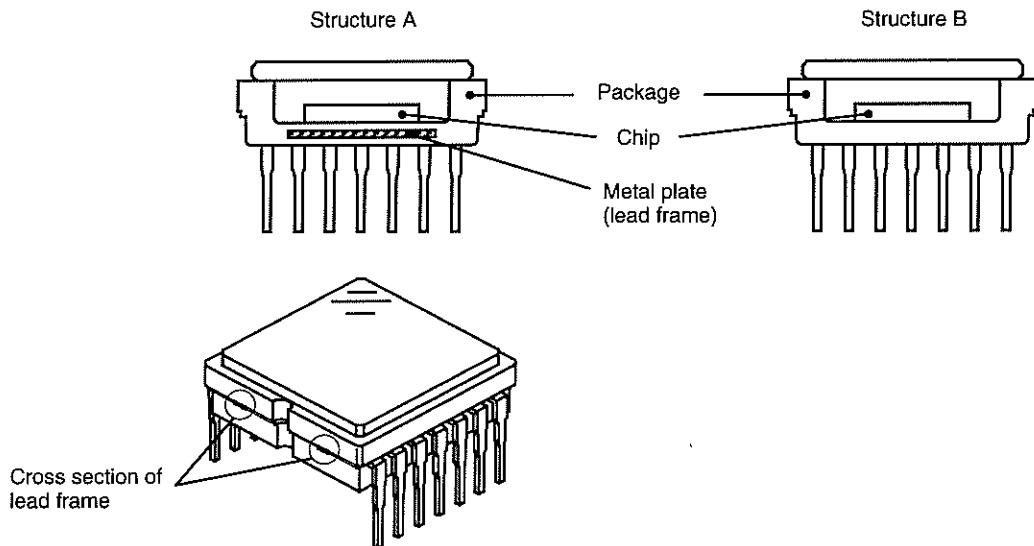


- If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.

- c) The adhesive may cause the marking on the rear surface to disappear, especially in case the regulated voltage value is indicated on the rear surface. Therefore, the adhesive should not be applied to this area, and indicated values should be transferred to the other locations as a precaution.
- d) The notch of the package is used for directional index, and that can not be used for reference of fixing. In addition, the cover glass and seal resin may overlap with the notch of the package.
- e) If the lead bend repeatedly and the metal, etc., clash or rub against the package, the dust may be generated by the fragments of resin.
- f) Acrylate anaerobic adhesives are generally used to attach CCD image sensors. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives. (reference)

5) Others

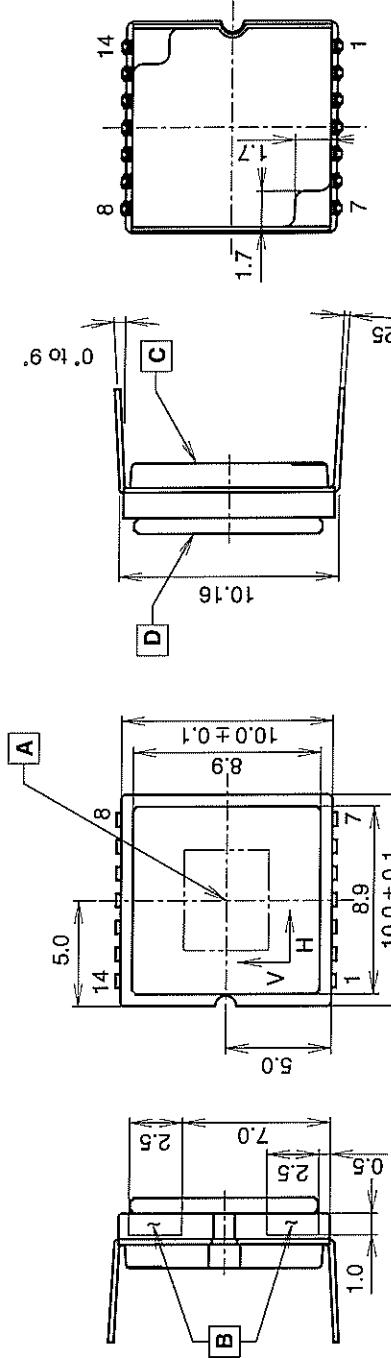
- a) Do not expose to strong light (sun rays) for long periods, color filters will be discolored. When high luminance objects are imaged with the exposure level control by electronic-iris, the luminance of the image-plane may become excessive and discolor of the color filter will possibly be accelerated. In such a case, it is advisable that taking-lens with the automatic-iris and closing of the shutter during the power-off mode should be properly arranged. For continuous using under cruel condition exceeding the normal using condition, consult our company.
- b) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.
- c) The brown stain may be seen on the bottom or side of the package. But this does not affect the CCD characteristics.
- d) This package has 2 kinds of internal structure. However, their package outline, optical size, and strength are the same.



The cross section of lead frame can be seen on the side of the package for structure A.

Package Outline Unit: mm

14 pin DIP (400mil)



1. "A" is the center of the effective image area.
2. The two points "B" of the package are the horizontal reference. The point "B" of the package is the vertical reference.
3. The bottom "C" of the package, and the top of the cover glass "D" are the height reference.
4. The center of the effective image area relative to "B" and "B" is $(H, V) = (5.0, 5.0) \pm 0.15\text{mm}$.
5. The rotation angle of the effective image area relative to H and V is $\pm 1^\circ$.
6. The height from the bottom "C" to the effective image area is $1.41 \pm 0.10\text{mm}$. The height from the top of the cover glass "D" to the effective image area is $1.94 \pm 0.15\text{mm}$.
7. The tilt of the effective image area relative to the bottom "C" is less than $25\mu\text{m}$. The tilt of the effective image area relative to the top "D" of the cover glass is less than $25\mu\text{m}$.
8. The thickness of the cover glass is 0.75mm, and the refractive index is 1.5.
9. The notch of the package is used only for directional index, that must not be used for reference of fixing.
10. Cover glass defect
 - Edge part
Length : no matter, Width : less than 0.5mm, Depth : less than the thickness of the glass.
 - Corner part
Length : less than 1.5mm, Depth : less than the thickness of the glass.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Plastic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.60g
DRAWING NUMBER	AS-D3-02(E)