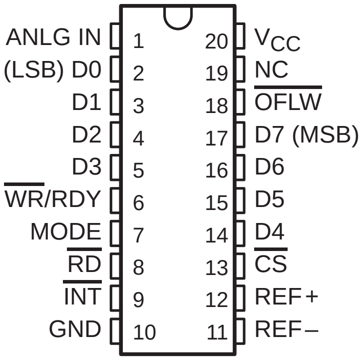
TLC0820AC, TLC0820AI
Advanced LinCMOS™ HIGH-SPEED 8-BIT ANALOG-TO-DIGITAL CONVERTERS USING MODIFIED FLASH TECHNIQUES

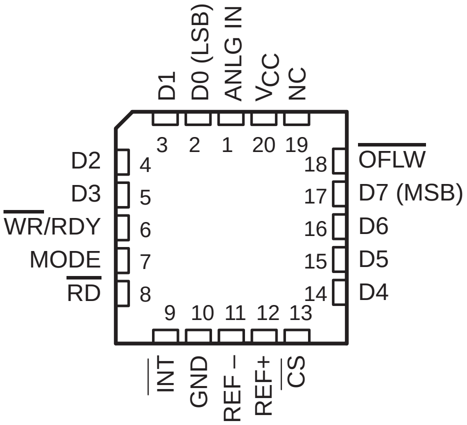
SLAS064A – SEPTEMBER 1986 – REVISED JUNE 1994

- **Advanced LinCMOS™ Silicon-Gate Technology**
- **8-Bit Resolution**
- **Differential Reference Inputs**
- **Parallel Microprocessor Interface**
- **Conversion and Access Time Over Temperature Range**
  Read Mode . . . 2.5 µs Max
- **No External Clock or Oscillator Components Required**
- **On-Chip Track and Hold**
- **Single 5-V Supply**
- **TLC0820A Is Direct Replacement for National Semiconductor ADC0820C/CC and Analog Devices AD7820K/B/T**

DB, DW, OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TLC0820AC and the TLC0820AI are Advanced LinCMOS™ 8-bit analog-to-digital converters each consisting of two 4-bit flash converters, a 4-bit digital-to-analog converter, a summing (error) amplifier, control logic, and a result latch circuit. The modified flash technique allows low-power integrated circuitry to complete an 8-bit conversion in 1.18 µs over temperature. The on-chip track-and-hold circuit has a 100-ns sample window and allows these devices to convert continuous analog signals having slew rates of up to 100 mV/µs without external sampling components. TTL-compatible 3-state output drivers and two modes of operation allow interfacing to a variety of microprocessors. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

AVAILABLE OPTIONS

T_A	TOTAL UNADJUSTED ERROR	PACKAGE			
		SSOP (DB)	PLASTIC SMALL OUTLINE (DW)	PLASTIC CHIP CARRIER (FN)	PLASTIC DIP (N)
0°C to 70°C	±1 LSB	TLC0820ACDB	TLC0820ACDW	TLC0820ACFN	TLC0820ACN
–40°C to 85°C	±1 LSB	—	TLC0820AIDW	TLC0820AIFN	TLC0820AIN

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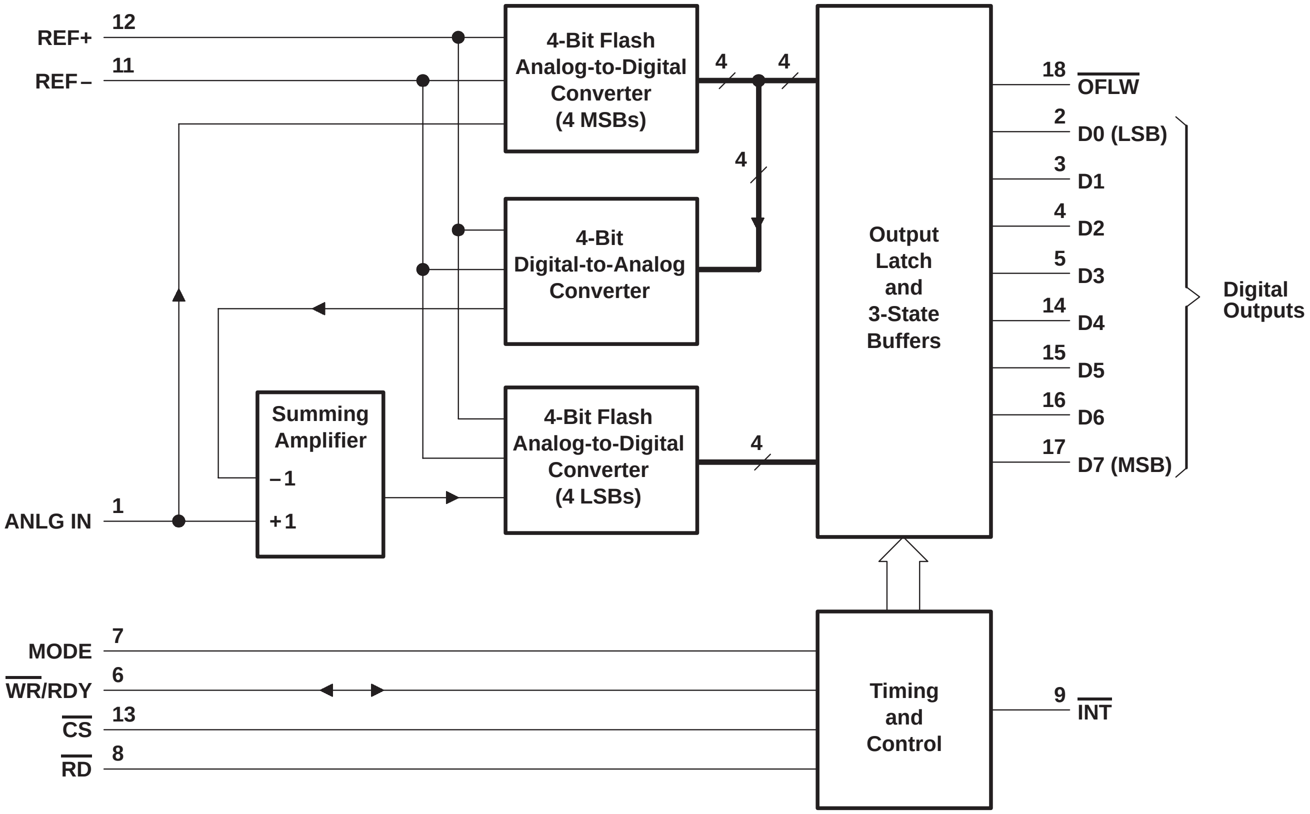
functional block diagram



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
ANLG IN	1	I	Analog input
$\overline{\text{CS}}$	13	I	Chip select. $\overline{\text{CS}}$ must be low in order for $\overline{\text{RD}}$ or $\overline{\text{WR}}$ to be recognized by the ADC.
D0	2	O	Digital, 3-state output data, bit 1 (LSB)
D1	3	O	Digital, 3-state output data, bit 2
D2	4	O	Digital, 3-state output data, bit 3
D3	5	O	Digital, 3-state output data, bit 4
D4	14	O	Digital, 3-state output data, bit 5
D5	15	O	Digital, 3-state output data, bit 6
D6	16	O	Digital, 3-state output data, bit 7
D7	17	O	Digital, 3-state output data, bit 8 (MSB)
GND	10		Ground
$\overline{\text{INT}}$	9	O	Interrupt. In the write-read mode, the interrupt output ($\overline{\text{INT}}$) going low indicates that the internal count-down delay time, $t_{d(int)}$, is complete and the data result is in the output latch. The delay time $t_{d(int)}$ is typically 800 ns starting after the rising edge of $\overline{\text{WR}}$ (see operating characteristics and Figure 3). If $\overline{\text{RD}}$ goes low prior to the end of $t_{d(int)}$, $\overline{\text{INT}}$ goes low at the end of $t_{d(RIL)}$ and the conversion results are available sooner (see Figure 2). $\overline{\text{INT}}$ is reset by the rising edge of either $\overline{\text{RD}}$ or $\overline{\text{CS}}$.
MODE	7	I	Mode select. MODE is internally tied to GND through a 50-µA current source, which acts like a pulldown resistor. When MODE is low, the read mode is selected. When MODE is high, the write-read mode is selected.
NC	19		No internal connection
$\overline{\text{OFLW}}$	18	O	Overflow. Normally $\overline{\text{OFLW}}$ is a logical high. However, if the analog input is higher than V_{ref+}, $\overline{\text{OFLW}}$ will be low at the end of conversion. It can be used to cascade two or more devices to improve resolution (9 or 10 bits).
$\overline{\text{RD}}$	8	I	Read. In the write-read mode with $\overline{\text{CS}}$ low, the 3-state data outputs D0 through D7 are activated when $\overline{\text{RD}}$ goes low. $\overline{\text{RD}}$ can also be used to increase the conversion speed by reading data prior to the end of the internal count-down delay time. As a result, the data transferred to the output latch is latched after the falling edge of $\overline{\text{RD}}$. In the read mode with $\overline{\text{CS}}$ low, the conversion starts with $\overline{\text{RD}}$ going low. $\overline{\text{RD}}$ also enables the 3-state data outputs on completion of the conversion. RDY going into the high-impedance state and $\overline{\text{INT}}$ going low indicate completion of the conversion.
REF –	11	I	Reference voltage. REF – is placed on the bottom of the resistor ladder.
REF +	12	I	Reference voltage. REF + is placed on the top of the resistor ladder.
V_{CC}	20		Power supply voltage
$\overline{\text{WR}}$/RDY	6	I/O	Write ready. In the write-read mode with $\overline{\text{CS}}$ low, the conversion is started on the falling edge of the $\overline{\text{WR}}$ input signal. The result of the conversion is strobed into the output latch after the internal count-down delay time, $t_{d(int)}$, provided that the $\overline{\text{RD}}$ input does not go low prior to this time. The delay time $t_{d(int)}$ is approximately 800 ns. In the read mode, RDY (an open-drain output) goes low after the falling edge of $\overline{\text{CS}}$ and goes into the high-impedance state when the conversion is strobed into the output latch. It is used to simplify the interface to a microprocessor system.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	10 V
Input voltage range, all inputs (see Note 1)	–0.2 V to V_{CC} + 0.2 V
Output voltage range, all outputs (see Note 1)	–0.2 V to V_{CC} + 0.2 V
Operating free-air temperature range: TLC0820AC	0°C to 70°C
TLC0820AI	–40°C to 85°C
Storage temperature range	–65°C to 150°C
Case temperature for 10 seconds: FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DB, DW or N package	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to network GND.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}			4.5	5	8	V
Analog input voltage			–0.1		V_{CC} + 0.1	V
Positive reference voltage, V_{ref+}			V_{ref-}		V_{CC}	V
Negative reference voltage, V_{ref-}			GND		V_{ref+}	V
High-level input voltage, V_{IH}	V_{CC} = 4.75 V to 5.25 V	$\overline{CS}$, $\overline{WR}$/RDY, $\overline{RD}$	2			V
		MODE	3.5			
Low-level input voltage, V_{IL}	V_{CC} = 4.75 V to 5.25 V	$\overline{CS}$, $\overline{WR}$/RDY, $\overline{RD}$			0.8	V
		MODE			1.5	
Pulse duration, write in write-read mode, $t_{w(W)}$ (see Figures 2, 3, and 4)			0.5		50	µs
Operating free-air temperature, T_A	TLC0820AC		0		70	°C
	TLC0820AI		–40		85	

electrical characteristics at specified operating free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	D0–D7, $\overline{\text{INT}}$, or $\overline{\text{OFLW}}$	V_{CC} = 4.75 V, I_{OH} = –360 µA	Full range	2.4			V
			V_{CC} = 4.75 V, I_{OH} = –10 µA	Full range	4.5			
				25°C	4.6			
V_{OL}	Low-level output voltage	D0–D7, $\overline{\text{OFLW}}$, $\overline{\text{INT}}$, or $\overline{\text{WR}}$/RDY	V_{CC} = 5.25 V, I_{OL} = 1.6 mA	Full range			0.4	V
				25°C			0.34	
I_{IH}	High-level input current	$\overline{\text{CS}}$ or $\overline{\text{RD}}$	V_{IH} = 5 V	Full range		0.005	1	µA
		WR/RDY		Full range			3	
				25°C		0.1	0.3	
		MODE		Full range			200	
				25°C		50	170	
I_{IL}	Low-level input current	$\overline{\text{CS}}$, $\overline{\text{WR}}$/RDY, $\overline{\text{RD}}$, or MODE	V_{IL} = 0	Full range		–0.005	–1	µA
I_{OZ}	Off-state (high-impedance-state) output current	D0–D7 or $\overline{\text{WR}}$/RDY	V_O = 5 V	Full range			3	µA
				25°C		0.1	0.3	
			V_O = 0	Full range			–3	
				25°C		–0.1	–0.3	
I_I	Analog input current		CS at 5 V, V_I = 5 V	Full range			3	µA
				25°C			0.3	
			CS at 5 V, V_I = 0	Full range			–3	
				25°C			–0.3	
I_{OS}	Short-circuit output current	D0–D7, $\overline{\text{OFLW}}$, $\overline{\text{INT}}$, or $\overline{\text{WR}}$/RDY	V_O = 5 V	Full range	7			mA
				25°C	8.4	14		
		D0–D7 or $\overline{\text{OFLW}}$	V_O = 0	Full range	–6			
				25°C	–7.2	–12		
		INT		Full range	–4.5			
				25°C	– 5.3	–9		
R_{ref}	Reference resistance			Full range	1.25		6	kΩ
				25°C	1.4	2.3	5.3	
I_{CC}	Supply current		$\overline{\text{CS}}$, $\overline{\text{WR}}$/RDY, and $\overline{\text{RD}}$ at 0 V	Full range			15	mA
				25°C		7.5	13	
C_i	Input capacitance	D0–D7		Full range		5		pF
		ANLG IN				45		
C_o	Output capacitance	D0–D7		Full range			5	pF

† Full range is as specified in recommended operating conditions.

operating characteristics, $V_{CC} = 5$ V, $V_{ref+} = 5$ V, $V_{ref-} = 0$, $t_r = t_f = 20$ ns, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
k_{SVS}	Supply-voltage sensitivity	V_{CC} = 5 V ± 5%,	T_A = MIN to MAX		±1/16	±1/4	LSB
	Total unadjusted error‡	MODE at 0 V,	T_A = MIN to MAX			1	LSB
$t_{conv(R)}$	Conversion time, read mode	MODE at 0 V,	See Figure 1		1.6	2.5	µs
$t_{a(R)}$	Access time, $\overline{\mathrm{RD}}$↓ to data valid	MODE at 0 V,	See Figure 1		$t_{conv(R)}$ +20	$t_{conv(R)}$ +50	ns
$t_{a(R1)}$	Access time, $\overline{\mathrm{RD}}$↓ to data valid	MODE at 5 V, $t_{d(WR)} < t_{d(int)}$, See Figure 2	C_L = 15 pF		190	280	ns
			C_L = 100 pF		210	320	
$t_{a(R2)}$	Access time, $\overline{\mathrm{RD}}$↓ to data valid	MODE at 5 V, $t_{d(WR)} > t_{d(int)}$, See Figure 3	C_L = 15 pF		70	120	ns
			C_L = 100 pF		90	150	
$t_{a(INT)}$	Access time, $\overline{\mathrm{INT}}$↓ to data valid	MODE at 5 V,	See Figure 4		20	50	ns
t_{dis}	Disable time, $\overline{\mathrm{RD}}$↑ to data valid	R_L = 1 kΩ, See Figures 1, 2, 3, and 5	C_L = 10 pF,		70	95	ns
$t_{d(int)}$	Delay time, WR/RDY↑ to INT↓	MODE at 5 V, See Figures 2, 3, and 4	C_L = 50 pF,		800	1300	ns
$t_{d(NC)}$	Delay time, to next conversion	See Figures 1, 2, 3, and 4		500			ns
$t_{d(WR)}$	Delay time, $\overline{\mathrm{WR}}$/RDY↑ to $\overline{\mathrm{RD}}$↓ in write-read mode	See Figure 2		0.4			µs
$t_{d(RDY)}$	Delay time, CS↓ to WR/RDY↓	MODE at 0 V, See Figure 1	C_L = 50 pF,		50	100	ns
$t_{d(RIH)}$	Delay time, $\overline{\mathrm{RD}}$↑ to $\overline{\mathrm{INT}}$↑	C_L = 50 pF,	See Figures 1, 2, and 3		125	225	ns
$t_{d(RIL)}$	Delay time, RD↓ to INT↓	MODE at 5 V, See Figure 2	$t_{d(WR)} < t_{d(int)}$,		200	290	ns
$t_{d(WIH)}$	Delay time, $\overline{\mathrm{WR}}$/RDY↑ to $\overline{\mathrm{INT}}$↑	MODE at 5 V, See Figure 4	C_L = 50 pF,		175	270	ns
	Slew-rate tracking				0.1		V/µs

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ Total unadjusted error includes offset, full-scale, and linearity errors.

PARAMETER MEASUREMENT INFORMATION

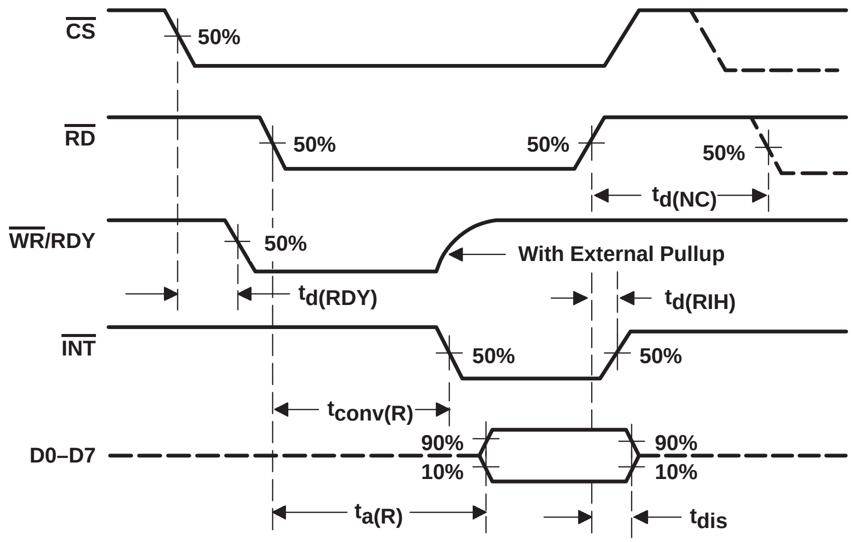


Figure 1. Read-Mode Waveforms (MODE Low)

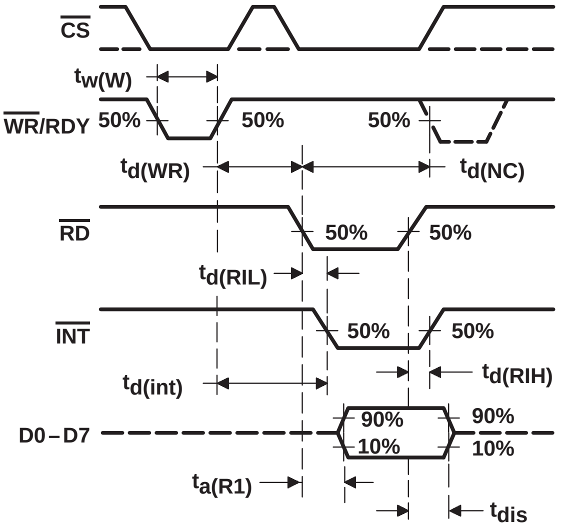


Figure 2. Write-Read-Mode Waveforms [MODE High and $t_{d(WR)} < t_{d(int)}$]

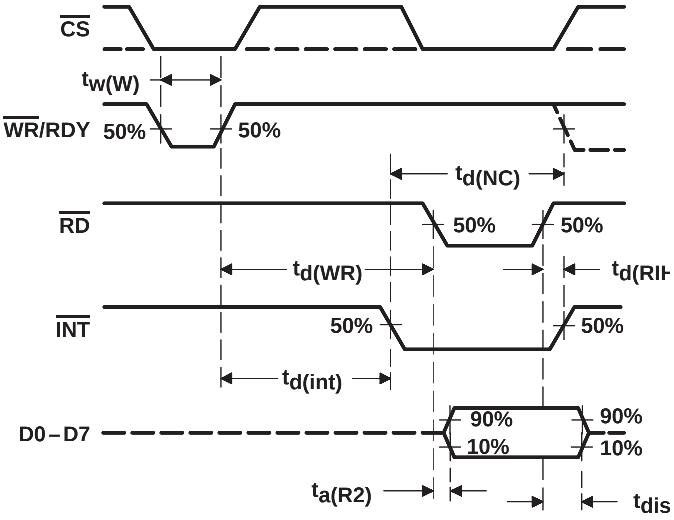


Figure 3. Write-Read-Mode Waveforms [MODE High and $t_{d(WR)} > t_{d(int)}$]

PARAMETER MEASUREMENT INFORMATION

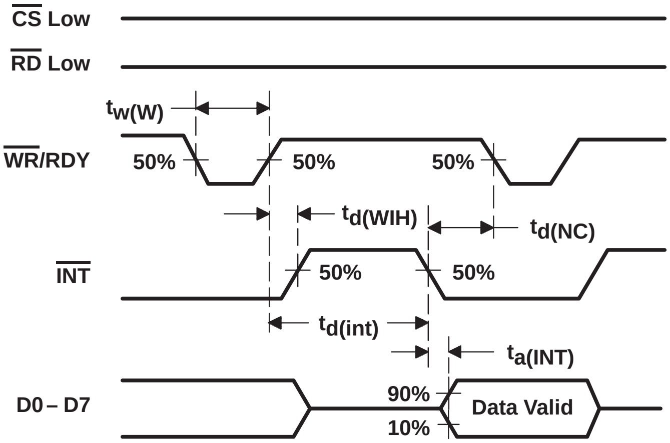


Figure 4. Write-Read-Mode Waveforms
(Stand-Alone Operation, MODE High, and RD Low)

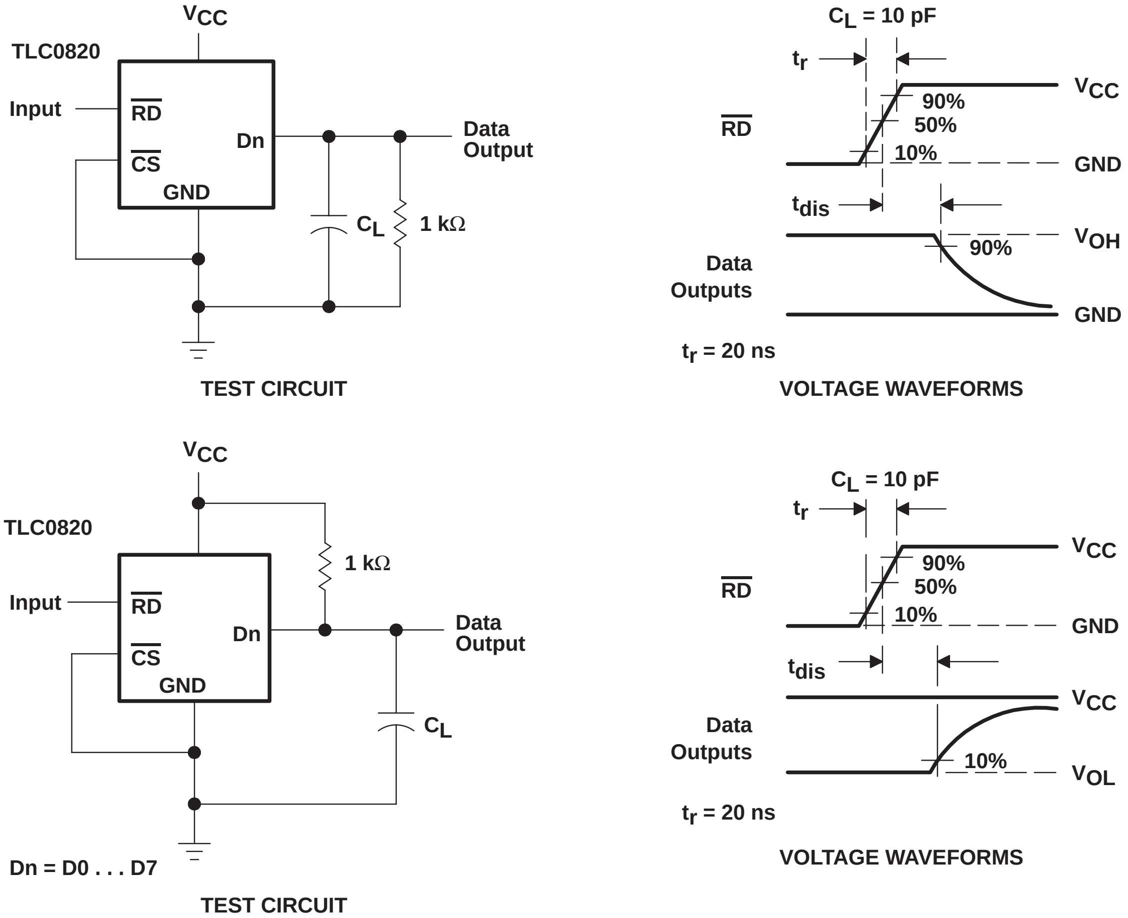


Figure 5. Test Circuit and Voltage Waveforms

PRINCIPLES OF OPERATION

The TLC0820AC and TLC0820AI each employ a combination of sampled-data comparator techniques and flash techniques common to many high-speed converters. Two 4-bit flash analog-to-digital conversions are used to give a full 8-bit output.

The recommended analog input voltage range for conversion is –0.1 V to V_{CC} + 0.1 V. Analog input signals that are less than V_{ref-} + 1/2 LSB or greater than V_{ref+} – 1/2 LSB convert to 00000000 or 11111111, respectively. The reference inputs are fully differential with common-mode limits defined by the supply rails. The reference input values define the full-scale range of the analog input. This allows the gain of the ADC to be varied for ratiometric conversion by changing the V_{ref+} and V_{ref-} voltages.

The device operates in two modes, read (only) and write-read, that are selected by MODE. The converter is set to the read (only) mode when MODE is low. In the read mode, $\overline{\text{WR}}$/RDY is used as an output and is referred to as the ready terminal. In this mode, a low on $\overline{\text{WR}}$/RDY while $\overline{\text{CS}}$ is low indicates that the device is busy. Conversion starts on the falling edge of $\overline{\text{RD}}$ and is completed no more than 2.5 µs later when $\overline{\text{INT}}$ falls and $\overline{\text{WR}}$/RDY returns to the high-impedance state. Data outputs also change from high-impedance to active states at this time. After the data is read, $\overline{\text{RD}}$ is taken high, $\overline{\text{INT}}$ returns high, and the data outputs return to their high-impedance states.

When MODE is high, the converter is set to the write-read mode and $\overline{\text{WR}}$/RDY is referred to as the write terminal. Taking $\overline{\text{CS}}$ and $\overline{\text{WR}}$/RDY low selects the converter and initiates measurement of the input signal. Approximately 600 ns after $\overline{\text{WR}}$/RDY returns high, the conversion is completed. Conversion starts on the rising edge of $\overline{\text{WR}}$/RDY in the write-read mode.

The high-order 4-bit flash ADC measures the input by means of 16 comparators operating simultaneously. A high-precision 4-bit DAC then generates a discrete analog voltage from the result of that conversion. After a time delay, a second bank of comparators does a low-order conversion on the analog difference between the input level and the high-order DAC output. The results from each of these conversions enter an 8-bit latch and are output to the 3-state output buffers on the falling edge of $\overline{\text{RD}}$.

APPLICATION INFORMATION

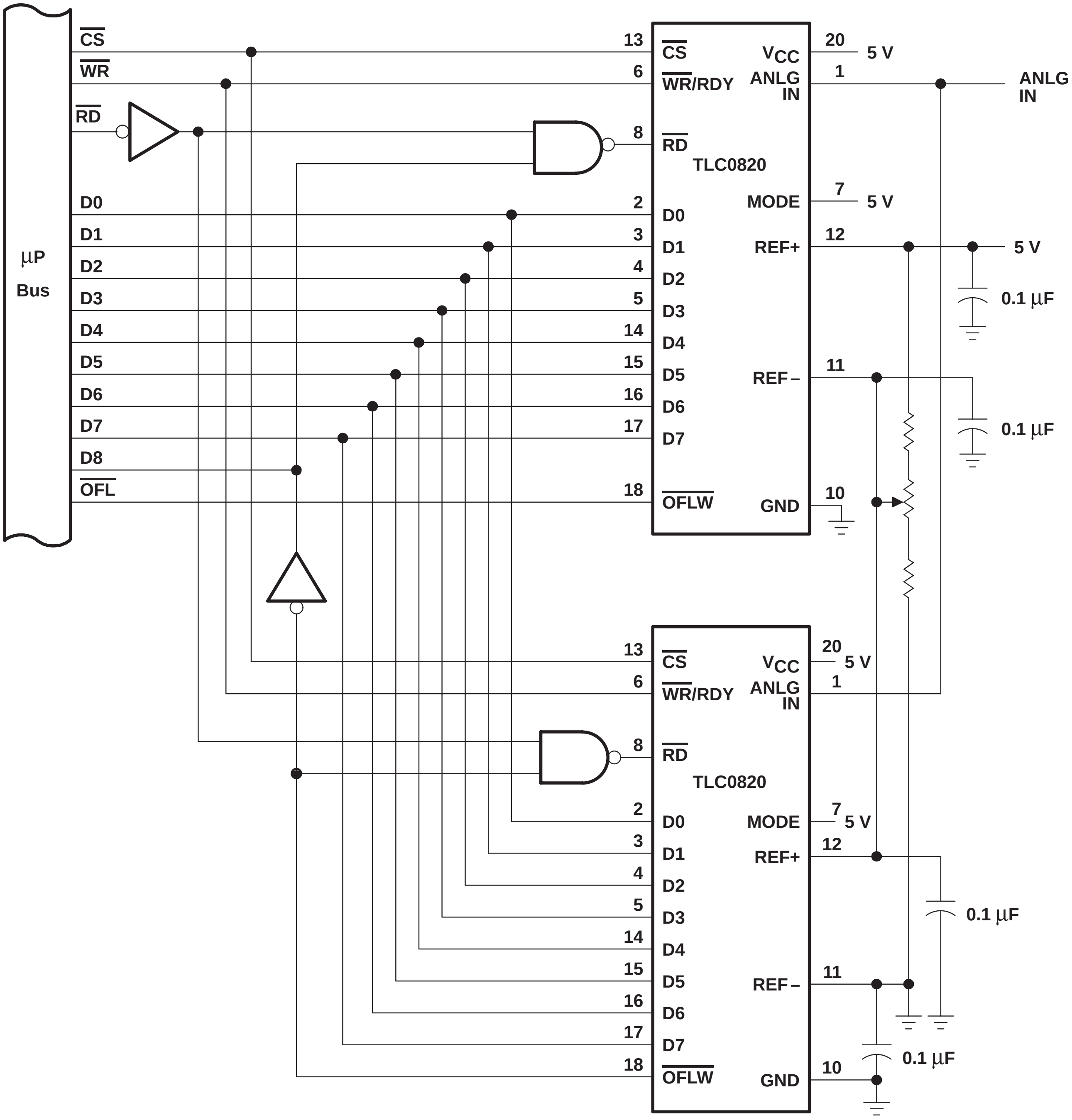


Figure 6. Configuration for 9-Bit Resolution

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC0820ACDB	Active	Production	SSOP (DB) | 20	70 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P0820A
TLC0820ACDB.A	Active	Production	SSOP (DB) | 20	70 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P0820A
TLC0820ACDBR	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	P0820A
TLC0820ACDBR.A	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P0820A
TLC0820ACDW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	TLC0820A
TLC0820ACDW.A	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC0820A
TLC0820ACDWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	TLC0820A
TLC0820ACDWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC0820A
TLC0820ACFN	Obsolete	Production	PLCC (FN) | 20	-	-	Call TI	Call TI	-	TLC0820AC
TLC0820ACN	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-	TLC0820ACN
TLC0820ACN.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC0820ACN
TLC0820AIDW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	TLC0820AI
TLC0820AIDW.A	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC0820AI
TLC0820AIDWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	TLC0820AI
TLC0820AIDWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC0820AI
TLC0820AIFN	Obsolete	Production	PLCC (FN) | 20	-	-	Call TI	Call TI	-	TLC0820AI
TLC0820AIN	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-	TLC0820AIN
TLC0820AIN.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC0820AIN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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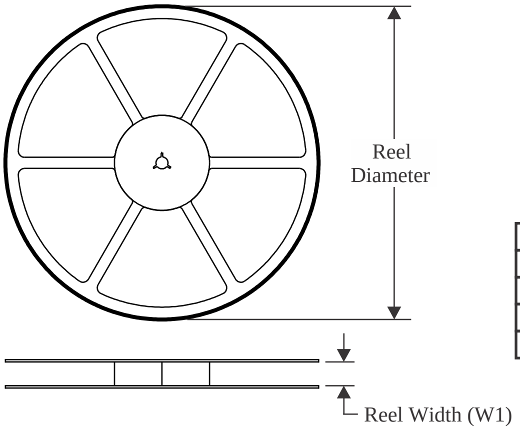
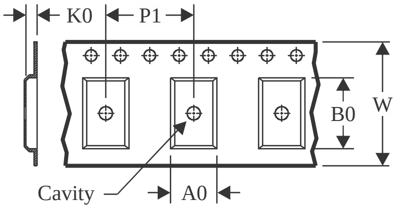
TAPE AND REEL INFORMATION

REEL DIMENSIONS

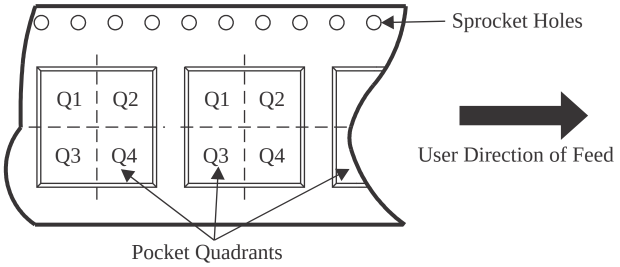


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

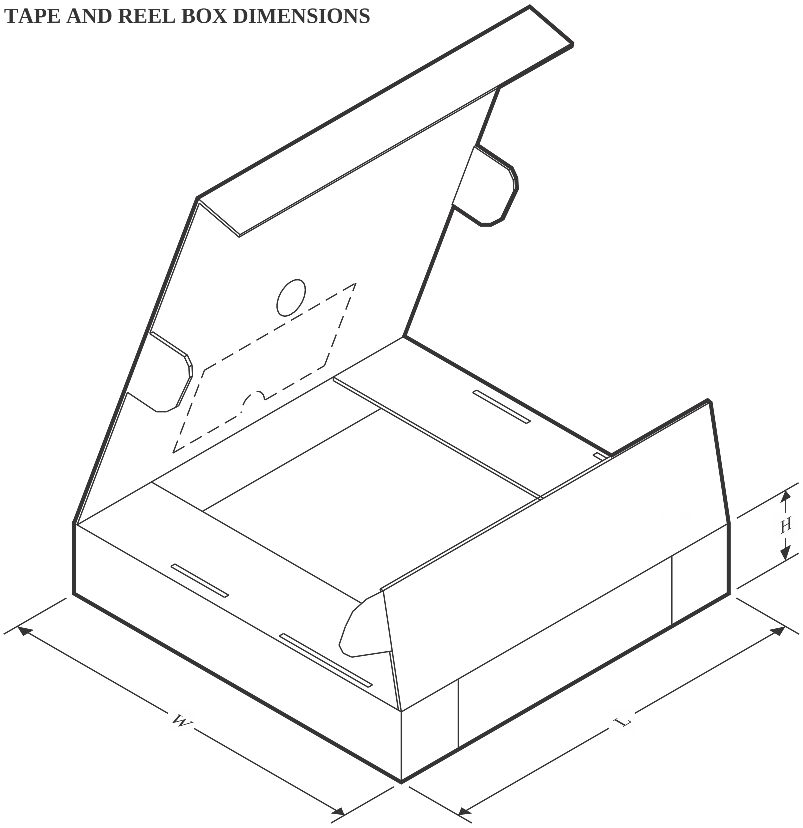
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC0820ACDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
TLC0820ACDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TLC0820AIDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

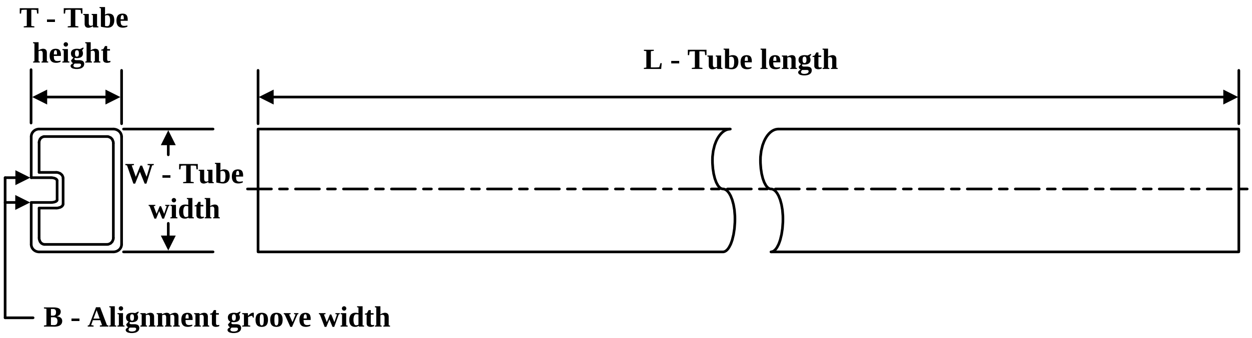
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC0820ACDBR	SSOP	DB	20	2000	350.0	350.0	43.0
TLC0820ACDWR	SOIC	DW	20	2000	350.0	350.0	43.0
TLC0820AIDWR	SOIC	DW	20	2000	350.0	350.0	43.0

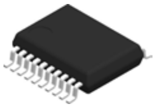
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC0820ACDB	DB	SSOP	20	70	530	10.5	4000	4.1
TLC0820ACDB.A	DB	SSOP	20	70	530	10.5	4000	4.1
TLC0820ACDW	DW	SOIC	20	25	506.98	12.7	4826	6.6
TLC0820ACDW.A	DW	SOIC	20	25	506.98	12.7	4826	6.6
TLC0820ACN	N	PDIP	20	20	506	13.97	11230	4.32
TLC0820ACN.A	N	PDIP	20	20	506	13.97	11230	4.32
TLC0820AIDW	DW	SOIC	20	25	506.98	12.7	4826	6.6
TLC0820AIDW.A	DW	SOIC	20	25	506.98	12.7	4826	6.6
TLC0820AIN	N	PDIP	20	20	506	13.97	11230	4.32
TLC0820AIN.A	N	PDIP	20	20	506	13.97	11230	4.32

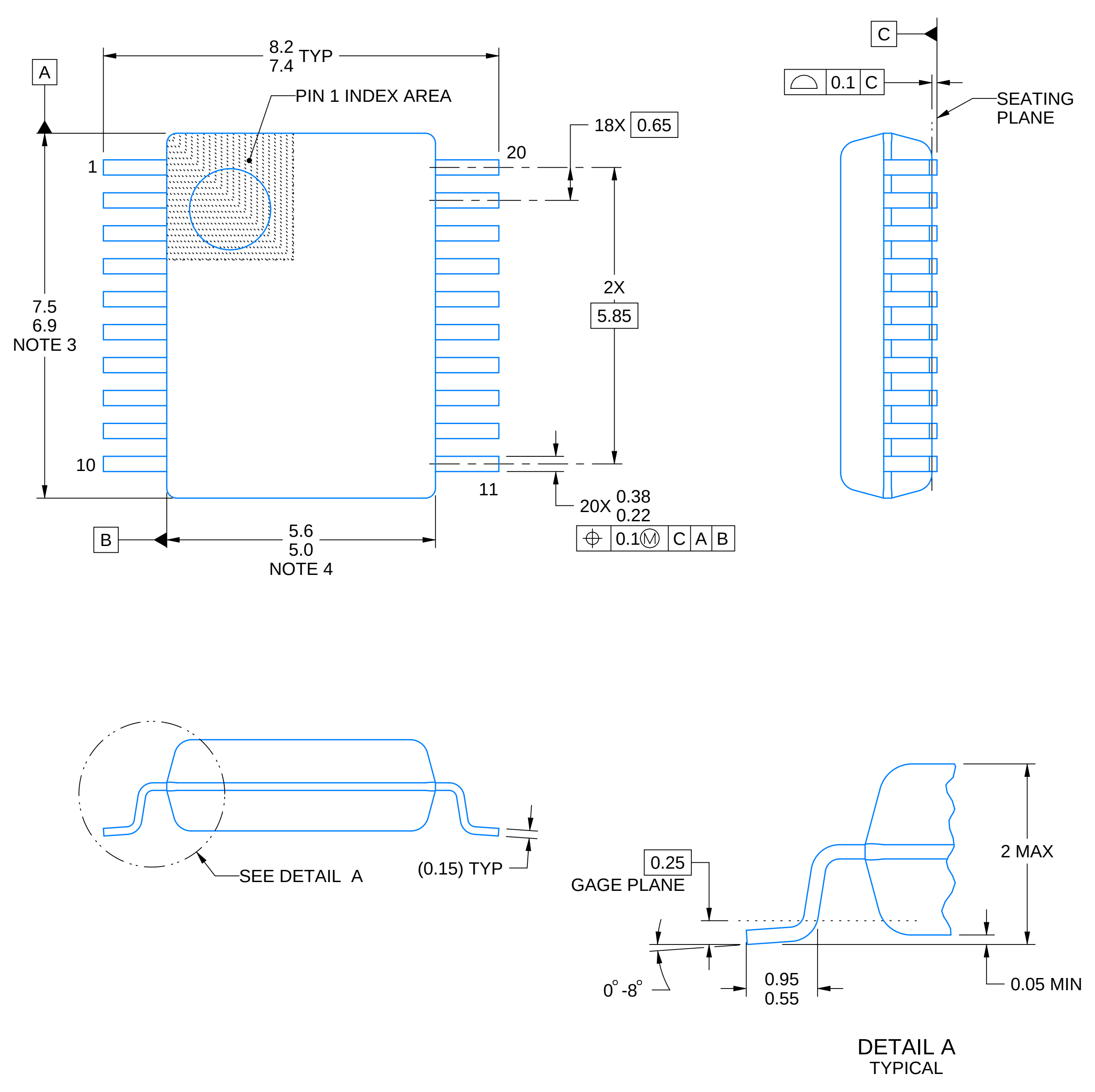
DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

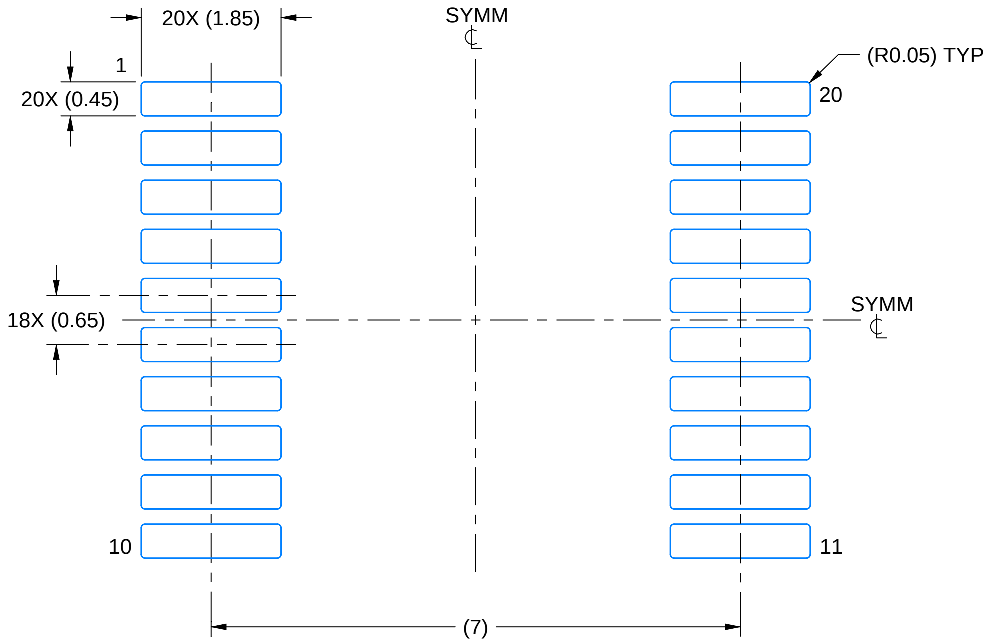
SMALL OUTLINE PACKAGE



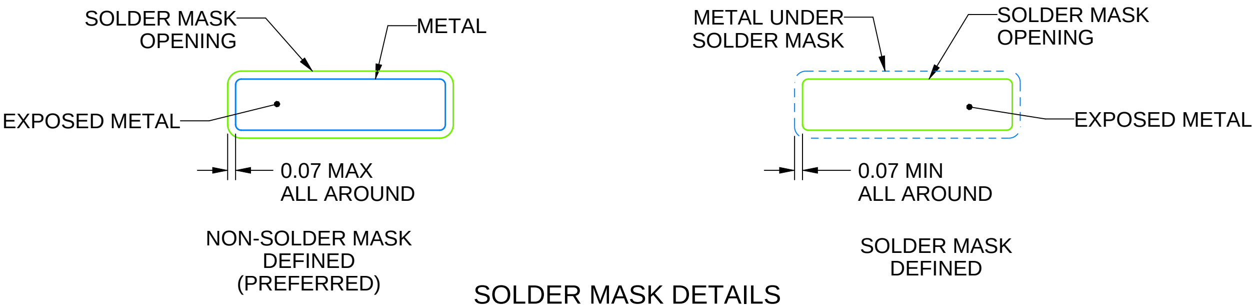
4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

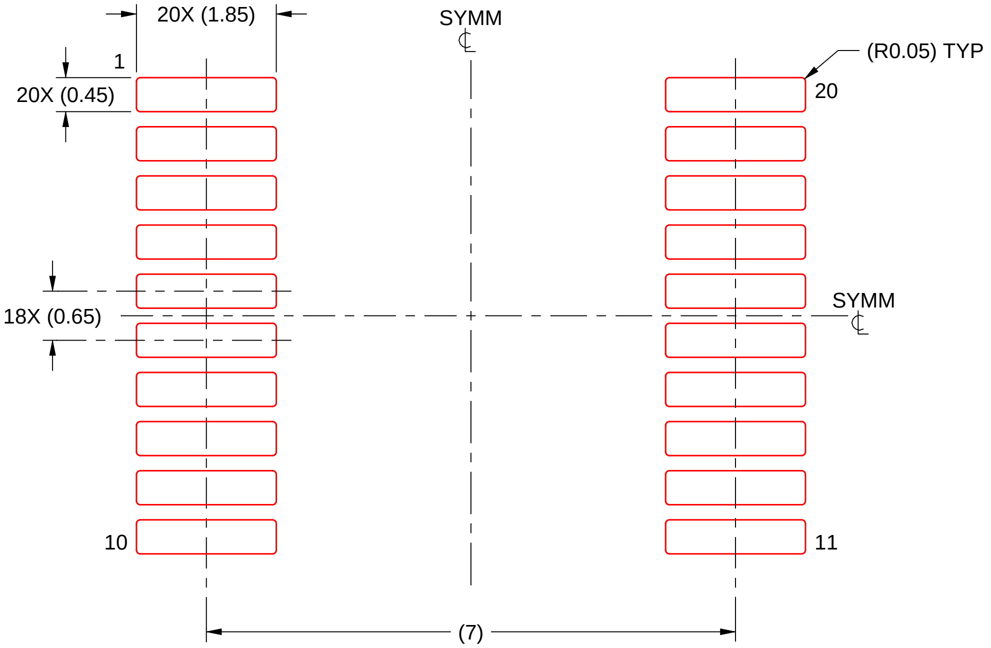


SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

NOTES: (continued)

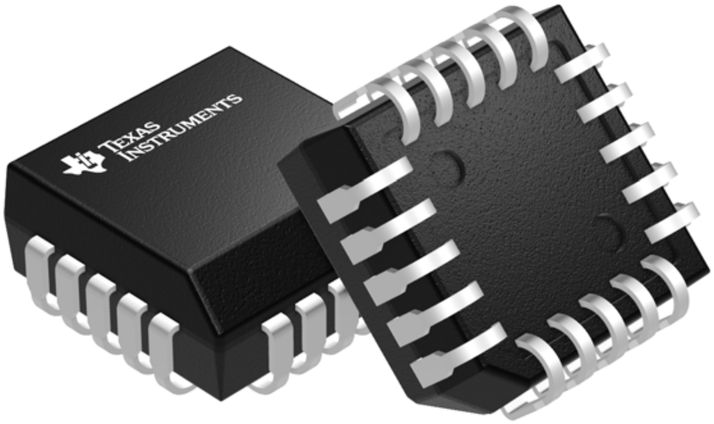
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

FN 20

PLCC - 4.57 mm max height

PLASTIC CHIP CARRIER



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

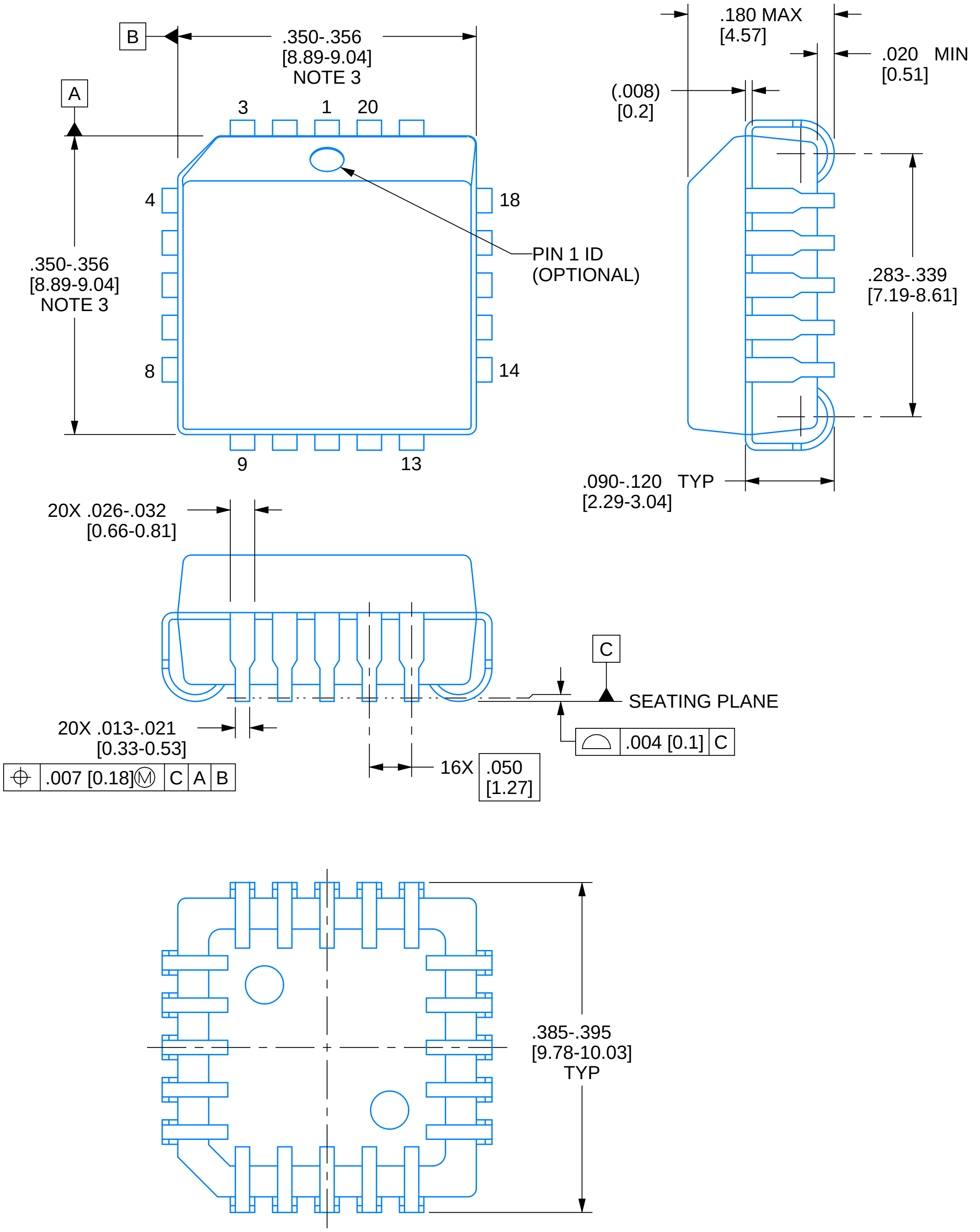
4040005-2/C

PACKAGE OUTLINE

FN0020A

PLCC - 4.57 mm max height

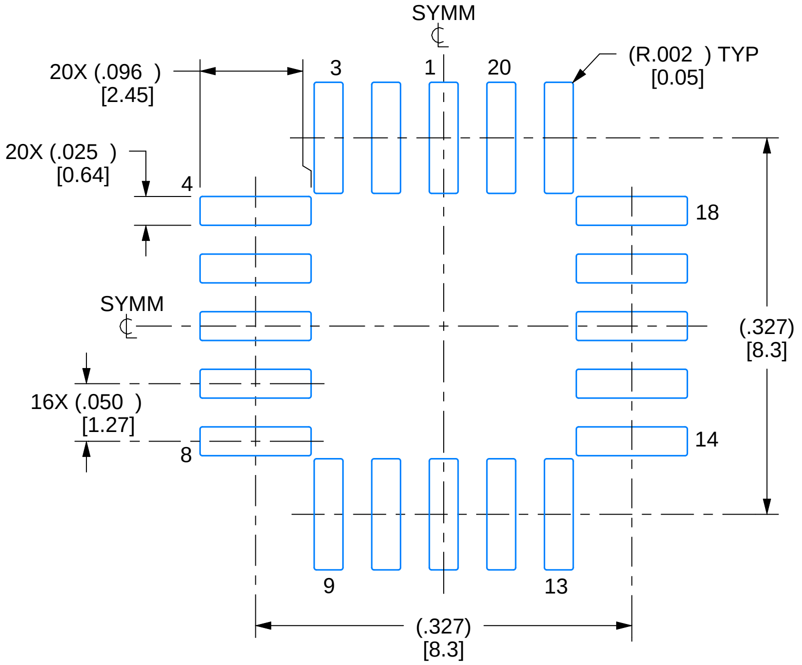
PLASTIC CHIP CARRIER



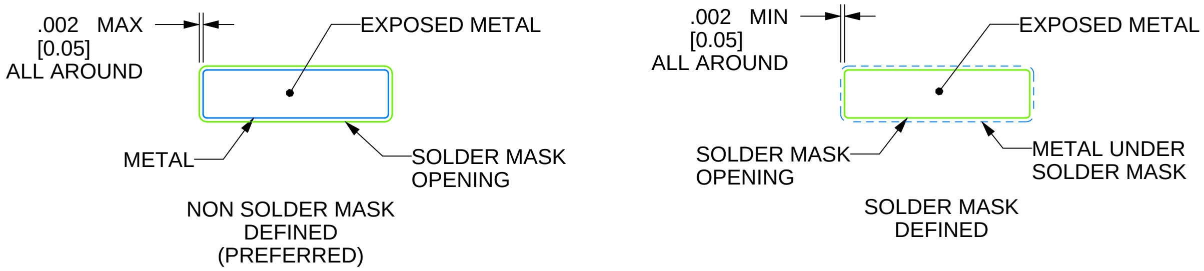
4215152/B 04/2017

NOTES:

1. All linear dimensions are in inches. Any dimensions in brackets are in millimeters. Any dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension does not include mold protrusion. Maximum allowable mold protrusion .01 in [0.25 mm] per side.
4. Reference JEDEC registration MS-018.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

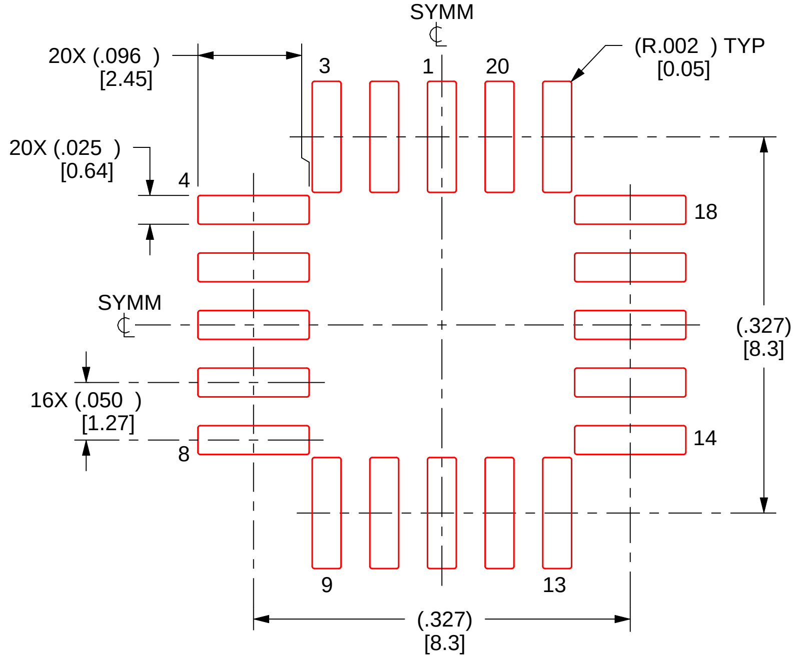


SOLDER MASK DETAILS

4215152/B 04/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

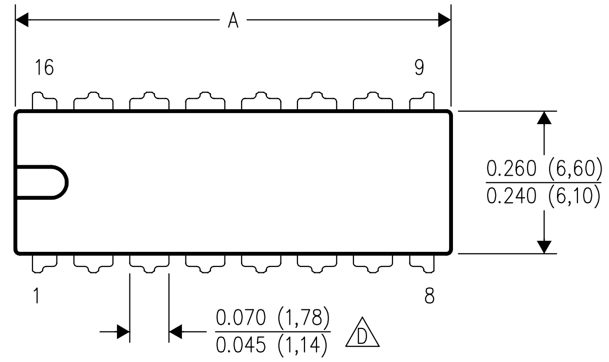
4215152/B 04/2017

NOTES: (continued)

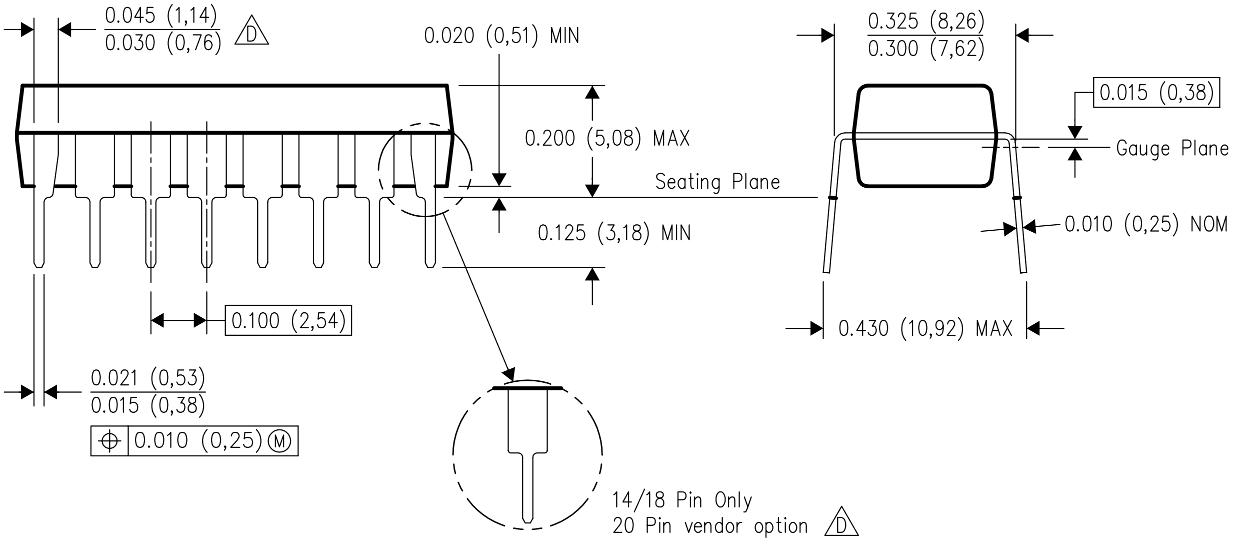
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

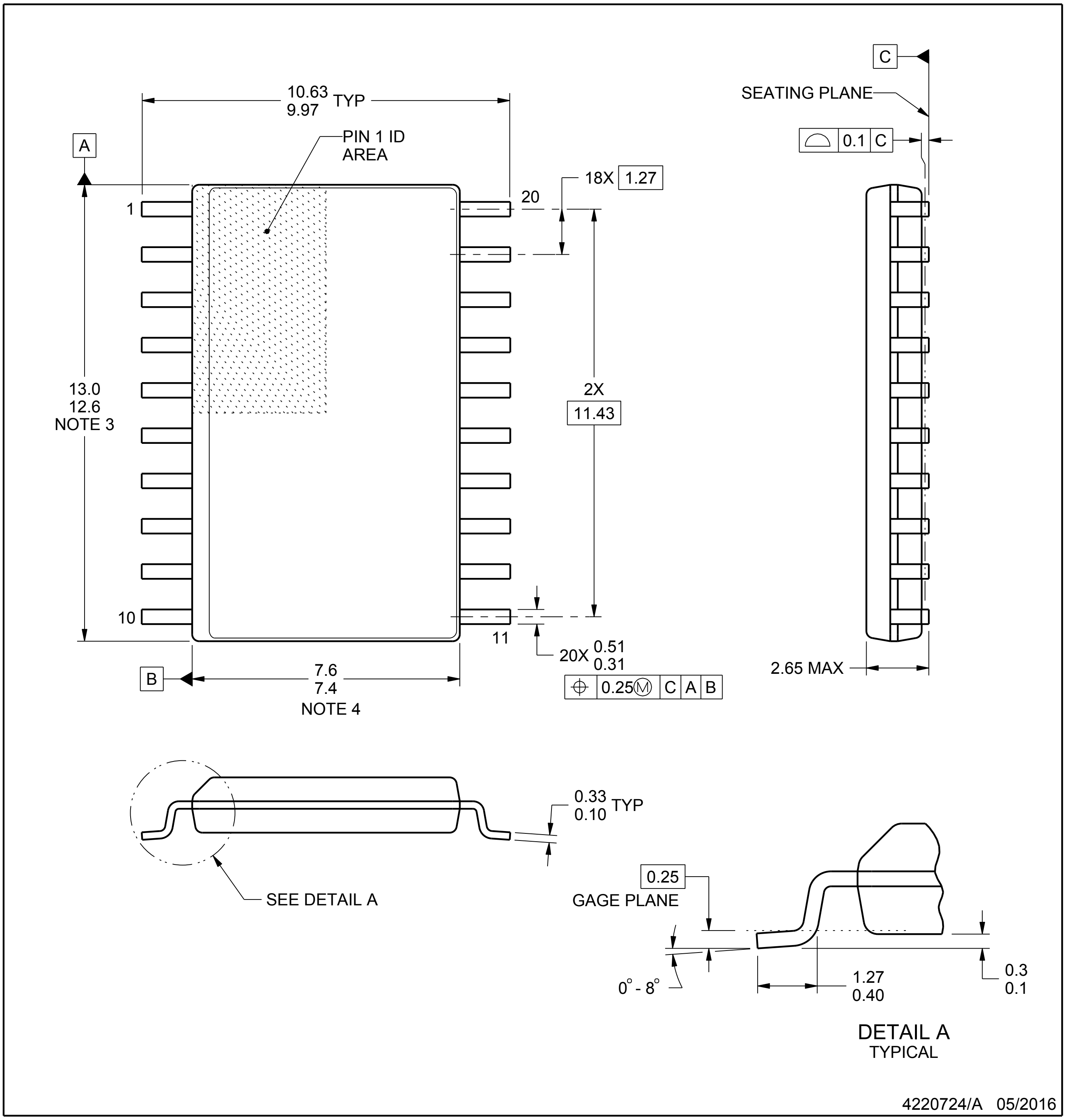


PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD



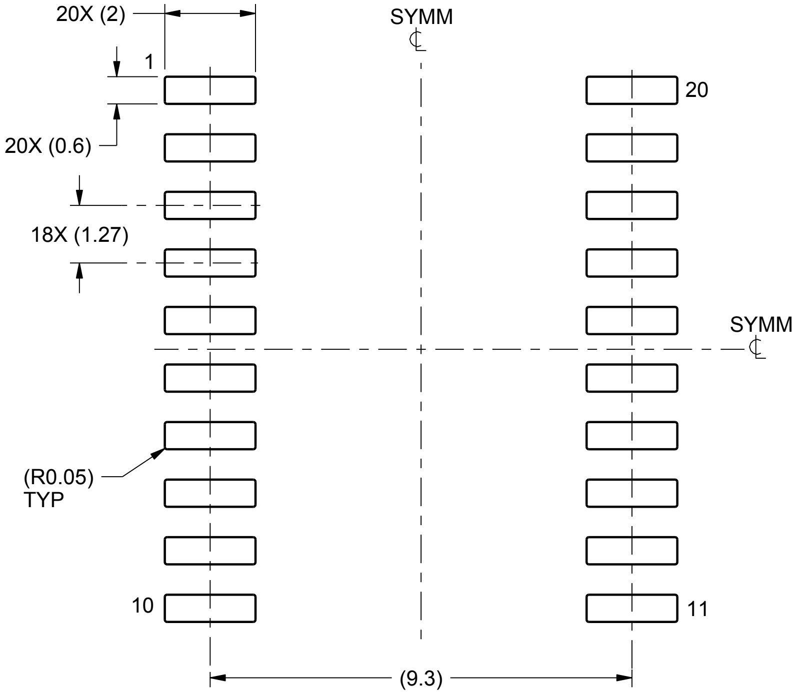
4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

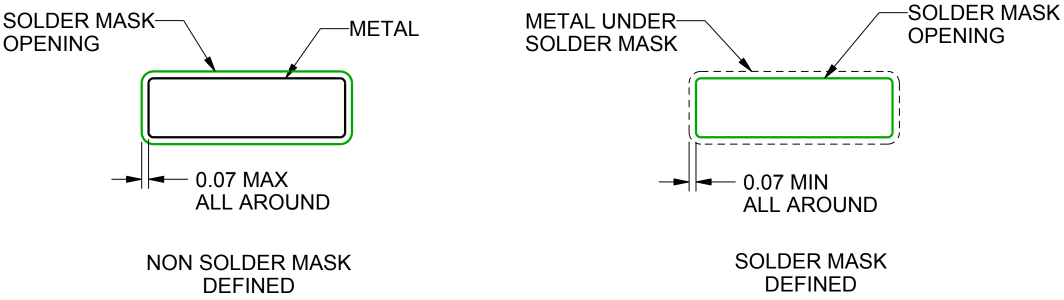


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

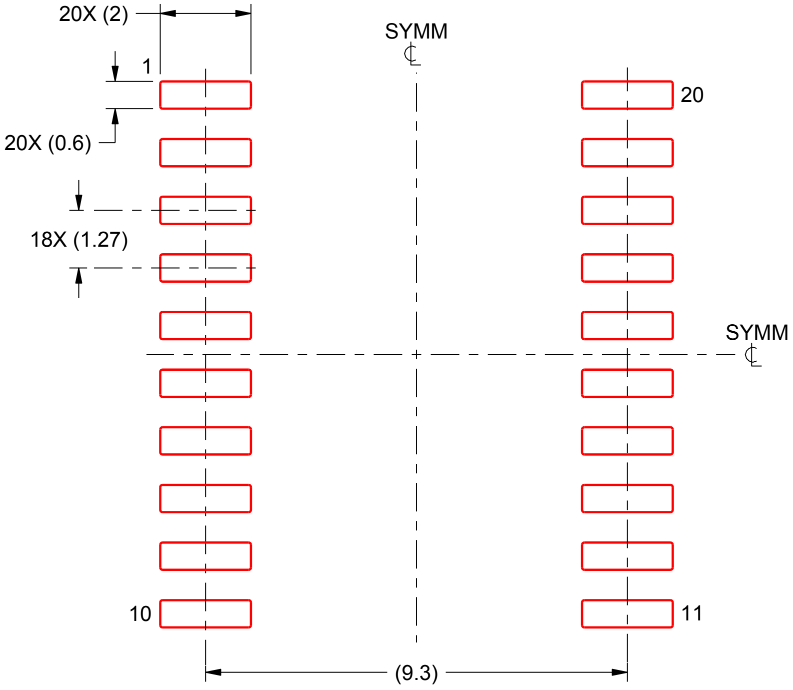


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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