

DS14C88 Quad CMOS Line Driver

Check for Samples: [DS14C88](#)

FEATURES

- Meets EIA-232D and CCITT V.28 Standards
- LOW Power Consumption
- Wide Power Supply Range: $\pm 5\text{V}$ to $\pm 12\text{V}$
- Available in SOIC Package

DESCRIPTION

The DS14C88, pin-for-pin compatible to the DS1488/MC1488, is a quad line drivers designed to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). This device translates standard TTL/CMOS logic levels to levels conforming to EIA-232-D and CCITT V.28 standards.

The device is fabricated in low threshold CMOS metal gate technology. The device provides very low power consumption compared to its bipolar equivalents: 500 μA (DS14C88) versus 25 mA (DS1488).

The DS14C88 simplifies designs by eliminating the need for external slew rate control capacitors. Slew rate control in accordance with EIA-232D is provided on-chip, eliminating the output capacitors.

Connection Diagram

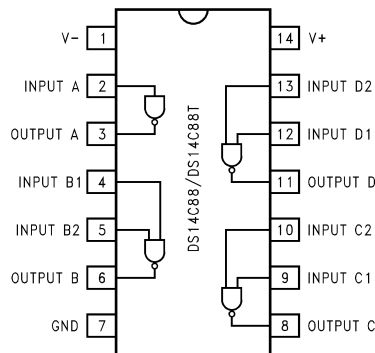


Figure 1. SOIC or PDIP Package- Top View
See Package Number NFF0014A or D0014A



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1998–2013, Texas Instruments Incorporated

Absolute Maximum Ratings⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

Supply Voltage	
V ⁺ Pin	+13V
V ⁻ Pin	-13V
Driver Input Voltage	(V ⁺) +0.3V to GND -0.3V
Driver Output Voltage	V ⁺ - V _O ≤ 30V
	V ⁻ - V _O ≤ 30V
Continuous Power Dissipation @+25°C ⁽⁵⁾	
NFF0014A Package	1513 mW
D0014A Package	1063 mW
Junction Temperature	+150°C
Lead Temperature (Soldering 4 seconds)	+260°C
Storage Temperature Range	-65°C to +150°C

- (1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be Ensured. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
- (3) This Product does not meet 2000V ESD rating.
- (4) ESD Rating (HBM, 1.5 kΩ, 100 pF) ≥ 1.0 kV.
- (5) Derate NFF0014A Package 12.1 mW/°C, and D0014A Package 8.5 mW/°C above +25°C.

Recommended Operating Conditions

	Min	Max	Units
V ⁺ Supply (GND = 0V)	+4.5	+12.6	V
V ⁻ Supply (GND = 0V)	-4.5	-12.6	V
Operating Free Air Temp. (T _A)			
DS14C88	0	+75	°C

Electrical Characteristics

Over Recommended Operating Conditions, unless otherwise specified

Parameter		Test Conditions		Min	Typ	Max	Units
I _{IL}	Maximum Low Input Current	V _{IN} = GND				+10	μA
I _{IH}	Maximum High Input Current	V _{IN} = V ⁺		-10			μA
V _{IL}	Low Level Input Voltage	V ⁺ ≥ +7V, V ⁻ ≤ -7V		GND		0.8	V
		V ⁺ < +7V, V ⁻ > -7V		GND		0.6	V
V _{IH}	High Level Input Voltage			2.0		V ⁺	V
V _{OL}	Low Level Output Level	V _{IN} = V _{IH} R _L = 3 kΩ or 7 kΩ	V ⁺ = 4.5V, V ⁻ = -4.5V		-4.0	-3.0	V
			V ⁺ = 9V, V ⁻ = 9V		-8.0	-6.5	V
			V ⁺ = 12V, V ⁻ = -12V		-10.5	-9.0	V
V _{OH}	High Level Output Level	V _{IN} = V _{IL} R _L = 3 kΩ or 7 kΩ	V ⁺ = 4.5V, V ⁻ = -4.5V	3.0	4.0		V
			V ⁺ = 9V, V ⁻ = -9V	6.5	8.0		V
			V ⁺ = 12V, V ⁻ = -12V	9.0	10.5		V
I _{OS+}	High Level Output Short Circuit Current ⁽¹⁾	V _{IN} = 0.8V, V _O = GND	V ⁺ = +12V, V ⁻ = -12V	-45			mA
I _{OS-}	Low Level Output Short Circuit Current ⁽¹⁾	V _{IN} = 2.0V, V _O = GND				+45	mA
R _{OUT}	Output Resistance	V ⁺ = V ⁻ = GND = 0V -2V ≤ V _O ≤ +2V ⁽²⁾ (Figure 2)		300			Ω

(1) I_{OS+} and I_{OS-} values are for one output at a time. If more than one output is shorted simultaneously, the device dissipation may be exceeded.

(2) Power supply (V⁺, V⁻) and GND pins are connected to ground for the Output Resistance Test (R_O).

Electrical Characteristics (continued)

Over Recommended Operating Conditions, unless otherwise specified

Parameter		Test Conditions		Min	Typ	Max	Units
I_{CC+}	Positive Supply Current	$V_{IN} = V_{ILmax}$ $R_L = OPEN$	$V^+ = 4.5V, V^- = -4.5V$			10	μA
			$V^+ = 9V, V^- = -9V$			30	μA
			$V^+ = 12V, V^- = -12V$			60	μA
		$V_{IN} = V_{IHmin}$ $R_L = OPEN$	$V^+ = 4.5V, V^- = -4.5V$			50	μA
			$V^+ = 9V, V^- = -9V$			300	μA
			$V^+ = 12V, V^- = -12V$			500	μA
I_{CC-}	Negative Supply Current	$V_{IN} = V_{ILmax}$ $R_L = OPEN$	$V^+ = 4.5V, V^- = -4.5V$			-10	μA
			$V^+ = 9V, V^- = -9V$			-10	μA
			$V^+ = 12V, V^- = -12V$			-10	μA
		$V_{IN} = V_{IHmin}$ $R_L = OPEN$	$V^+ = 4.5V, V^- = -4.5V$			-30	μA
			$V^+ = 9V, V^- = -9V$			-30	μA
			$V^+ = 12V, V^- = -12V$			-60	μA

Switching Characteristics⁽¹⁾⁽²⁾

Over Recommended Operating Conditions, unless otherwise specified (Figure 3, Figure 4)

Parameter		Test Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Low to High	$V^+ = +4.5V, V^- = -4.5V$			1.5	6.0	μs
		$V^+ = +9.0V, V^- = -9.0V$			1.2	5.0	μs
		$V^+ = +12V, V^- = -12V$			1.2	4.0	μs
t_{PHL}	Propagation Delay High to Low	$V^+ = +4.5V, V^- = -4.5V$			1.5	6.0	μs
		$V^+ = +9.0V, V^- = -9.0V$			1.35	5.0	μs
		$V^+ = +12V, V^- = -12V$			1.3	4.0	μs
t_r	Rise Time ⁽³⁾			0.2	1.0		μs
t_f	Fall Time ⁽³⁾			0.2	1.0		μs
t_{sk}	Typical Propagation Delay Skew	$V^+ = +4.5V, V^- = -4.5V$			250		ns
		$V^+ = +9.0V, V^- = -9.0V$			200		ns
		$V^+ = +12V, V^- = -12V$			150		ns
S_R	Output Slew Rate ⁽³⁾	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$ $C_L = 15\text{ pF}$ to 2500 pF				30	V/ μs

(1) AC input test waveforms for test purposes: $t_r = t_f \leq 20\text{ ns}$, $V_{IH} = 2V$, $V_{IL} = 0.8V$ ($0.6V$ at $V^+ = 4.5V, V^- = -4.5V$)

(2) Input rise and fall times must not exceed $5\text{ }\mu s$.

(3) The output slew rate, rise time, and fall time are measured from the $+3.0V$ to the $-3.0V$ level on the output waveform.

Parameter Measure Information

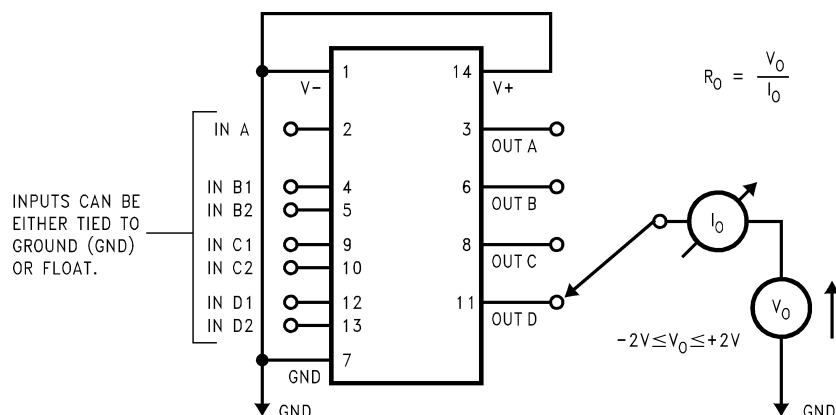


Figure 2. Output Resistance Test Circuit (Power-Off)

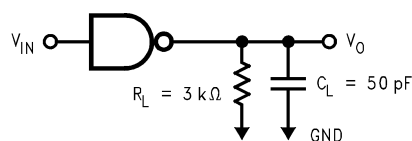


Figure 3. Driver Load Circuit⁽⁴⁾

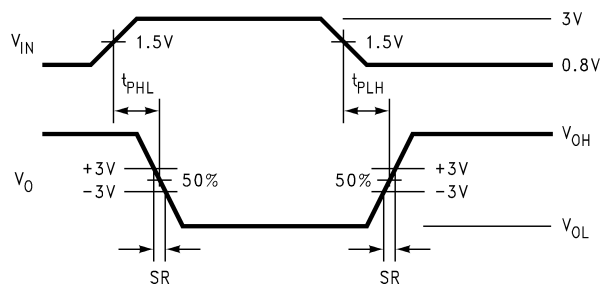


Figure 4. Driver Switching Waveform

(4) C_L include jig and probe capacitances.

TYPICAL APPLICATION INFORMATION

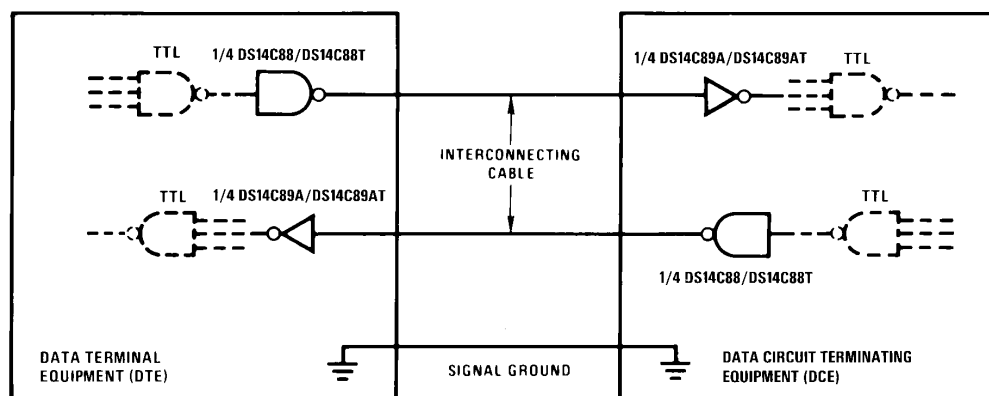


Figure 5. EIA-232D Data Transmission

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	4

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS14C88M/NOPB	Active	Production	SOIC (D) 14	55 TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	DS14C88M
DS14C88M/NOPB.A	Active	Production	SOIC (D) 14	55 TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	DS14C88M
DS14C88M/NOPB.B	Active	Production	SOIC (D) 14	55 TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	DS14C88M
DS14C88MX/NOPB	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	DS14C88M
DS14C88MX/NOPB.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	DS14C88M
DS14C88MX/NOPB.B	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	DS14C88M

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS14C88MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS14C88MX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
DS14C88M/NOPB	D	SOIC	14	55	495	8	4064	3.05
DS14C88M/NOPB.A	D	SOIC	14	55	495	8	4064	3.05
DS14C88M/NOPB.B	D	SOIC	14	55	495	8	4064	3.05

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

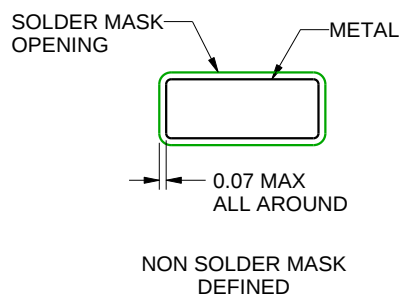
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated