

# FDP80N06

## N-Channel MOSFET

60V, 80A, 10mΩ

### Features

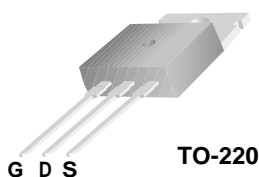
- $R_{DS(on)} = 8.5m\Omega$  (Typ.) @  $V_{GS} = 10V$ ,  $I_D = 40A$
- Low gate charge (Typ. 57nC)
- Low  $C_{rss}$  (Typ. 145pF)
- Fast switching
- Improved dv/dt capability
- RoHS compliant



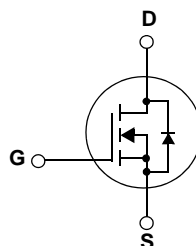
### Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pluse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies, active power factor correction, electronic lamp ballast based on half bridge topology.



TO-220



### MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted\*

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain to Source Voltage	60	V
$V_{GSS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ C$ )	A
		- Continuous ( $T_C = 100^\circ C$ )	
$I_{DM}$	Drain Current	- Pulsed (Note 1)	A
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	mJ
$I_{AR}$	Avalanche Current	(Note 1)	A
$E_{AR}$	Repetitive Avalanche Energy	(Note 1)	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	V/ns
$P_D$	Power Dissipation	( $T_C = 25^\circ C$ )	W
		- Derate above $25^\circ C$	W/ $^\circ C$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +175	$^\circ C$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ C$

\*Drain current limited by maximum junction temperature

### Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.85	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	

**Package Marking and Ordering Information**  $T_C = 25^\circ\text{C}$  unless otherwise noted

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP80N06	FDP80N06	TO-220	-	-	50

**Electrical Characteristics**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$ , $T_J = 25^\circ\text{C}$	60	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	0.075	-	$V/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{V}$ , $V_{GS} = 0\text{V}$ $V_{DS} = 48\text{V}$ , $T_C = 150^\circ\text{C}$	-	-	1 10	$\mu\text{A}$
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{V}$ , $V_{DS} = 0\text{V}$	-	-	$\pm 100$	nA

**On Characteristics**

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}$ , $I_D = 40\text{A}$	-	8.5	10	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 25\text{V}$ , $I_D = 40\text{A}$ (Note 4)	-	67	-	S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{V}$ , $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	2450	3190	pF
$C_{oss}$	Output Capacitance		-	910	1190	pF
$C_{rss}$	Reverse Transfer Capacitance		-	145	190	pF

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\text{V}$ , $I_D = 80\text{A}$ $R_G = 25\Omega$ (Note 4, 5)	-	32	75	ns
$t_r$	Turn-On Rise Time		-	259	528	ns
$t_{d(off)}$	Turn-Off Delay Time		-	136	282	ns
$t_f$	Turn-Off Fall Time		-	113	236	ns
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 48\text{V}$ , $I_D = 80\text{A}$ $V_{GS} = 10\text{V}$ (Note 4, 5)	-	57	74	nC
$Q_{gs}$	Gate to Source Gate Charge		-	15	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	24	-	nC

**Drain-Source Diode Characteristics**

I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		-	-	80	A
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	320	A
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 80A	-	-	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 80A	-	64	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI <sub>F</sub> /dt = 100A/μs (Note 4)	-	127	-	nC

**Notes:**

- 1: Repetitive Rating: Pulse width limited by maximum junction temperature
- 2:  $L = 0.15\text{mH}$ ,  $I_{AS} = 80\text{A}$ ,  $V_{DD} = 50\text{V}$ ,  $R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$
- 3:  $I_{SD} \leq 80\text{A}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
- 4: Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$
- 5: Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

Figure 1. On-Region Characteristics

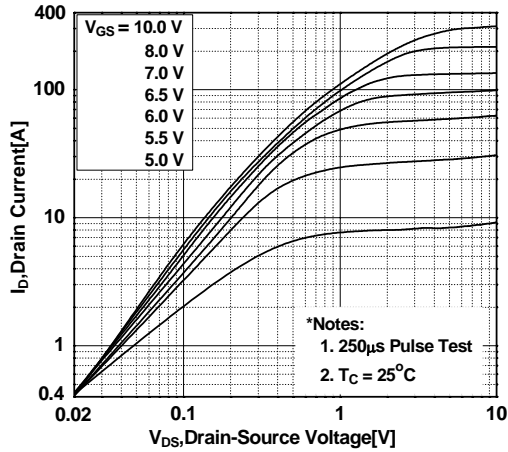


Figure 2. Transfer Characteristics

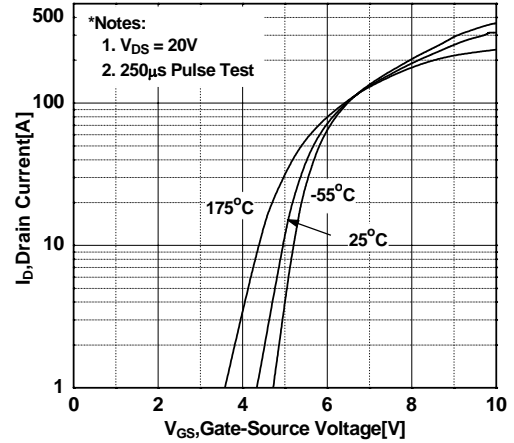


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

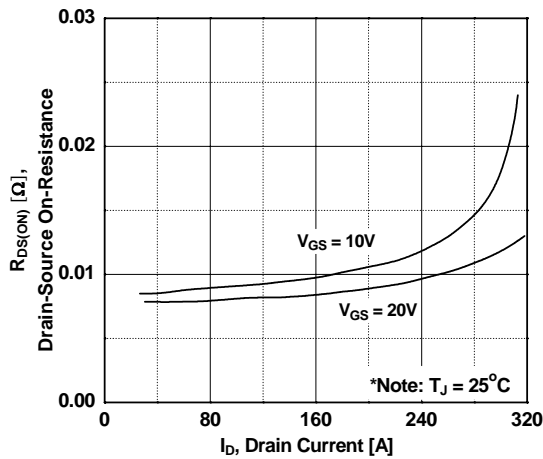


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

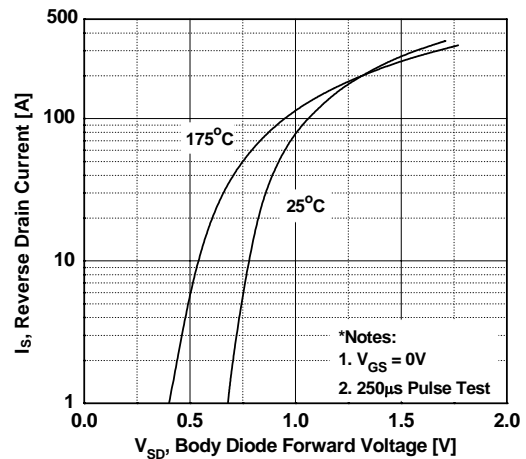


Figure 5. Capacitance Characteristics

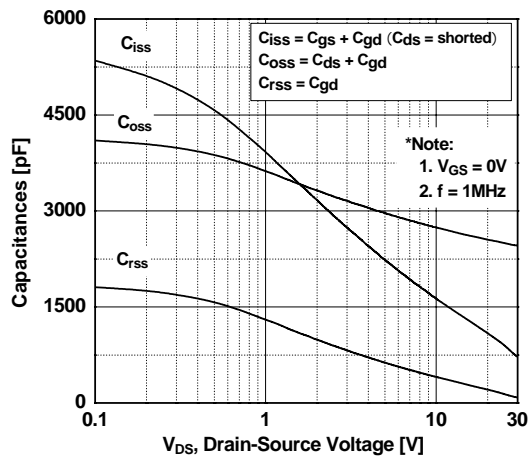
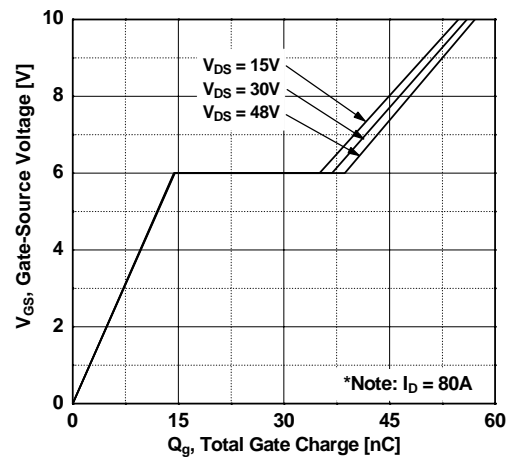


Figure 6. Gate Charge Characteristics



# Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

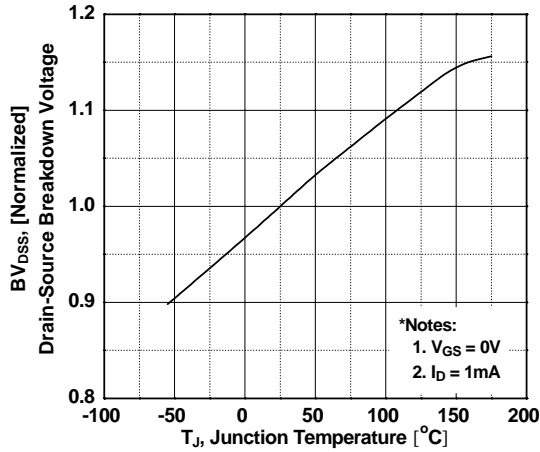


Figure 8. On-Resistance Variation vs. Temperature

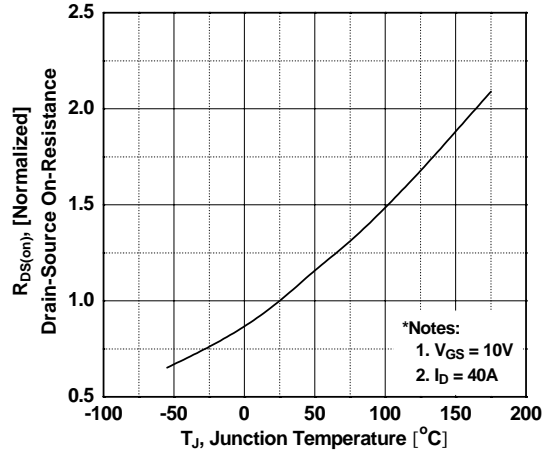


Figure 9. Maximum Safe Operating Area

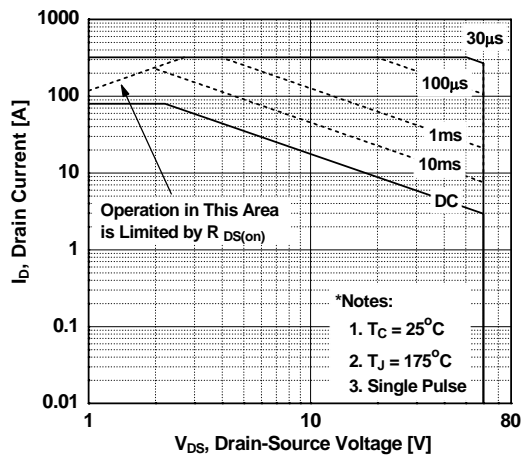


Figure 10. Maximum Drain Current vs. Case Temperature

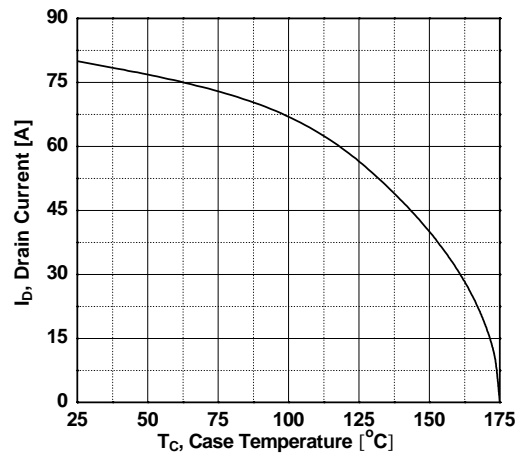
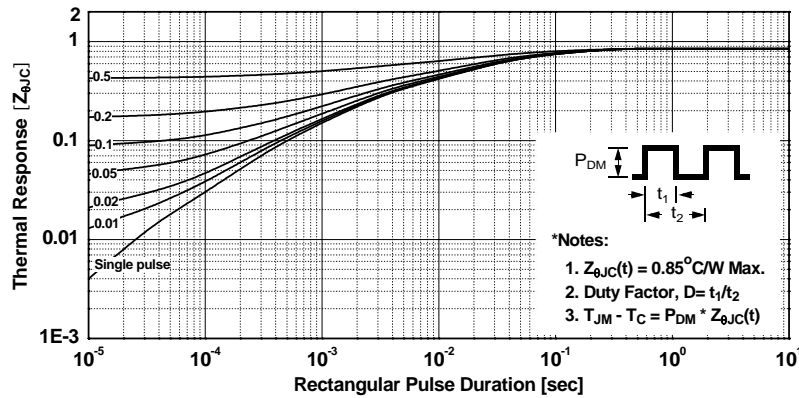
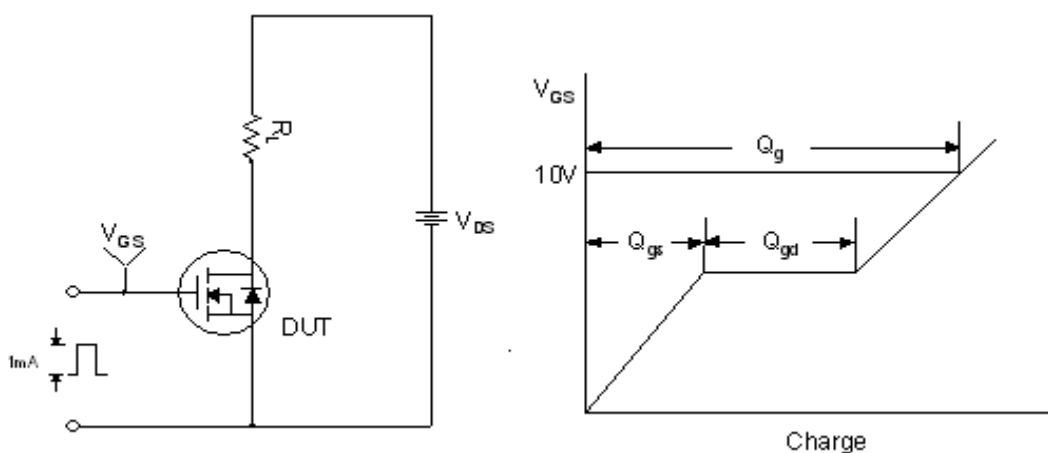


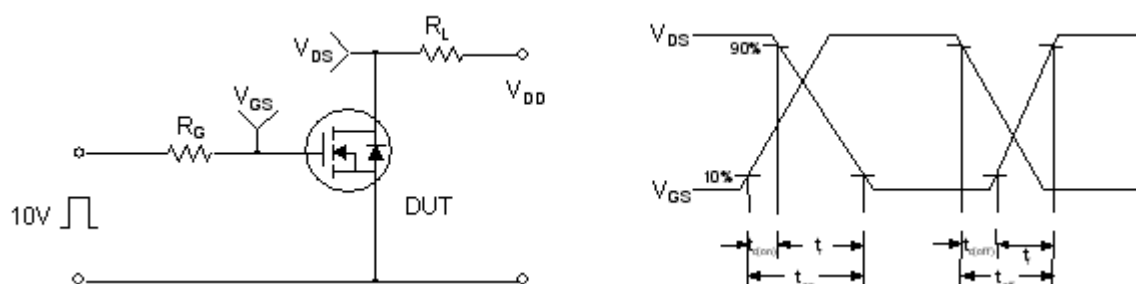
Figure 11. Transient Thermal Response Curve



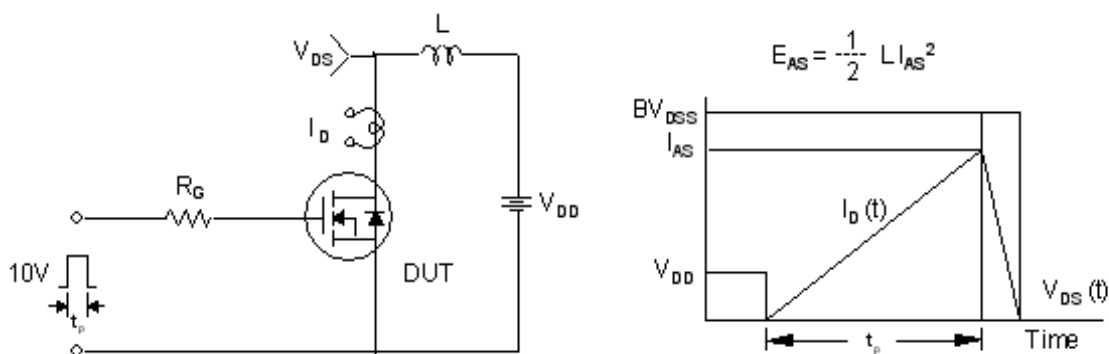
Gate Charge Test Circuit & Waveform



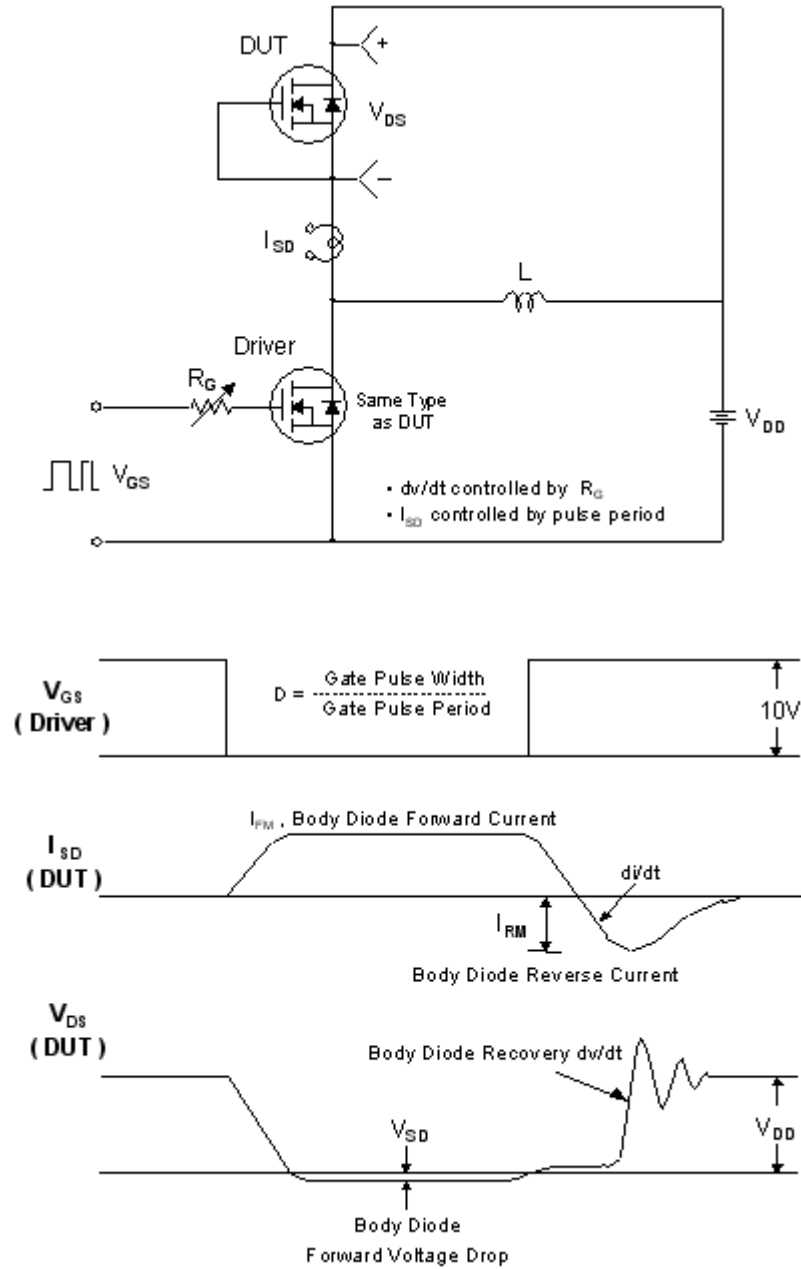
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

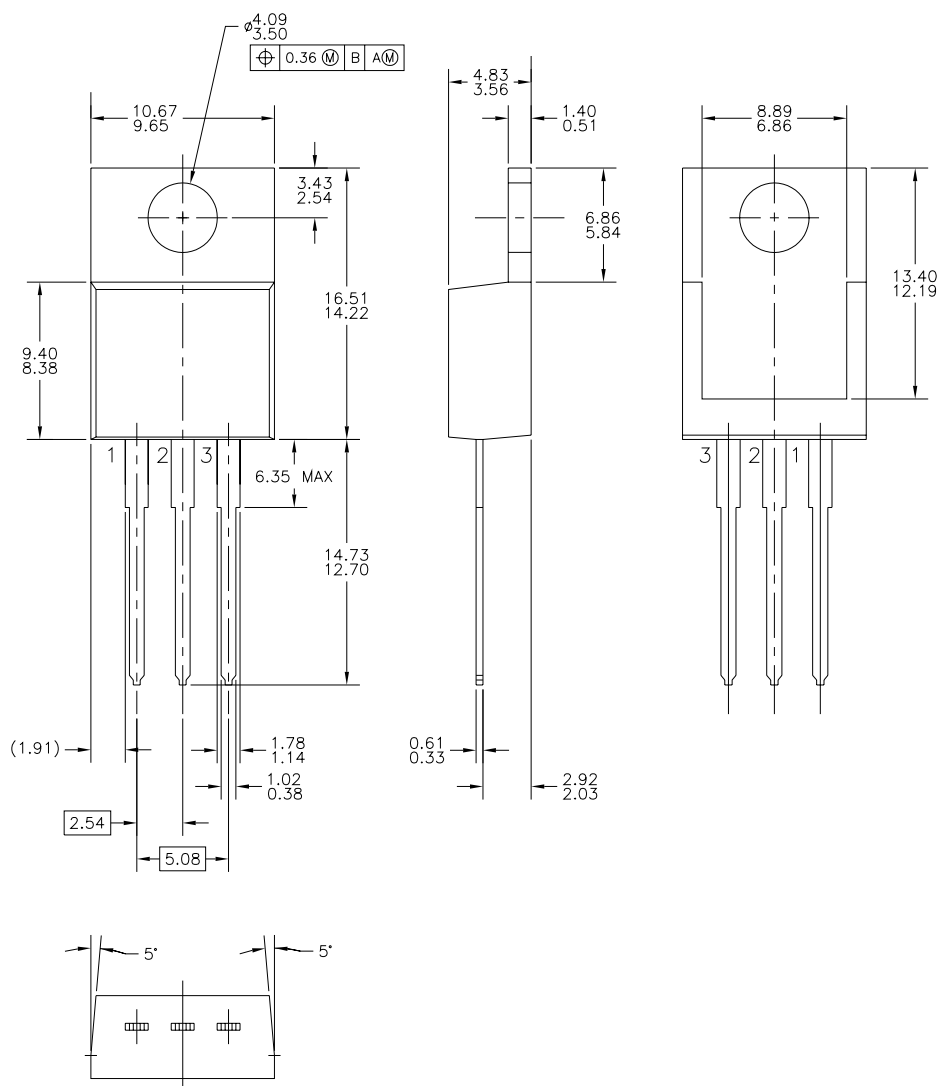


# Peak Diode Recovery dv/dt Test Circuit & Waveforms



## Mechanical Dimensions


## TO-220



### Dimensions in Millimeters

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