NO.84-12 1

T-51-09-16

YM3014

Serial Input Floating D/A Converter (DAC-SS)

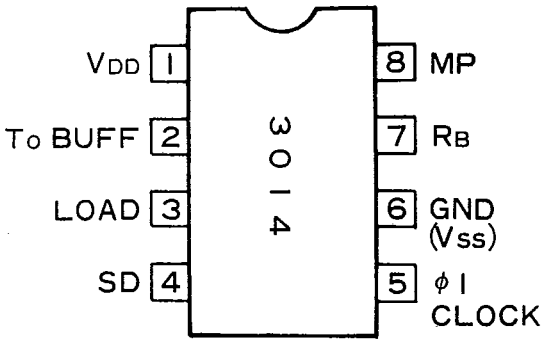
■ OUTLINE

YM3014: DAC-SS (hereinafter referred to as DAC) is a floating D/A converter with serial input for single channel. It can generate analog output (dynamic range 16 bits) having 10-bit mantissa section and 3-bit exponent section on the basis of input digital signal.

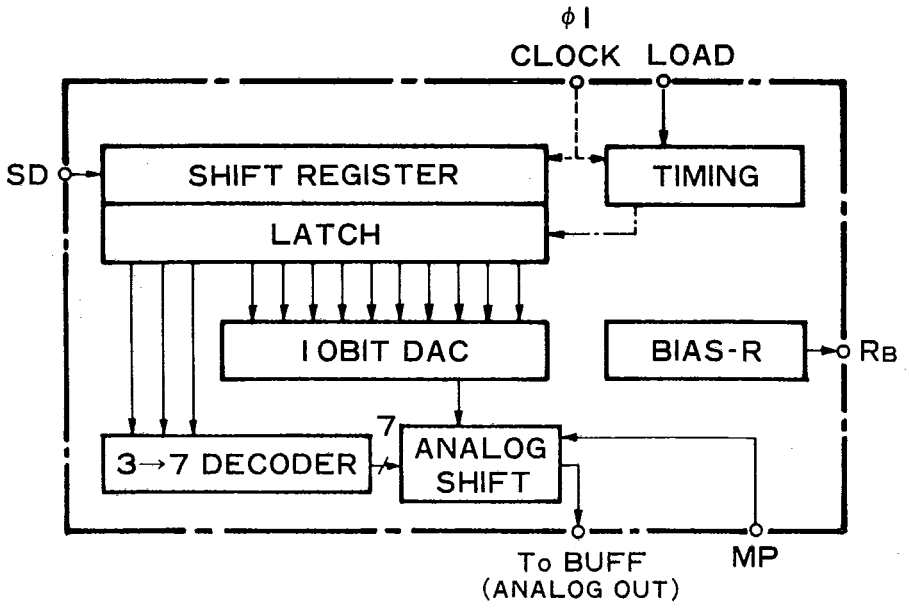
■ FEATURES

- An external buffer operational amplifier is provided to obtain analog output easily.
- A wide dynamic range with 16 bits.
- Sample holding circuit is unnecessary.
- It is possible to reduce noise and the distortion rate of high harmonic and to obtain good temperature characteristics.
- It is produced by the monolithic process with high precision thin film resistance and CMOS and contained in a 8 pin plastic DIL package.

■ TERMINAL DIAGRAM



■ BLOCK DIAGRAM



■ DESCRIPTION OF TERMINAL FUNCIOTNS

PIN NO.	SYMBOL NAME	FUNCTIONS
1	VDD	Reference power sourch on the high potential side.
2	To BUFF	Analog output from DAC is input into a buffer operational amplifier.
3	LOAD	Generates in ternal signal to latch the serial data by use of trailing edge.
4	SD	Serial input of the converted digital siganl.
5	CLOCK	Clock (ϕ 1) to operate the shift register and timing generator.
6	VSS	Power source on the low potential side (GND).
7	RB	High precision 1/2 VDD voltage generated inside of the unit is obtained at this terminal. It is added to 8 pin through the buffer operational amplifier.
8	MP	Exponential analog value is obtained by S signal with reference to potential given to MP. Normally it is biased to 1/2VDD.

■ DESCRIPTION OF FUNCTIONS

1. Relationship between Digital Input Data and Analog Output Voltage

To perform one conversion at 16-bit time by YM3014, the first 3-bit data among the 16-bit serial data is processed as invalid data in the DAC. The next 10 bit data (D_0 through D_9) is input into the 10-bit DAC section as the MSB data from the LSB to constitute the mantissa section of analog output. The remaining 3-bit data (S_0 through S_2) is input into the 2^{-N} analog shift section to constitute the exponent section of analog output.

For example, when the basic circuit is used, output voltage is as follows.

$$Vour = 1/2\ V_{DD} + 1/4\ V_{DD}\ (-1 + D_9 + D_8 2^{-1} + \cdots D_0 2^{-9} + 2^{-10}) 2^{-N}$$

$$N = S_2 2^2 + S_1 2^1 + S_0$$

$S_2 = S_1 = S_0 = 0$: not allowed.

That is, it has the maximum aplitude of ± 1/4VDD and the minimum amplitude of ± $1/4V_{DD}\ 2^{-16}$ with 1/2VDD potential in the center.

2. Operation in the DAC

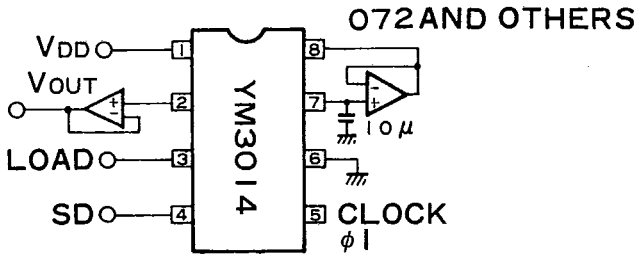
Digital input data is taken into the shift register through SD terminal in synchronous with the clock rise. Latch signal is generated in the timing circuit by use of the trailing edge of LOAD. By this latch signal, the serial data of D_0 through D_9 and S_0 through S_2 is latched, which drives the 10-bit DAC section and the analog shift section, respectively, to start conversion.

Its analog output is obtained at the terminal "TO BUTT". It can be output through an adequate buffer operational amplifier.

3. Summary of Operation

- As shown in Fig. 3, Timing diagram, coincide the trailing edge of LOAD with the timing of the S_2 rear end of the SD signal. "H" time of LOAD requires more than one bit time.
- Conversion at the bit time other than 16 bits is possible by increasing or decreasing the invalid bit number part.

■ EXAMPLE OF BASIC CIRCUIT



■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Rating

ITEM	RATING	UNIT
Supply voltage	−0.3 ~ +15.0	V
High level input voltage	VDD + 0.3	V
Low level input voltage	VSS − 0.3	V
Ambient operating temperature	0 ~ 70	°C
Storage temperature	−50 ~ +125	°C

2. Recommended Operation Conditions

ITEM	SYMBOL	MIN.	STD.	MAX.	UNIT
Supply voltage	VDD VSS	+4.75 0	5.0 0	10.0 0	V V
Input signal voltage	CLOCK SD LOAD	0	–	VDD	V
Ambient operation temperature	Ta	0	–	70	°C

3. D.C. Characteristics

ITEM	SYMBOL	MEASUREMENT CONDITIONS	MIN.	STD.	MAX.	UNIT
High level input voltage	VIH	VDD= 5.0V	3.3	–	–	V
Low level input voltage	VIL	VDD= 5.0V	–	–	1.5	V
Input current	IIN	VDD= 10.0V	–	–	10^{-3}	μA
Analog output voltage	VOUT	VDD= 5.0V	–	–	2.5	Vp − p
Power current	IDD	VDD= 5.0V	–	–	6	mA

4. AC Characteristics

ITEM	SYMBOL	CONDITIONS	MIN.	STD.	MAX.	UNIT
• Clock Frequency	fc		0.65	0.8	2.6	MHz
High level time	TH		180			ns
Rise time	Tr				50	ns
Breaking time	Tf				50	ns
• Data Set-up time	TDS	SD LOAD	0			
Rise time	Tr				50	ns
Breaking time	Tf				50	ns

5. Capacity

ITEM	SYMBOL	CONDITIONS	MIN.	STD.	MAX.	UNIT
Input capacity	CIN		–	–	5	PF

6. DAC Characteristics

ITEM	SYMBOL	CONDITIONS	MIN.	STD.	MAX.	UNIT
Max. out put amplitude	VOUT			1/2 VDD		Vpp
Resolution				16		Bit
Settling time	Ts			4		μsec
Total distortion rate of high harmonic	THD1 THD6	VDD= 5V, 110Hz level 0 dB – 36dB		0.05	0.2 0.2	% %
Noise				– 92	– 80	dBm
Temperature characteristics		Out put voltage Total distortion rate of high hermonic		5		ppm/°C

7. Timind Diagram

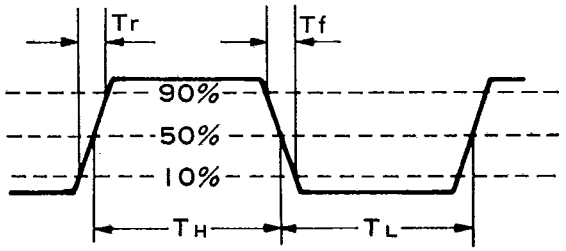


Fig. 1 Data timing

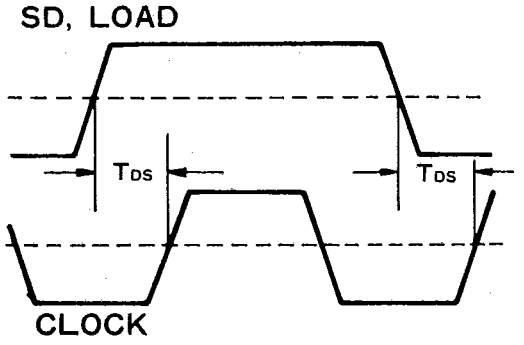


Fig. 2 Input data clock timing

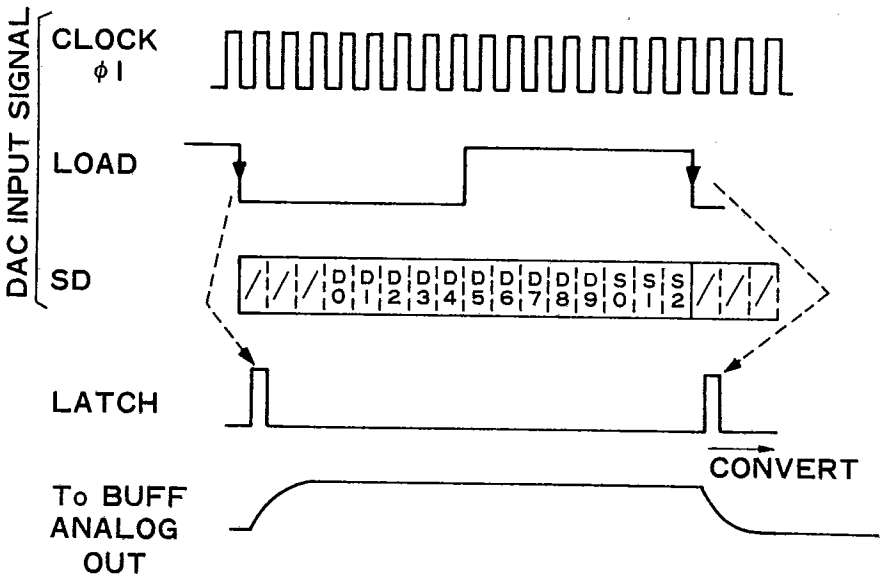
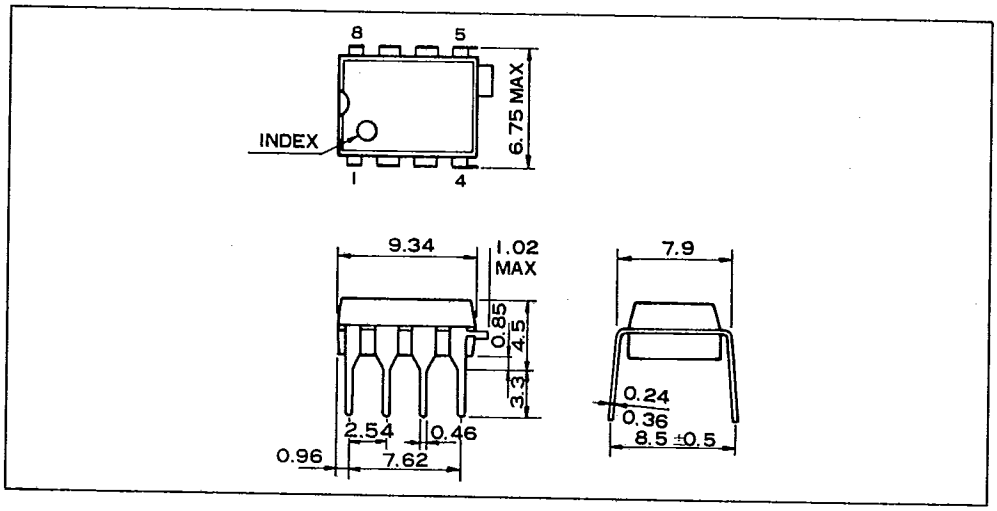


Fig. 3 YM3014 timing

■ OUTER DIMENSION DRAWING



The specifications of this product are subject to improvement changes without prior notice.

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