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# HMC540LP3 / 540LP3E

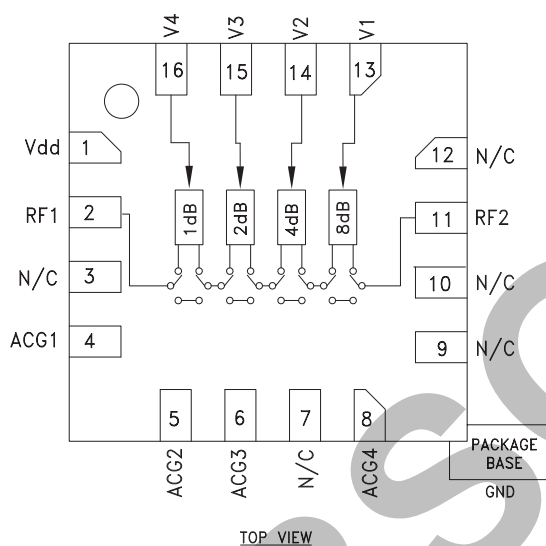
**1 dB LSB GaAs MMIC 4-BIT DIGITAL  
POSITIVE CONTROL ATTENUATOR, DC - 5.5 GHz**

## Typical Applications

The HMC540LP3 / HMC540LP3E is ideal for both RF and IF applications:

- Cellular Infrastructure
- ISM, MMDS, WLAN, WiMAX, WiBro
- Microwave Radio & VSAT
- Test Equipment and Sensors

## Functional Diagram



## Features

- 1 dB LSB Steps to 15 dB
- ± 0.2 dB Typical Step Error
- Low Insertion Loss: 1 dB
- High IP3: +50 dBm
- Single Control Line Per Bit
- TTL/CMOS Compatible Control
- Single +5V Supply
- 3x3 mm SMT Package

## General Description

The HMC540LP3 & HMC540LP3E are broadband 4-bit GaAs IC digital attenuators in low cost leadless surface mount packages. This single positive control line per bit digital attenuator utilizes off chip AC ground capacitors for near DC operation, making it suitable for a wide variety of RF and IF applications. Covering DC to 5.5 GHz, the insertion loss is less than 1 dB typical. The attenuator bit values are 1 (LSB), 2, 4 and 8 dB for a total attenuation of 15 dB. Attenuation accuracy is excellent at ± 0.2 dB typical step error. The attenuator also features a IIP3 of +50 dBm. Four TTL/CMOS control inputs are used to select each attenuation state. A single Vdd bias of +5V is required.

## Electrical Specifications,

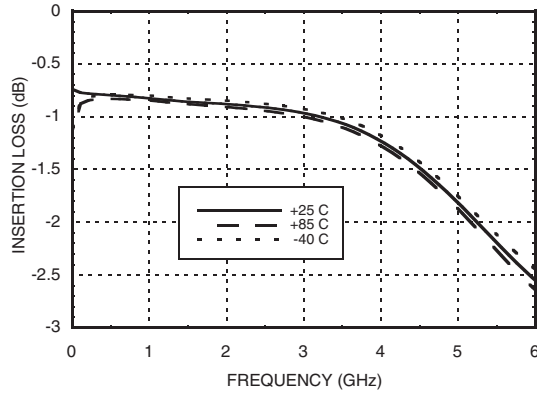
$T_A = +25^\circ \text{C}$ , With  $V_{dd} = +5\text{V}$  &  $V_{ctl} = 0/+5\text{V}$  (Unless Otherwise Noted)

| Parameter  | Frequency (GHz) | Min.                                | Typ. | Max. | Units |
|--|-----------------|-------------------------------------|------|------|-------|
| Insertion Loss   | DC - 2.0 GHz    |                                     | 0.8  | 1.1  | dB    |
|  | 2.0 - 3.0 GHz   |                                     | 1.0  | 1.3  | dB    |
|  | 3.0 - 4.0 GHz   |                                     | 1.3  | 1.6  | dB    |
|  | 4.0 - 5.5 GHz   |                                     | 2.2  | 2.6  | dB    |
| Attenuation Range  | DC - 5.5 GHz    |                                     | 15   |      | dB    |
| Return Loss (RF1 & RF2, All Atten. States)                                   | DC - 3.5 GHz    |                                     | 20   |      | dB    |
|  | 3.5 - 5.5 GHz   |                                     | 15   |      | dB    |
| Attenuation Accuracy:<br>(Referenced to Insertion Loss)                      | DC - 1.0 GHz    | ± (0.2 + 2% of Atten. Setting) Max. |      |      | dB    |
|  | 1.0 - 4.0 GHz   | ± (0.2 + 3% of Atten. Setting) Max. |      |      | dB    |
|  | 4.0 - 5.0 GHz   | ± (0.3 + 5% of Atten. Setting) Max. |      |      | dB    |
|  | 5.0 - 5.5 GHz   | ± (0.4 + 8% of Atten. Setting) Max. |      |      | dB    |
| Input Power for 0.1 dB Compression   | 0.1 - 5.5 GHz   |                                     | 27   |      | dBm   |
| Input Third Order Intercept Point<br>(Two-Tone Input Power= 0 dBm Each Tone) | 0.1 - 5.5 GHz   | REF - 4 dB States                   | 50   |      | dBm   |
|  |                 | 5 - 15 dB States                    | 45   |      | dBm   |
| Switching Characteristics  | DC - 5.5 GHz    |                                     |      |      |       |
| tRISE, tFALL (10/90% RF)   |                 |                                     | 95   |      | ns    |
| tON, tOFF (50% CTL to 10/90% RF)   |                 |                                     | 100  |      | ns    |

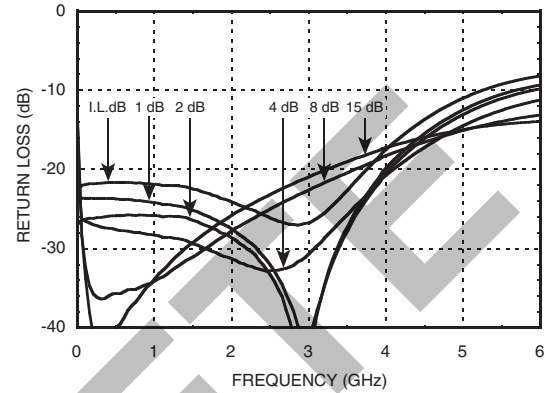
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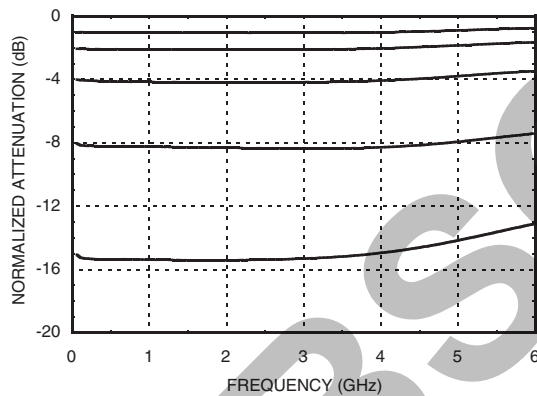
**Insertion Loss**



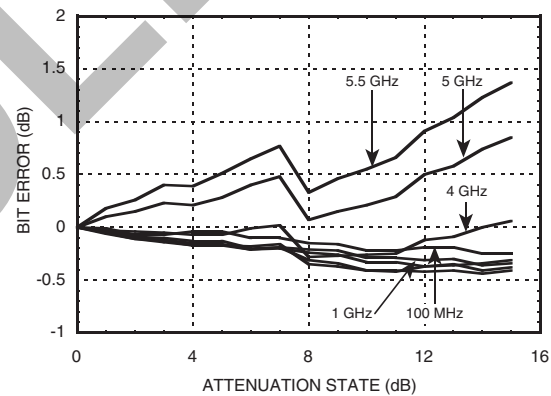
**Return Loss RF1, RF2**  
(Only Major States are Shown)



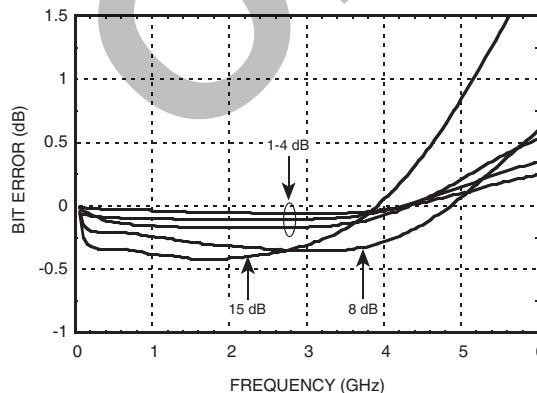
**Normalized Attenuation**  
(Only Major States are Shown)



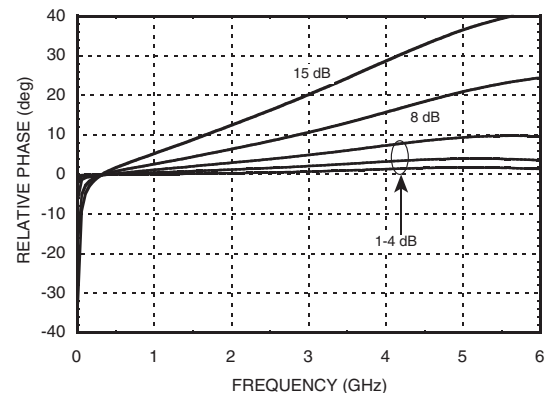
**Bit Error vs. Attenuation State**

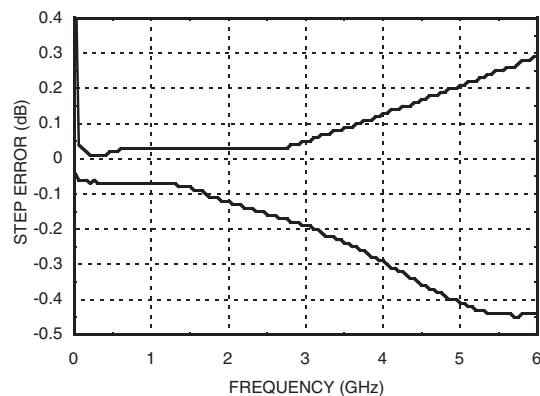


**Bit Error vs. Frequency**  
(Only Major States are Shown)



**Relative Phase vs. Frequency**  
(Only Major States are Shown)




**Worst Case Step Error**
**Between Successive Attenuation States**

**Bias Voltage & Current**

| Vdd = +5.0 Vdc ± 10% |                 |
|----------------------|-----------------|
| Vdd (VDC)            | Idd (Typ.) (mA) |
| +4.5                 | 3.0             |
| +5.0                 | 3.2             |
| +5.5                 | 3.4             |

**Control Voltage**

| State | Bias Condition                 |
|-------|--------------------------------|
| Low   | 0 to +0.8V @ -5 uA Typ.        |
| High  | +2.0 to + 5.0 Vdc @ 40 uA Typ. |

Note: Vdd = +5V

**Truth Table**

| Control Voltage Input |            |            |            | Attenuation State<br>RF1 - RF2 |
|-----------------------|------------|------------|------------|--------------------------------|
| V1<br>8 dB            | V2<br>4 dB | V3<br>2 dB | V4<br>1 dB |                                |
| High                  | High       | High       | High       | Reference I.L.                 |
| High                  | High       | High       | Low        | 1 dB                           |
| High                  | High       | Low        | High       | 2 dB                           |
| High                  | Low        | High       | High       | 4 dB                           |
| Low                   | High       | High       | High       | 8 dB                           |
| Low                   | Low        | Low        | Low        | 15 dB                          |

Any combination of the above states will provide an attenuation approximately equal to the sum of the bits selected.

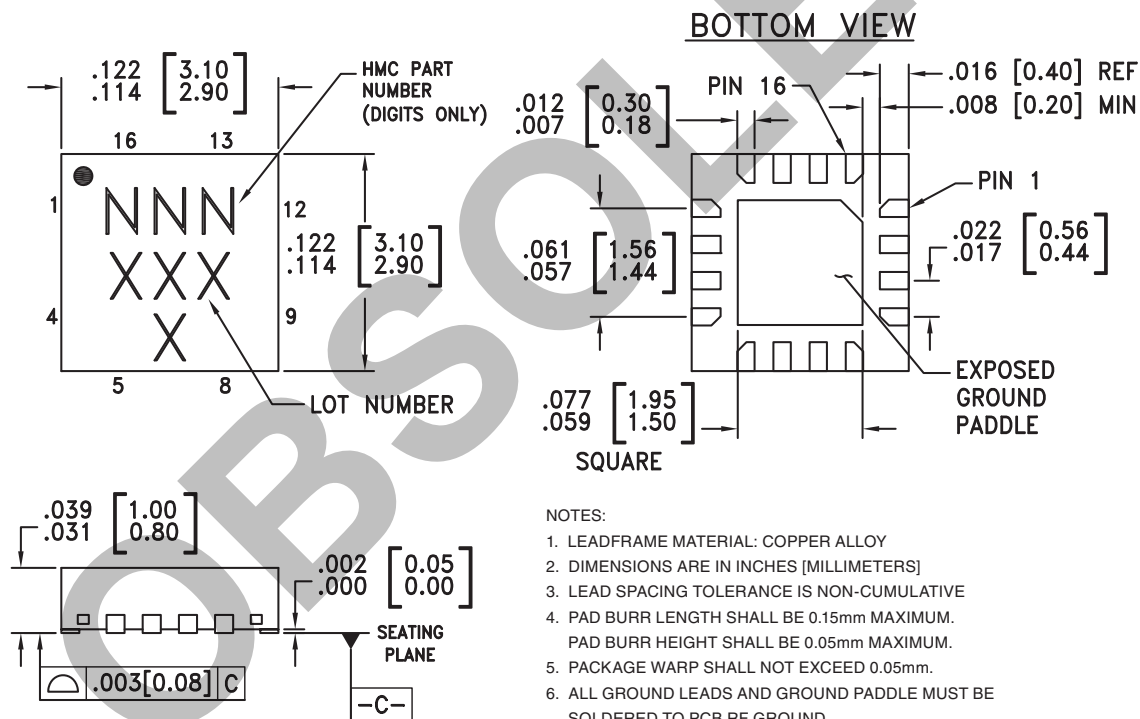
### Absolute Maximum Ratings

|   |                      |
|---|----------------------|
| RF Input Power (DC - 5.5 GHz)                                   | +29 dBm (T = +85 °C) |
| Control Voltage Range (V1 to V4)                                | -1V to Vdd +1V       |
| Bias Voltage (Vdd)  | +7.0 Vdc             |
| Channel Temperature   | 150 °C               |
| Continuous Pdiss (T = 85 °C)<br>(derate 11.7 mW/°C above 85 °C) | 0.769 W              |
| Thermal Resistance  | 85 °C/W              |
| Storage Temperature   | -65 to +150 °C       |
| Operating Temperature   | -40 to +85 °C        |



**ELECTROSTATIC SENSITIVE DEVICE  
OBSERVE HANDLING PRECAUTIONS**

### Outline Drawing



### Package Information

| Part Number | Package Body Material                              | Lead Finish   | MSL Rating          | Package Marking <sup>[3]</sup> |
|-------------|--|---------------|---------------------|--------------------------------|
| HMC540LP3   | Low Stress Injection Molded Plastic                | Sn/Pb Solder  | MSL1 <sup>[1]</sup> | 540<br>XXXX                    |
| HMC540LP3E  | RoHS-compliant Low Stress Injection Molded Plastic | 100% matte Sn | MSL1 <sup>[2]</sup> | 540<br>XXXX                    |

[1] Max peak reflow temperature of 235 °C

[2] Max peak reflow temperature of 260 °C

[3] 4-Digit lot number XXXX

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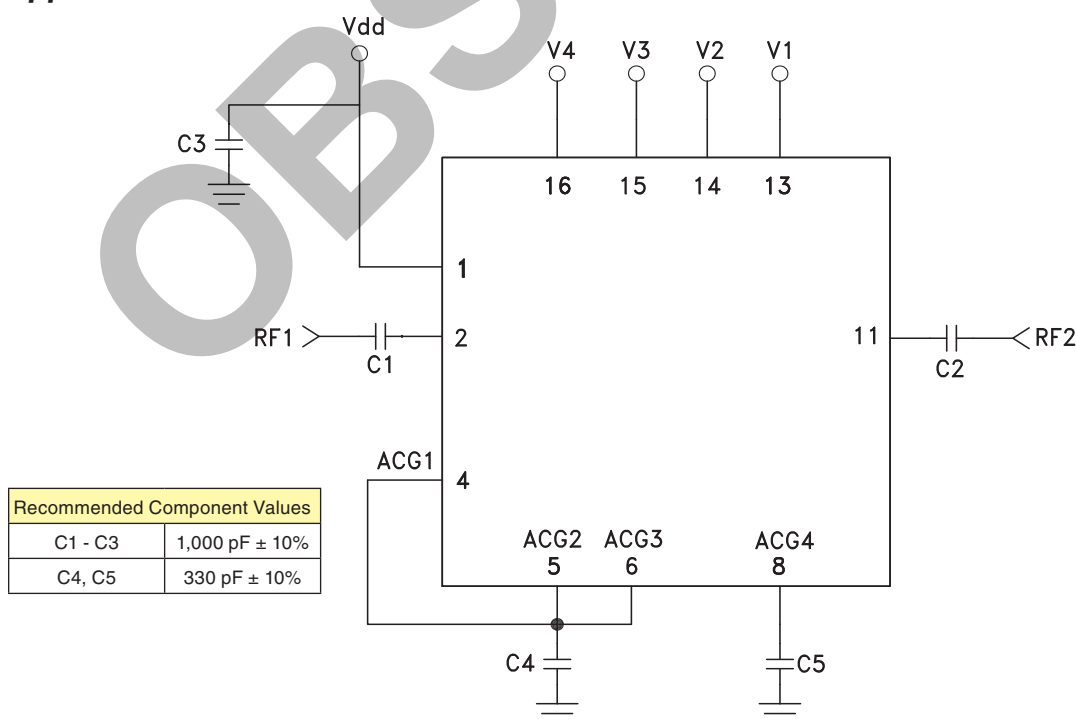
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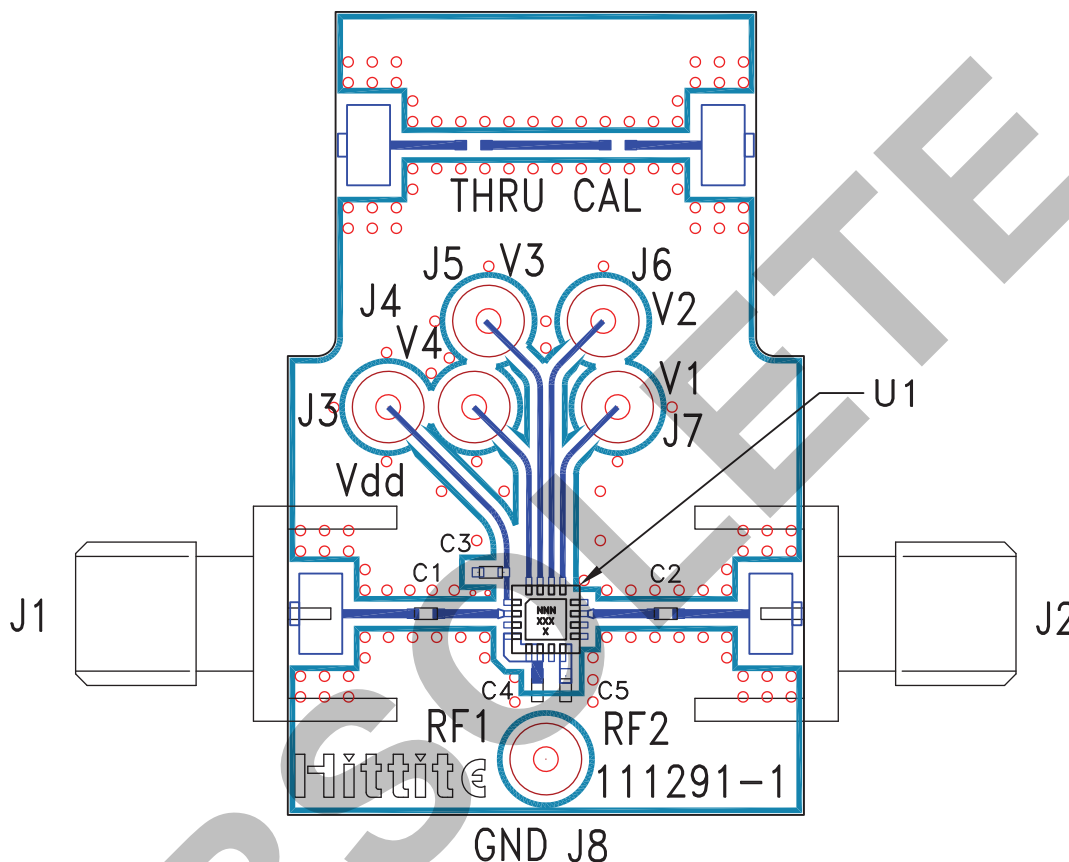
## Pin Descriptions

| Pin Number      | Function    | Description   | Interface Schematic |
|-----------------|-------------|---|---------------------|
| 1               | Vdd         | Supply Voltage.   |                     |
| 2, 11           | RF1, RF2    | This pin is DC coupled and matched to 50 Ohm. Blocking capacitors are required. Select value based on lowest frequency of operation.    |                     |
| 3, 7, 9, 10, 12 | N/C         | These pins should be connected to PCB RF ground to maximize performance.  |                     |
| 4 - 6, 8        | ACG1 - ACG4 | External capacitor to ground is required. Select value for lowest frequency of operation. Place capacitor as close to pins as possible. |                     |
| 13 - 16         | V1 - V4     | See truth table and control voltage table.  |                     |
|                 | GND         | Package bottom has an exposed metal paddle that must be connected to RF/DC Ground.  |                     |

## Application Circuit



**Evaluation PCB**



**List of Materials for Evaluation PCB 111315 [1]**

| Item    | Description                               |
|---------|---|
| J1 - J2 | PCB Mount SMA Connector                   |
| J3 - J8 | DC Pin                                    |
| C1 - C3 | 1000 pF Capacitor, 0402 Pkg.              |
| C4, C5  | 330 pF Capacitor, 0402 Pkg.               |
| U1      | HMC540LP3 / HMC540LP3E Digital Attenuator |
| PCB [2] | 111291 Evaluation PCB                     |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.