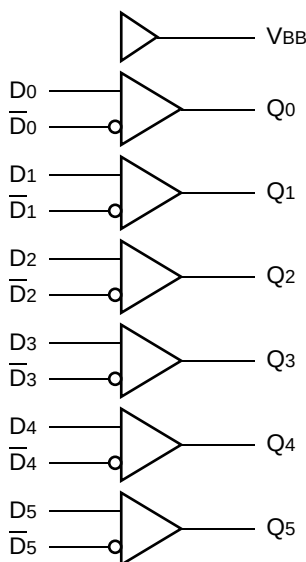


FEATURES

- Max. propagation delay of 3.7ns
- IEE min. of -37mA
- TTL outputs
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- 25% faster than National's 325
- Differential inputs with built-in offset
- Voltage and temperature compensation for improved noise immunity
- VBB output for single-ended use
- Internal 75KΩ input pull-down resistors
- Function and pinout compatible with Fairchild F100K
- Available in 24-pin CERPACK and 28-pin PLCC packages

BLOCK DIAGRAM

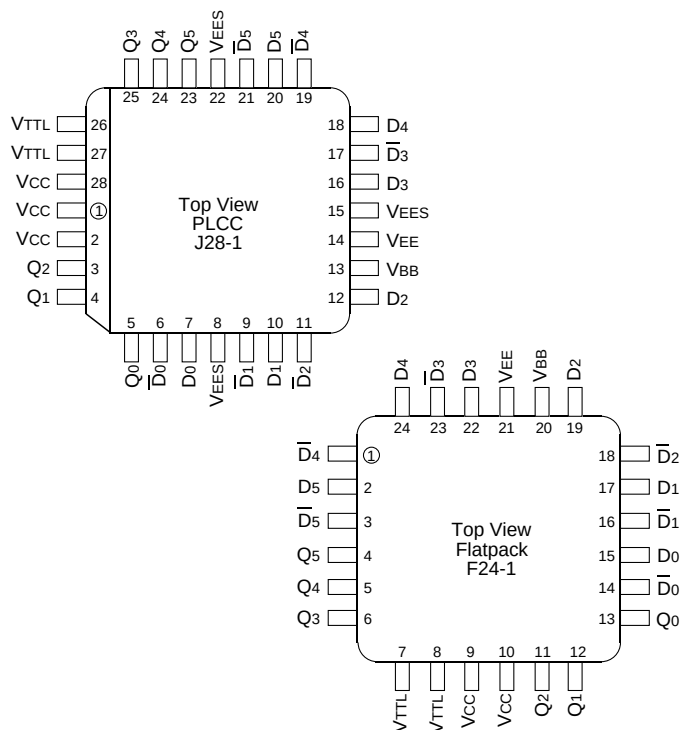


DESCRIPTION

The SY100S325 are hex translators for converting 100K ECL logic levels to TTL logic levels. Inputs can be used as inverting, non-inverting or differential receivers. An internal reference voltage generator provides VBB for single-ended operation or for use in Schmitt trigger applications. All inputs have 75KΩ pull-down resistors. The outputs will go LOW when the inputs are either open or have the same potential.

When used in single-ended operation, the apparent input threshold of the true inputs is 20mV to 40mV higher (positive) than the threshold of the complementary inputs. The VTTL and VEE power may be applied in either order.

PIN CONFIGURATIONS



PIN NAMES

Pin	Function
D0-D5	Data Inputs
D0-D5	Inverting Data Inputs
Q0-Q5	Data Outputs
VEES	VEE Substrate
VTTL	TTL Vcc Power Supply
VCCA	Vcco for ECL Outputs

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition	
VOH	Output HIGH Voltage	2.5	—	—	V	IOH = −2.0mA	VIN = VIH (Max.) VIN = VIL (Min.)
VOL	Output LOW Voltage	—	—	0.5	V	IOL = 24mA	
VDIFF	Input Voltage Differential	150	—	—	mV	Required for Full Output Swing	
VCM	Common Mode Voltage	—	—	1.0	V	Permissible ±VCM with Respect to VBB	
IIH	Input HIGH Current	—	—	350	μA	VIN = VIH (Max.), D0–D5 = VBB, <u>D0–D5</u> = VIL (Min.)	
IIL	Input LOW Current	0.5	—	—	μA	VIN = VIH (Min.), D0–D5 = VBB	
Ios	Output Short Circuit Current	−150	−80	−60	mA	VOUT = GND	
IEE	VEE Power Supply Current	−37	−24	−17	mA	D0–D5 = VBB	
ITTL	VTTL Power Supply Current	—	42	65	mA	D0–D5 = VBB	
VBB	Ouptut Reference Voltage	−1380	−1320	−1260	mV	IVBB = −2.1mA	
VIH	Single-Ended Input HIGH Voltage	−1165	—	−880	mV	Guaranteed HIGH Signal for All Inputs (with One Tied to VBB)	
VIL	Single-Ended Input LOW Voltage	−1810	—	−1475	mV	Guaranteed LOW Signal for All Inputs (with One Tied to VBB)	

AC ELECTRICAL CHARACTERISTICS

PLCC/FLATPACK

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	900	2100	2900	ps	$C_L = 15pF$, Figure 2
t_{PLH} t_{PHL}	Propagation Delay Data to Output	900	3100	3700	ps	$C_L = 50pF$, Figure 2

SWITCHING WAVEFORM

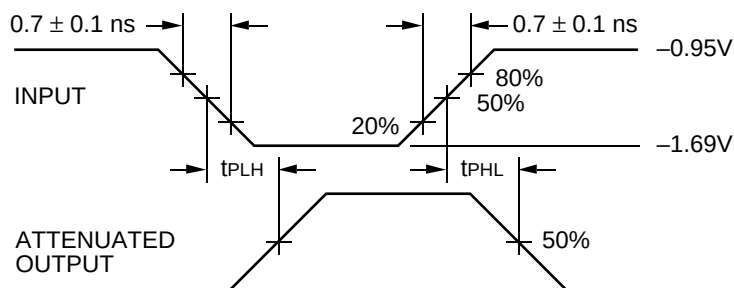


Figure 1. Propagation Delay

NOTE:

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

TEST CIRCUITS

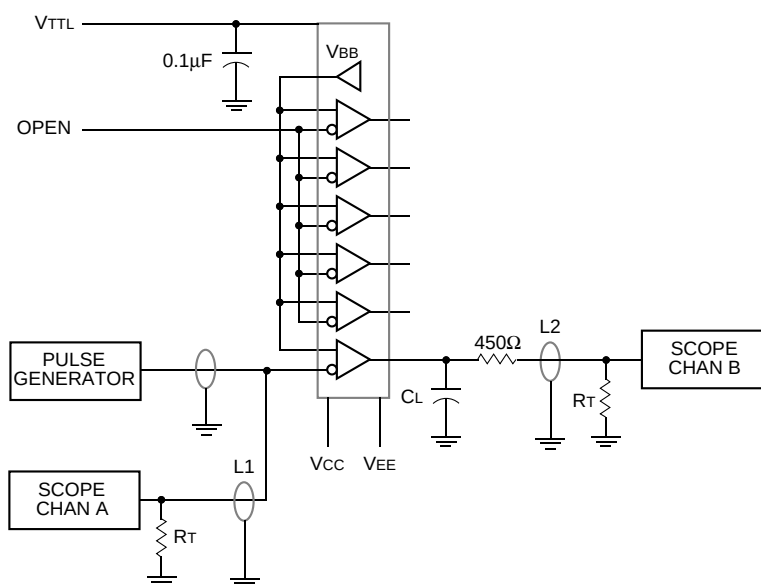


Figure 2. AC Test Circuit for 15pF Loading

NOTES:

$V_{CC} = 0V$, $V_{EE} = -4.5V$, $V_{TTL} = +5V$

L1 and L2 = equal length 50Ω impedance lines

$R_T = 50\Omega$ terminator internal to scope

Decoupling 0.1μF from GND to V_{CC} , V_{EE} and V_{TTL}

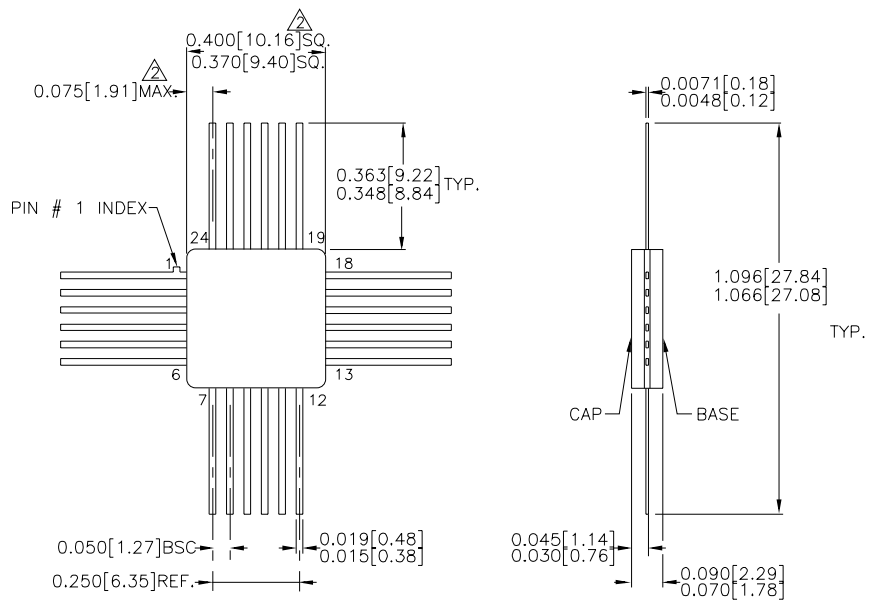
All unused outputs are loaded with 500Ω to GND

C_L = Fixture and stray capacitance = 3pF

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S325FC	F24-1	Commercial
SY100S325JC	J28-1	Commercial
SY100S325JCTR	J28-1	Commercial

24 LEAD CERPACK (F24-1)

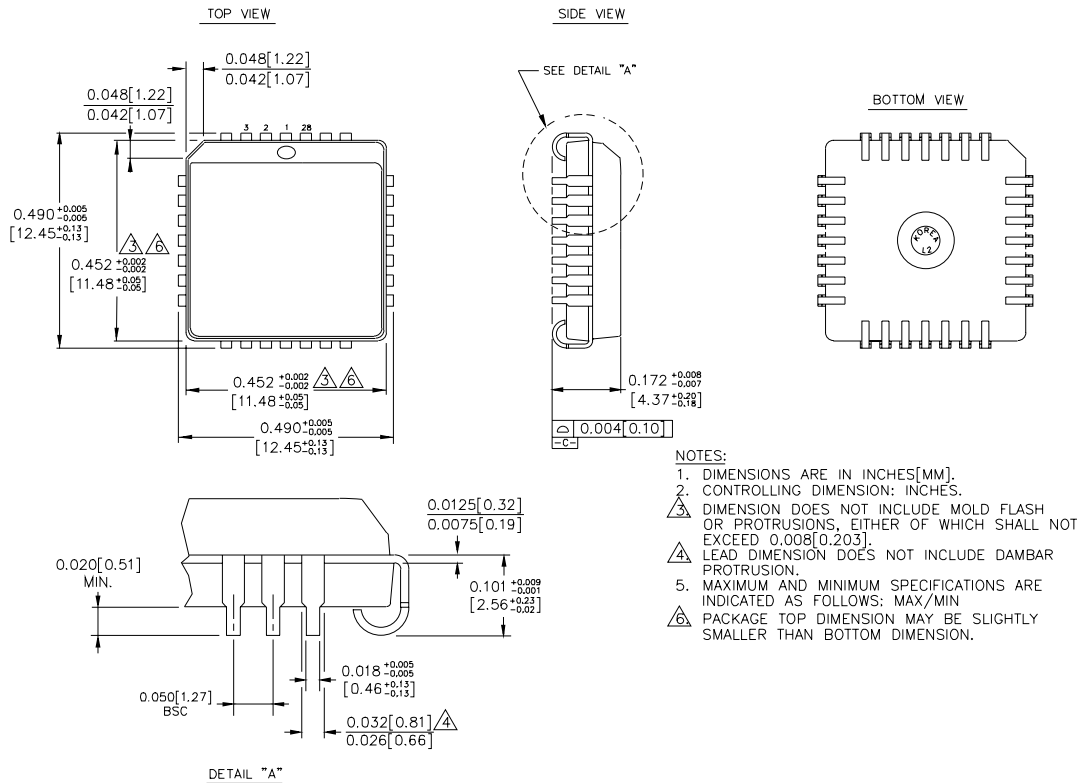


NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev. 03

28 LEAD PLCC (J28-1)



Rev. 03

MICREL-SYNERGY 3250 SCOTT BOULEVARD SANTA CLARA CA 95054 USA

TEL + 1 (408) 980-9191 FAX + 1 (408) 914-7878 WEB <http://www.micrel.com>

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